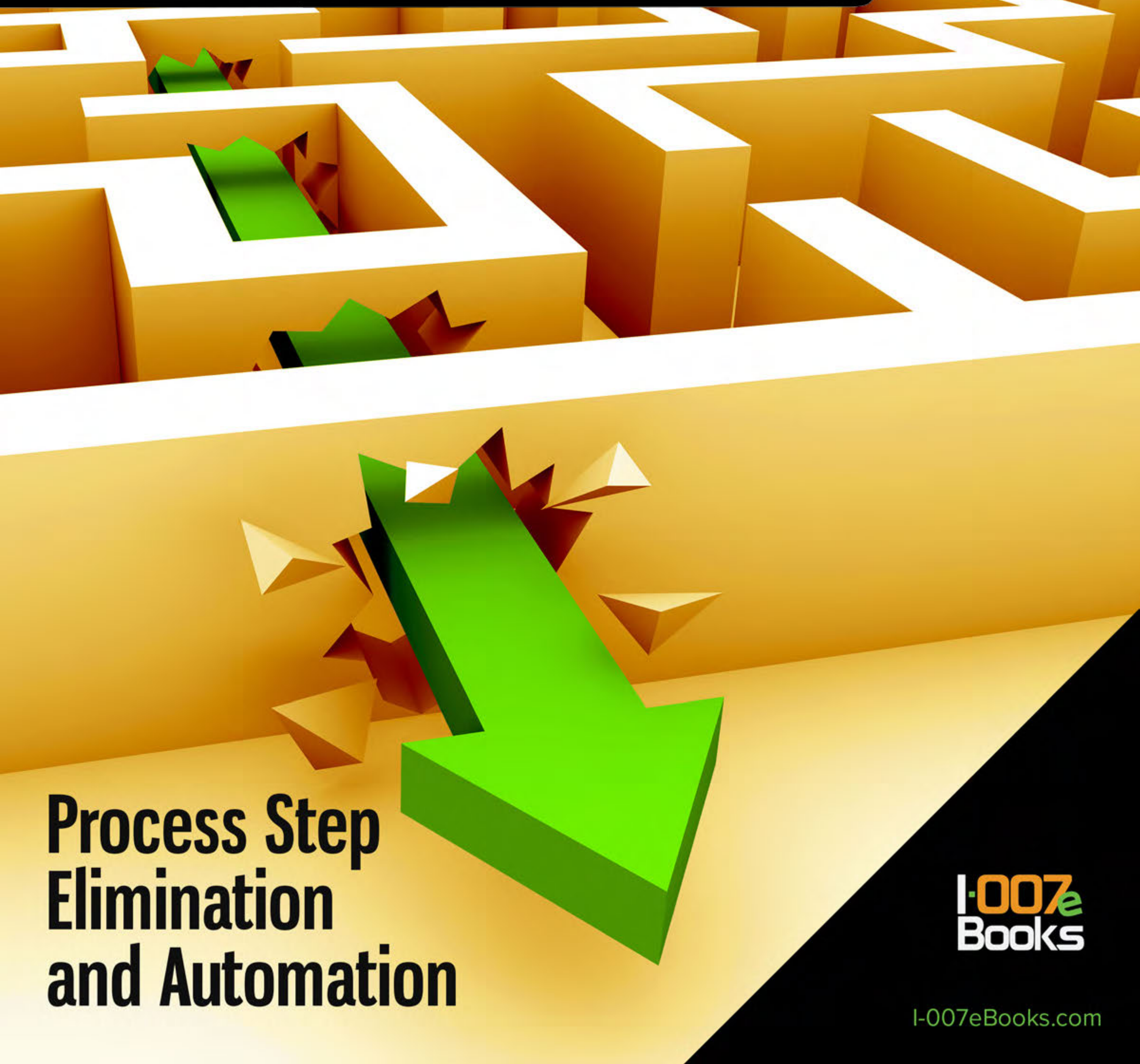
I-Connect007 Presents

August 2017

the pcb magazine



Process Step Elimination and Automation

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the pcb magazine

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Process Step Elimination & Automation

Exactly what defines process step elimination and/or automation? So many possibilities! Does it include reducing the number of steps in manufacturing a PCB? Eliminating queue times, inspection or cleaning steps? Is automation adding a hoist to your plating line, or conveyorizing everything? These considerations and more by industry experts will give you plenty to think about as the summer sun sets on the horizon.

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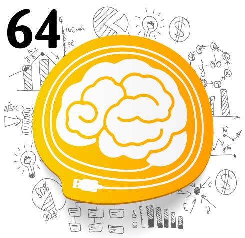

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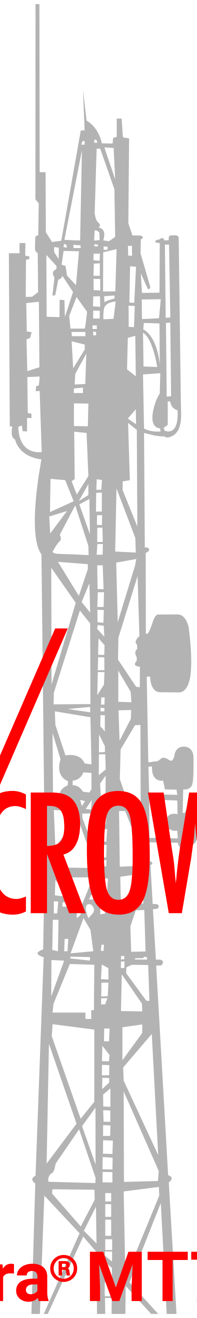

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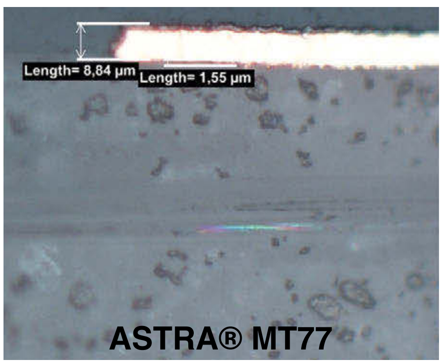

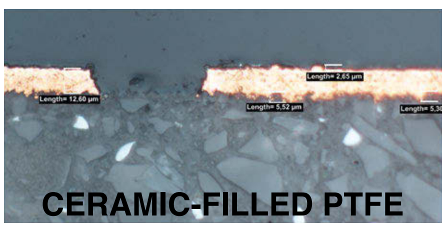

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How do You Define Process Step Elimination and Automation?

by Patty Goldman
I-CONNECT007

This month, we can call our theme PSE&A—a fancy acronym for process step elimination and automation. Sounds straightforward, but what exactly do we mean by "process step elimination?" Does it refer to shortening the numerous steps involved in making a printed circuit board? There sure are a lot of them, but they all must be necessary—or why would we have them?

Or perhaps it means eliminating unnecessary steps such as wait or queue times, extra inspections, extra cleaning processes, etc. Or, could process step elimination include actual steps, physical or otherwise, that an operator or engineer takes to perform their duties?

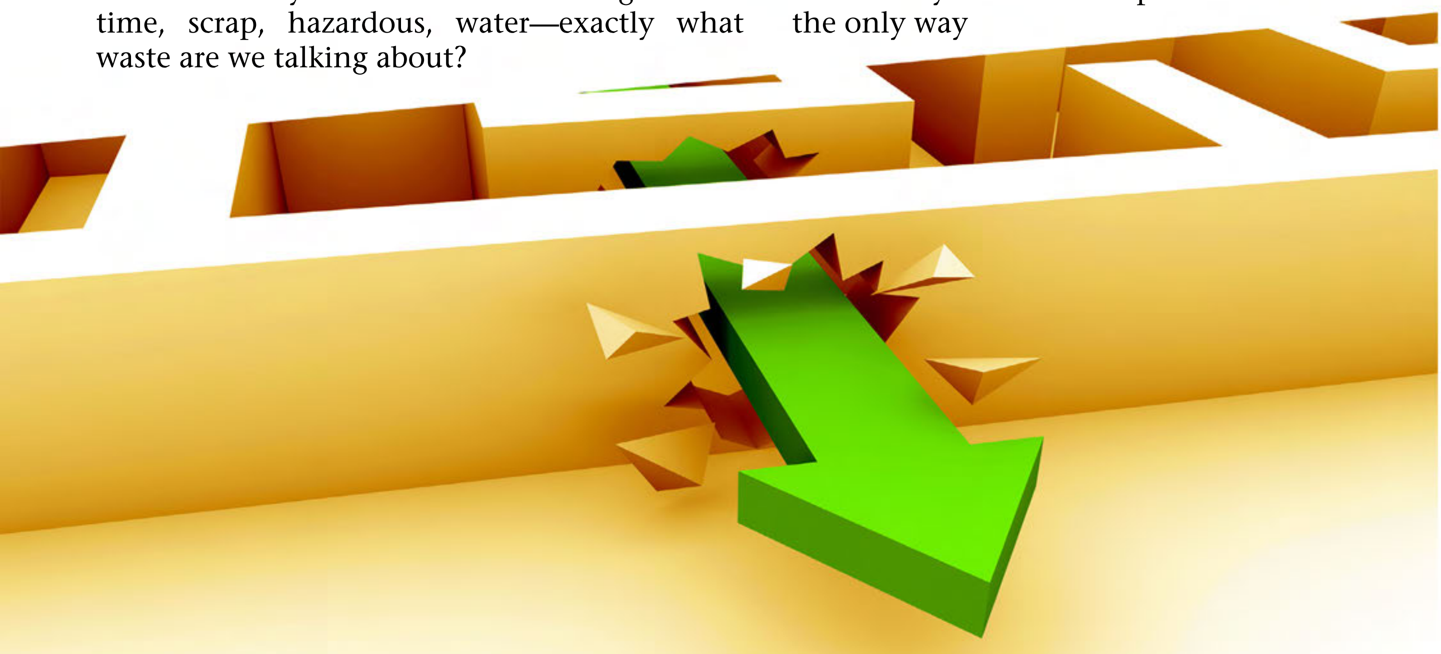
'Automation' is an equally broad term. Does it mean load/unload stations, an automatic hoist on your plating line, or perhaps conveyorizing everything possible in the process? Or, does it mean automating some lab analysis and replenishment tasks?

Another way of looking at extra steps is to consider them waste or non-value-added. Ah, but waste is yet another far-reaching term—time, scrap, hazardous, water—exactly what waste are we talking about?

Maybe PSE&A means all these things. That seems overwhelming! There isn't a PCB facility in the world that doesn't want to remove as many steps in as many areas as possible, but of course there are constraints. These are usually in the form of available capital to purchase new equipment that is more automated, plus possibly shortening the process steps.

How can we help with this? Well, I'm hoping our articles and columns this month will give you plenty of food for thought, some good tips, and perhaps a healthy dose of inspiration for improving your processes while saving time and money. Let's get started.

It's been two years since we first discovered Whelen Engineering, a private manufacturer of alarms and sirens in New Hampshire. Whelen management decided to bring their PCB manufacturing back to the U.S. because they were spending $7 million a year for circuit boards in Asia and the delivery times were long. They hired an ace engineer and gave him a mandate: Build a PCB facility for our needs with an ROI of less than five years. Alex Stepinski found that the only way



he could meet Whelen's criteria was with a fully automated line such that a minimum number of people were needed and all materials were recycled. For this issue, we decided to check in and find out what's happening and how it's working out. We talked with Alex and that conversation is our lead article this month.

Steve Williams of The Right Approach Consulting introduces us to a new concept, W.O.R.C. cells, developed specifically for high-mix, low-volume operations…like yours. Steve discusses the three types of cells—physical, virtual and hybrid—and goes into detail on setting this up, complete with a couple of case studies. You'll learn what W.O.R.C. stands for and can decide for yourself if this makes sense for your company.

Columnist Marc Ladle, Viking Test, came away from a recent factory install in Europe impressed by the inkjet technology he saw and he wanted to share with us. The process for primary image he describes eliminates not just the artwork but also the developing step—and can be fully automated.

A very interesting paper was presented at IPC this spring by ESI (Schrauben, et al.) that describes using glass as a substrate for high-frequency PCB applications. The process involves laser etching to create the circuit pattern followed by laser deposition of copper. Perhaps still in its infancy, but the capability for extremely fine features makes it a definite consideration.

We all know the importance of eliminating waste, at least what we call "scrap." But what about wasted time and energy? How is that accounted for? Or do we mostly just accept it as a necessary? You may have heard it before, but Todd Kolmodin of Gardien Services reviews the 5S system for us and admonishes us with the adage, "work smarter, not harder." It might be time (or past time) to apply this to your workplace.

Switching gears, a bit, Omni PCB's Tara Dunn discusses ways to drive cost from flex designs. It may not be that simple, but there are a few basics that can help, focusing on fab capabilities, material choices and communications. Note that reducing cost almost always results in reduced time and waste—surprise!

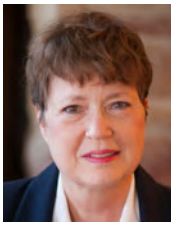
Now to the off-theme, but technical portion of the magazine…and we have a couple of good ones. First, Mike Carano, RBP Technology, moves away from troubleshooting and gives us an introduction to microvias and HDI. HDI is the subject of an upcoming IPC conference (see Events page near the end of the magazine), which may have gotten Mike started on this subject.

In another technical paper, from MacDermid (Dharmarathna, et al.), the focus is on acid copper for a vertical continuous electroplating process. Extensive performance and testing data are presented.

With a tongue-in-cheek title, NTS's Keith Sellers talks about the rather serious subject of traceability. Some end customers don't care, but in the automotive, medical and military/aerospace arenas it is becoming an increasing necessity. Can you trace a defective PCB back to the day and time it was processed—and know all the processing parameters that were in play then? While such a scenario may not happen, the idea is that there is a troubleshooting advantage to having ultimate traceability.

Wrapping up is IPC's John Mitchell with a report on the manufacturing industry in India. With a population to rival China and engineers to match, only a poor infrastructure seems to be holding India back. In fact, India is expected to be a top five manufacturing nation by 2020 (note: that's just around the corner).

OK, enough for one month. Digest this month's issue and put into practice what you can. And, heads up, next month it's all about process engineering. What is it, what do those guys do, and what should they be doing? We'll try to answer it all and give them a boost at the same time. Tune in, pay attention and for sure you've already subscribed, right? Don't make me tell you again! **PCB**



Patricia Goldman is managing editor of *The PCB Magazine.* To contact Goldman, click here.

Overview of the Whelen automated PCB line.

Whelen Engineering, Two Years Later

If you know anything about this unusual (and extremely private) company, you probably read it right here at I-Connect007. Whelan Engineering's truly unique PCB manufacturing operation is the result of a company initiative to bring their PCB needs back into the States—and do so at a cost savings. It has been quite a success, largely due to the efforts of brainchild Alex Stepinski, now VP–PCB at Whelen. The company is still in the thick of manufacture, including an expansion of the PCB facility.

We published our first article on Whelen in the October 2015 issue of *The PCB Magazine*. Then, we published Alex's "how-to" paper that he presented at IPC's Spring meeting and conference in June 2016. By reading that article carefully, you can learn a great deal about automating your process using off-the-shelf items.

This time I had the privilege to accompany Happy Holden (with I-Connect007 colleagues Jonathan Zinski and Bryson Matties) to visit Whelen's PCB operation in the far reaches of New Hampshire.

Patty Goldman: Alex, it's good to be here at Whelen to see your process firsthand. It's been two years since I-Connect007 last visited when you were just getting started. Now we're interested in an update on this, the most automated PCB factory in North America. How's it going, and how are things running?

Figure 1: Happy Holden (left) and Alex Stepinski discuss Whelen's process in detail.

Alex Stepinski: The process has stabilized since the last conversation, and it's very predictable now from a quality perspective. From a labor perspective, we have consistent schedules and predictable labor and delivery schedules; we have predictable quality at this point. It's a robust process, and it essentially runs itself, the control plan that's in place.

Goldman: How was the startup?

Stepinski: The startup was challenging from a couple of perspectives. One was the inkjet technology and the second was reliance on smaller suppliers to deliver on a consistent basis. We had some late deliveries on things as well.

Goldman: Once everything was installed, did it take a few months to get everything smoothed out?

Stepinski: It was a few months to balance in the chemistries for recycling. The recycling was the biggest challenge there, because we kind of went out on our own in developing things. We didn't have all of the equipment configured from the beginning; we couldn't find any supplier that could give us full systems for recycling, even though we looked diligently. Everybody had only half measures; nothing was complete.

We bought a lot of half measures and connected the dots to make a system, and this required a lot of research, data collection, adjustments, improvements, and updates, to get to the closed-loop efficient system. A closed-loop inefficient system was how we started, and a closed-loop efficient system was where we ended up.

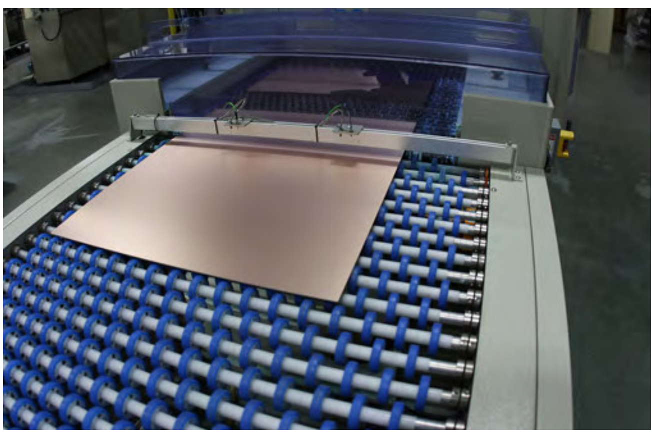


Figure 2: IPS conveyor line.

Happy Holden: I have a couple questions on the inkjet printing. Both the innerlayer imaging and outer layer imaging utilize the same etch and strip equipment in the line but in a different order—for outer layers you strip and etch. I asked you earlier about this and you indicated that the innerlayers and outer layers aren't interspersed, they're run batch-wise. It's a manual intervention in terms of bypassing one process because it's been turned off and using another one. That's done manually. I assume then that there's an accumulator there?

Stepinski: Yes.

Holden: So if you're running innerlayers, you can still run outer layers, and the outer layers go into the accumulators while it's processing innerlayers, and then once you're finished with innerlayers it takes the outers out of the accumulator and runs on. It's probably a quick switchover between innerlayers and outer layers, but it's not done automatically. It's done manually since they're all inline. The other question about the accumulators was, are they also for the fact that all the conveyors don't run at the same speed? Is that why there's an accumulator for that optimal process?

Stepinski: It's actually not because of speed. The speeds have all been balanced. The accumulators are going from a continuous process to a batch process; that's where we have accumulators. Not for speed, because the average speed coming out of the batch processes matches the continuous processes. It's just that they can't take them at the same rate, the same interval. For instance, an inkjet machine will probably deliver two panels at about the same time, and then there'll be a two-minute delay, and then it takes the next two. It's not doing one every minute.

Holden: But if you had a change in thickness of the copper from one product line to another, you'd have to slow down the horizontal plater,

Figure 3: Strip-etch-strip line.

and then wouldn't all the other machines have the wrong immersion time?

Stepinski: But that's the slowest line so it doesn't really matter.

Holden: If you had a spec that called for twice as much copper, that machine would have to be even slower. Do you have the flexibility of changing the current density or the pulse rate to keep the conveyor the same speed and double the amount of copper? Or, do you have to actually reduce the conveyor speed, changing the immersion time?

Stepinski: It depends on how much copper.

Holden: Everything tied together means everything has to be balanced. One reason why processes are separated is because you might say for maximum throughput, the conveyors run at different speeds, and so you have isolated conveyorized processes, with manual loads and unloads.

Stepinski: Relative to that, the individual loaders/unloaders, when a panel enters then, and they all automatically center the panels, because you get drift going through horizontal equipment. Every time we go through a loader/unloader, we center and then we change the speed immediately after centering to get the panel out. That deals with the speed changes.

We can deal with speed changes at that level as well so we don't burn out on the material. We're entering the load/unload station, at the speed of the preceding line, stopping, centering, and then exiting at next line speed. The gaps are managed accordingly. The speed of the etcher is almost one-to-one with the speed of the plater; we've matched that. If the plater runs at one meter a minute, the etcher runs at one meter a minute. If the plater runs at half a meter a meter a minute, the etcher runs at half a meter a minute. Remember, we're panel plating, so if the plater is running at half a meter a minute, it's putting on twice as much copper. Then the etcher runs slower and it matches. It's all matched and balanced.

Holden: This is an unusual line in that it's panel-plated plus patterned tin. It's not a conventional panel plate line; it's kind of a panel/pattern hybrid.

Stepinski: That was the lowest-cost solution I could come up with.

Goldman: Meaning lowest cost to do the panel.

Stepinski: Yes.

Holden: I'm surprised that the companies that sell inkjet printing for solder mask haven't come out with a plating or etch resist machine or mask. Yours are adapted with this wax-based ink. Where did you start on that inkjet printing for resist and for pattern plating? They're not really even available now, so you made an obvious choice to custom engineer that level of inkjet printing. You're not ink formulators, so...

Stepinski: No, Dow formulated the ink. We tested it here and validated that it worked before we bought the equipment. When the machine showed up, we optimized the preceding and follow-up processes to handle it. There were a few uncertainties in designing the process. I planned it very quickly, so I had to compensate for the uncertainties. We have a preclean in front of the line, and it turns out that


Figure 4: Horizontal pulse plater.

is an unnecessary process, it's non-value added. It was originally designed as a subtractive etch process. We were able to modulate the plating recipes to pulse the right amount of roughness on at the last anodes, and we were able to eliminate the subtractive etch with the roughness or stripping process after inkjet so it would in effect strip it and do tin plating and handle surface treatment because we're plating it in. Even though it's there, we're not using it. I didn't know we'd be able to get that good.

Holden: Is anyone else using a horizontal pulse plater to improve the resist adhesion?

Stepinski: It was recommended to us by Atotech. They said they had a handful of accounts that had been able to achieve it. What we had to do was do the DOE to see what roughness worked best with the inkjet ink. The inkjet ink has extremely good adhesion, and you can't make it too rough. The product is so thin that when it hits the surface, it penetrates every crack, every nook and cranny in the crystal structure, unlike a dry film, which is extremely viscous, and you have to push it in.

Holden: Is that UV-cured or thermally cured?

Stepinski: This is a UV-cured product. It gets a dose of 900 millijoules.

Holden: And that machine has a built-in AOI. Is there anything else built-in?

Stepinski: No, that's basically it. It's the AOI, and cure and coating.

Holden: And the pinless lamination saves a lot of process steps. Since you're not using pins, you don't have the messy caul-plates to deal with.

Stepinski: Or maintenance program, yes.

Holden: It's an optical alignment, and then kind of a welding of the layers together.

Goldman: How well does that work?

Stepinski: For our technology, it's fine.

Holden: I noticed the rotary oxygen plasma etch replaces all the permanganate desmear. Does that have sufficient throughput?

Stepinski: Yes.

Goldman: The rotary plasma etch, though, that's really a batch process. How automated can you make that? Somebody has to load and unload right?

Stepinski: Yes, and the plasma machine is a limiting factor with higher volume. You're not going to get 100 plasma machines by a chemical desmear line. For us, the rotary plasma machine makes sense.

Holden: Because of the high level of automation and the minimum of any kind of delay, there's an elimination, a lot of outer layer and innerlayer pre-etch, acids, and things like that that people have because panels are sitting around.

Stepinski: Fingerprints.

Holden: Those all have to be eliminated. If it's not touched by people then there's no chance. Plus, your equipment is really designed under the concept of a microclimate. The building is not specifically climate-controlled because there's a microclimate inside of the process area

and it can be kept extra clean and conditioned. Also, you have a concept of no fume scrubbers. I think one time you wrote that, wherever possible, you've elevated the temperature to facilitate evaporation, which is one of the ways of recycling the chemicals.

Stepinski: Yes, thermal energy instead of chemical energy.

Goldman: Is the copper that you produce from etching usable in your copper plating process?

Stepinski: Yes. It's been qualified but we don't put it in there right now. The concern is that in the theoretical world, it works fine. The concern is that someday, somebody is going to put in some copper that still has some ammonia on it or something like that, on fifth shift or something like this. I have this nightmare—this nightmare that has never happened to us, but it pops into my head in the middle of the night. We get paid 95% of the anode price anyway, so we're covering the cost basically. For 5% more, I avoid a lot of potential risk. But it has been certified by Atotech to be reused. They don't do that lightly.

Goldman: It's an insurance policy.

Holden: The conductive polymer that replaces electroless copper—what are the trade-offs between the two?

Figure 5: Horizontal conductive polymer process.

Stepinski: Electroless copper is more expensive to maintain and analyze in a conventional factory. It's also an environmental liability. We've done a lot of work to develop countermeasures so it's not an environmental liability in our factory.

Goldman: How has it been working in the line? Has it been 100% reliable? Right now, I know you're mostly doing single- and double-sided.

Stepinski: The conductive polymer is working fine. It's a no-brainer. I don't know of any issues. We do a low percentage of multilayer but have had no issues. It's an extremely reliable process.

Holden: What is the mechanism of the conductive polymer?

Stepinski: The conductive polymer mechanism is putting down the permanganate, and the conductive polymer is an acid permanganate. You're actually precipitating manganese dioxide onto the dielectric surface, and then the conductive polymer absorbs onto it and gets conductive enough to galvanically plate it up.

Goldman: Because you're going right to panel plating in the acid copper, with just a few rinse steps. I suppose that helps.

Stepinski: Yes, and the conductive polymer itself has a pH of 1.9. The whole line is acidic permanganate polymer and galvanic copper. The conditioner on the front of the line is alkaline; it's just a wetting step. The only limitation with the conductive polymer process is that on more exotic materials it doesn't absorb as well. In those cases, you're in the electroless arena.

Goldman: You mean anything beyond FR-4? Like polyimide or flex?

Stepinski: No, we were able to do polyimide. We have flex and it's not been a problem. As long as there is no acrylic through the process. If you expose acrylic in the hole wall it will chew up the acrylic because of the high temperature of the acid permanganate which is at 90°C (the first step of the conductive polymer process).

Goldman: Other than acrylic, what specialized materials can you not run through?

Stepinski: There are a few where you have lower deposition rates that you have to run it through multiple passes. Some of the Megtron materials for instance are a little more challenging. Those materials may leach out as well.

Holden: One of the questions I had was about the maximum lot size or order size.

Stepinski: We have up to 1,000 panel lots right now. Minimum lot size is one.

Goldman: Of course, because you can automatically change…

Stepinski: Yes, it's pretty automatic.

Goldman: Put that part number in or whatever and everything changes down the line as necessary.

Stepinski: As long as it's part of the same kind of family of product, yes. If it's a different product family then no, we have to intervene a little bit, just mainly changing some things. For instance, if you go from double-sided to multilayer, there are a couple of slight changes. If you go from double-sided to single-sided, there are some changes. We have one recipe for IPC-6012 Type 1, one for Type 2, one for Type 3.

Goldman: Interesting. You have different recipes and that's part of the programming.

Stepinski: Yeah, within our thickness limits.

Holden: Is the front-end tooling done here?

Stepinski: It's actually done in New York state for the most part. I have a tooling team in New York state of former employees of mine from another fabricator. They've been trained over here, the designs get sent over there, and they do all the tooling and send them over.

Holden: I was thinking, since there's no artwork, are there any new files required here that haven't been a conventional part of tooling? We've had direct imaging for a while.

Stepinski: Not really, no.

Holden: Once you start utilizing any kind of direct imaging, you have those artwork files. We've always had drill/router files, and we've always had electrical test files. There are no changes in the files between an inkjet printer and, say, the laser direct imaging.

Stepinski: There's one more step in between for the inkjet, but it's just a quick software step that's automated.

Goldman: You also said that there are files for drill rout, files for solder, files for direct imaging, even the tacking. If that's automated, there have to be files for that too, right?

Stepinski: Yes.

Holden: Is there a file for AOI?

Stepinski: Yes. It's all CAD reference.

Goldman: I want to ask about yields. Has there been a ramp-up? What are you seeing yieldwise? I think this is something the readers would be interested in.

Stepinski: The yields have been solid—in the high 90s. We've had some issues with the inkjet from time to time but we've captured all those and corrected them. When we have rework it's a very, very small amount. What we would have more than anything would be downtime. We capture these things quickly and the downtime is the big risk.

Goldman: Do those captures happen automatically? If there is a problem, is there something that stops things?

Stepinski: Yes, but there's a little gap sometimes. For direct defects, you can capture them at the machine; it's for interactive problems where you have some subtle issue with the ink or something like that. That turns into a plating problem, and it takes a little longer, and then you have some panels to work on. So far everything is correctable.

Holden: Does the WIP system currently read barcodes?

Stepinski: In the current system, when we release a job to the floor, we print stickers. We don't have travelers here; stickers are coming out of a sticker printer with barcodes on them, and it tells the person at drill how many are in the stack, what material type it is, and then they build the stack and put the sticker on the stack. The drill machine reads the sticker, and then it drills the material codes into the frame.

Holden: How many additional readers are throughout the system?

Stepinski: We have six total—in process, input, and things like that. The part-specific data is at AOI at each imaging step. Then, right at the end, as we build the board, we make another barcode. If you look at finished boards you'll see there's a barcode made by a solder mask and legend, in combination. That gets read by the score machine and the router.

Goldman: Nobody programs anything in; each machine reads the barcode and knows what to do.

Stepinski: Yes, it's a paperless factory.

Holden: What happens if something breaks?

Stepinski: It's like at any other factory. If something breaks, the first thing that happens is that the panels in the previous step get offloaded to the loader/unloader, and when that one fills up it goes to the next loader/unloader. It stops feeding and it cascades all the way back.

Goldman: It must be difficult then, because you lose that advantage of things not sitting.

Stepinski: Usually we can recover very quickly when we have a downtime issue. At a regular shop, what happens is it just gets shoved in the corner somewhere, and then at the production meeting, someone gets notified that there's a big problem. Things don't resolve themselves automatically. Usually, someone's got to push to make sure someone shows up to fix it, or changes somebody's priority to go fix it.

Here, there are different line segments and I think we have seven total line segments broken up, and for each segment, all the critical alarms go into a big megaphone that we make. Whelen makes the megaphones—an emergency warning megaphone. You can have it sound like a British police car, a U.S. fire truck, or whatever. All these sirens. We have seven different sounds, and we've all memorized the sounds. You hear that sound, everybody in the factory goes there. That's how we've functioned, and it's the same way in the new process.

Goldman: I presume you have some sort of preventive maintenance schedule so that doesn't happen very often.

Stepinski: Yes, we have a very detailed preventative maintenance schedule. But, it's not just for breaking that we have sirens. If someone has to change a filter, we get notified as well. If the resist strip drum needs to have the resist taken out of it, the alarms go off too. All these things are what we call critical issues that require labor. The equipment is considered fully autonomous, and when an alarm goes off, that means it needs some labor. Because then your process is more predictable, you've got less downtime, and your customers are happier. We can afford to do things that way, which is great.

Holden: You selected copper ammonium sulfate etchant over the traditional ammonium chloride. Was that specific or simply because that was what was recommended?

Stepinski: This process came from a European company that built a number of these types of machines. They relocated to China, and we purchased from them. As received, the equipment was not what you see today. There were a lot more peripherals, and we did a lot of development work on the tool, and arrived at the current process. As received it did not have fume recycling, and the rinse recycling wasn't effective. We

Figure 6: One of seven Whelen-made sirens used to alert employees that a process needs manual attention.

added fume recycling and rinse recycling to the system, and made it a totally closed loop; there's no connection to the scrubber or anything.

Holden: Is that etchant made of basic chemicals or is it proprietary?

Stepinski: No, we mix it. It came with proprietary chemicals, and we now use our own formulation. We run 75 grams per liter copper and two grams per liter ammonium phosphate, with a pH around 8.6. The galvanic process liberates ammonium and oxygen, which we then reintroduce into the system with the Venturi to regenerate it. One of the keys to the system is the etching goes through a cascade mechanism and gets the Venturi action, and it sits through that, it goes through this cascade for about four minutes. In that time, we're able to regenerate all the copper one (Cu^{+}) to copper two (Cu^{++}), and then return it to the etchant, to the spray bars.

We never spray with any copper one; it's always regenerated. The etch rate is much more consistent in this case. We're not doing any reaction in the chamber itself. It's in a hermetically sealed offline tank, and we do not reintroduce the etchant until all the copper one is gone, because the copper one is a poison and changes the etch rate. Our etch rate is always the same.

Goldman: You basically have the same bath in there that you've had from the very beginning. But you must have some dragout?

Stepinski: No, the dragout is all returned to the etcher.

Holden: If you do a mass balance, and you're introducing copper from copper foil, you have to take copper out somewhere.

Goldman: I was thinking of just a solution dragout at the end, but with the rinsing…

Stepinski: One of the differences with our system is that with a typical ammonium etch system they run a much higher copper content. This causes other problems; now the solution is at the saturation limit. When you introduce a little bit of water in there, you cause a lot of problems, you start making sludge. The fun thing about our process is we run at a little less than half the normal concentration. We've adjusted the other components to balance that. Etch factors are good; we're 5:1 plus for etch factors.

Because the salt content is so low—we manage the total salt content—we say the maximum total salt content is 200 grams/liter. That's everything, anions, cations, everything—we can take a water hose and just put it right into the etcher. Our rinses cascade back into the etcher.

Holden: Your first rinse is probably the replenisher, isn't it?

Stepinski: No, we just have a cascade rinse. In fact, it doesn't go back into the etcher directly; the rinse cascade goes into a little holding tank, which gets metered into the galvanic cell where we have a very high ammonia content, and that's able to absorb it all. That's how we balance. The air fumes are balanced, the negative pressure that we generate from the Venturi above the solution level, we connected the front of the entry to that. So, we're able to locally remove the fumes from the atmosphere right around the machine. You don't smell any ammonia fumes even though we walked by the etcher and it was fully on, everything was on. You don't really smell anything.

There's enough suction there just from the Venturi, which isn't even connected, nothing's connected to a fume scrubber. It's just local

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pressure. We have a local under-pressure, and we have over-pressure in other areas to compensate. Everything balances.

Holden: That's the one process I don't find in North America, this ammonium sulfate one. But also this one is tied up in a very rigorous closed-loop system, and that is highly unusual.

Goldman: How long did it take you to get that to balance?

Stepinski: Six months. It was one of the longest items, because the process was brought to us by a supplier, and we relied on the supplier a lot initially to get it set up, and then when it didn't meet my expectations we had to go and really dig into it ourselves. We changed everything and ended up where we are now. Half the equipment is not even there anymore. It was highly overengineered and overcomplicated, and simple is the way to go.

Holden: That's one area I'd like to look at, the chemical dosing or chemical control stations.

Stepinski: Yeah, you can't even really see it. It's so simple. You can see it, but there's nothing much to see. We have a specific gravity controller on the galvanic cell, and one on what we call the complexer, with the cascade inside, which oxidizes. This is all specific gravity based, but it's just a huge, long tube.

Holden: Most of them are controlled by specific gravity, which you could really throw away because the specific gravity controllers are absolutely terrible.

Stepinski: Terrible. I agree. We made all our own specific gravity controllers. We just use a densitometer. We put a pressure transducer on the bottom of a tall pipe. The taller the pipe, the more sensitive it is.

Holden: That's the differential pressure (DP) method. Most of the guys that sell these things with the chemical use a hydrometer or something like that, and if you break a beam or close a microswitch…

Stepinski: Any turbulence causes a lot of problems.

Holden: Yeah, they bounce around and things like that. It's better if you have a totally sealed one where that center mass never changes but you can change the calibration. It's an interesting set of equations and debate between remembering what Archimedes' principle really says. Most of them work off the changing volume, and that is the displaced mass can change, because it floats up and down, but if it's totally immersed then that mass isn't going to change. Or it works off a little titanium chain, and as it goes up and down, it changes the weight rather than changing the volume. There's a radiation-based densitometer and there's differential pressure-based specific gravity controllers. Are there any other etchers or pre-etches in the line?

Stepinski: The only pre-etches are associated with final finish, so HASL pre-clean or ENIG pre-clean, and then we have an alternative oxide process we use prior to solder mask, which also does double duty as our multilayer treatment.

Goldman: I was going to say, your innerlayers must get some oxide treatment.

Stepinski: We have one process for both.

Goldman: In the very beginning, you've got copper coming in. You have to clean that. Is that a microetch up there on your laminate copper?

Stepinski: No, we deburr it—mechanical deburr right now for double-sided products. For cores, we don't clean it; we go straight into inkjet.

Holden: The inkjet has much better adhesion. Although, changing current density or pulsing in the panel plate for the inkjet, how is that compared with the innerlayer inkjet?

Stepinski: The unannealed grain structure and annealed grain structure are very different things. We're going with an unannealed copper on all the electroplated stuff, because we're going too fast, we're not giving it time to anneal. It's a very different grain structure than what we get out of a box that's fully annealed. The crystal structure is very different.

Holden: In one of your talks, you said the process time is 105 minutes from load to unload.

Stepinski: The whole factory takes four and a half hours to go around, but it is 105 minutes to get from plate through etch.

Holden: I have been comaparing 105 minutes to the typical four weeks, which is the conventional way with all the queues and the movements and things like that.

Goldman: I think the conventional way, plate through etch, from the beginning of a design, taking a panel, putting it in at the very beginning of the core drill to the exit, completed parts, is four and a half hours. That's what you should compare to your four weeks. Although, some companies have a special prototype line or area and prototype engineers whose job it is to speed fast-turn jobs through shop. Comparing single-sided versus the double-sided, the single-sided turnaround must be shorter.

Stepinski: Not much. You just don't have to drill and you don't plate it. If you measure the cycle time starting at plate, all you're getting rid of is plating steps, and that saves an hour total. It's three and a half hours I guess, something like that.

Goldman: If a designer comes to you with a prototype design and plops it on there, in less than half a day he's got his board to test. That's pretty good.

Holden: You could have a lot size of one, so you could do one panel, which would be the prototype if he wants one or two boards.

Goldman: Or, if he's not here, he zaps over all the information, and you could have his panel on his desk the following morning at the latest if he's not local.

Stepinski: Sure, and we've done that.

Holden: One of the global strategic goals we had at HP was from bill of materials and schematic to an assembled, tested prototype in five working days. In other words, we'd take two days to design the board, two days to fabricate the board, and one day to assemble and test it. You give us a schematic and a bill of materials, and five days later we'll hand you a finished, assembled prototype. We got down to five and a half days, versus 12 or 16 weeks for everybody else.

That comes through a lot of automation and a lot of standardization. Somebody was telling me, "It takes three weeks to get a solder paste stencil." I said, "We don't use solder paste stencils. We apply the solder while the board is still in the panel form, clean it, and then calendar it, and the solder paste is on the board when we ship it to the assembly guy. They don't do any solder pasting, they just apply flux and put down the part."


Figure 7: Schmoll Maschinen drill machines.

Goldman: Of course, now you can inkjet that solder paste, and the stencil guys ought to be worried.

Holden: One of the things that we found, even 40 years ago, when HP was doing 150 GHz test equipment was that we would monitor not just the thickness but the dielectric constant of incoming laminate.

Stepinski: That is the only thing that we're not checking, but we probably will down the road.

Holden: Well, Alex, our time is up. Thank you for all the time you have spent with us. Thanks for the update and for answering our questions about your most intriguing facility.

Goldman: Yes, it has been a pleasure and a privilege to visit Whelen. PCB

Supply Lines Highlights

[Isola Group Names Industry Veteran Michael White as Chief Revenue Officer]

Isola Group has named industry veteran Michael White to the newly created position of chief revenue officer. White has over 30 years of global high-tech industry experience. Prior to joining Isola, he was SVP of Sales and Marketing at Transphorm, a leader in the high-power, high-efficiency semiconductor market.

Mentor Introduces Unique Valor NPI Automated Technology Solution to Ease PCB DFM

Mentor, a Siemens business, today announced the unique Valor NPI [New Product Introduction] design-for-manufacturing (DFM) technology that automates printed circuit board (PCB) design reviews based on the PCB technology and manufacturing processes employed.

Sunstone Upgrades Capabilities by Adding New Orbotech LDI

Sunstone Circuits has just announced the addition of the Paragon-9800, the latest in laser direct imaging equipment from Orbotech, to its Oregon manufacturing facility.

Park Electrochemical Introduces M-Ply, the Newest Member of the Meteorwave Family

Park Electrochemical Corp. announced the introduction of M-Ply, a prepreg designed specifically for radio frequency (RF)/digital hybrid bonding. M-ply is the newest member of the Meteorwave family of materials, as well as the newest addition to Park's line of very low-loss and ultra-low-loss electronic materials.

Zuken Improves Team Communication and High-Speed Design Support with CADSTAR 18

The latest version of its CADSTAR desktop PCB design software also supports industry requirements for high-speed design, and includes across-the-board performance enhancements and ease-of-use features. One highlight is developments in the industry-leading Activ-45 router—making the routing experience even more intuitive and powerful, and giving users more control over their designs.

Ventec International Materials Certified to Latest IPC-4101 Revision E

Further to the latest release of the IPC-4101 revision E, Ventec International Group announces that as of 1st July 2017, all related products are certified and released to the IPC-4101E standard.

Camtek to Sell PCB Business for $35 Million

Camtek Ltd has signed a definitive agreement with an affiliate of Principle Capital, a Shanghai-based private-equity fund, to sell its PCB business for $35 million, of which $32 million will be paid in cash upon closing and an additional amount of up to $3 million conditioned upon the PCB business' financial performance in 2018.

IEC Announces New Sales Director, ITEQ Laminate Products for North America

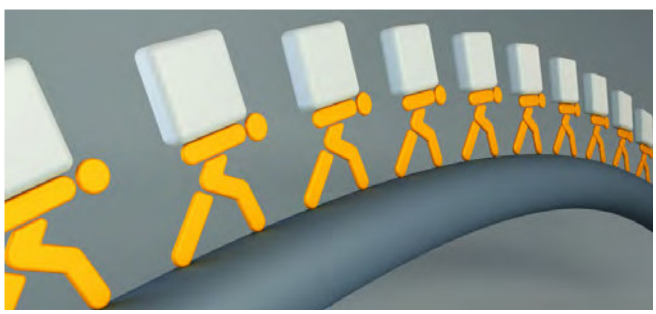
International Electronic Components Inc. is pleased to announce that Mike Muck has joined IEC as the Sales Director, ITEQ laminate products for North America.

ITEQ Launches IT-988G

ITEQ Corp. has launched its next generation halogen-free low-loss product for ultrahigh-speed signal transmission.

Lenthor Engineering Invests in Hakuto's Mach630NP Next-Gen Dry Film Laminator

Lenthor Engineering, a California-based designer, manufacturer, and assembler of flex and rigid-flex printed circuit boards, has invested in Hakuto's Mach630NP next-gen dry film laminator from Matrix USA.



Cycle Time Reduction Through W.O.R.C.

by Steve Williams
THE RIGHT APPROACH CONSULTING

Introduction

Lean, theory of constraints (ToC), quick response manufacturing (QRM), cross-training, and staticstical process control (SPC) are powerful, tried and true methodologies for process improvement. However, these tools are rooted in high-volume manufacturing environments and don't always play nice in a high-mix, low-volume (HMLV) operation. The new W.O.R.C. manufacturing strategy was specifically developed to overcome these shortcomings while capitalizing on their strengths.

Limitations of the Current Toolset

Lean is a collection of tools and methods designed to eliminate waste, reduce delays, improve performance and reduce costs. Lean focuses on eliminating non-valued added activities, as opposed to more traditional improvement efforts, which focus on reducing the time in value-added steps. The problem with lean is that many of the tools work best in a high-volume process that has very little variation in product mix.

ToC is a methodology that focuses on removing bottlenecks from a process through a series of five steps: Identify the constraint, Exploit (improve) the constraint, Subordinate (align all activities), Elevate (additional actions) and Repeat. The problem with ToC is that, by definition, eliminating one bottleneck creates another, and in a high-mix process the bottlenecks can change with the mix.

Quick Response Manufacturing (QRM) is a cell-based strategy closely related to focus factories that was developed specifically for HMLV that has been gaining popularity over the past few years. The problem with QRM is that it works best when equipment sets from several sequential departments can be physically organized into small cells. This becomes problematic in operations that have processes requiring capital-intensive environments like plating, clean room imaging, etc., where setting up a single machine in a cell is prohibitive.

Cross-training is critical to manufacturing continuity to overcome employee absences,

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specific department surges, and other unforeseen events that would compromise ongoing processes. The problem with cross training is that it is typically employed randomly, meaning that employees are cross trained based on their past experience or interest with no strategy to cross train across closely related tasks.

SPC uses statistical analysis to monitor and control processes. Once again, the problem with SPC is that it works best in a mature, high-volume process with a stable product mix. Companies tend to focus SPC on product specific attributes that change with each product, which creates challenges with processes that change part numbers multiple times daily, like in printed circuit manufacturing.

Introducing W.O.R.C.

Workflow Optimized for Rapid proCessing (W.O.R.C.) was developed by The Right Approach Consulting (TRAC) in reaction to the expressed needs and feedback from clients. It adapts the most critical elements of the current toolset to the HMLV manufacturing environment. Developed over the past three decades in the trenches with manufacturing companies all over the world, TRAC is rolling out this new manufacturing strategy specifically aligned for high-mix, low-volume companies. W.O.R.C. isn't just a production toolset; it applies to all processes from order entry through shipping. While the foundational tools and techniques are certainly not new or groundbreaking, the unique combination and adaptation to HMLV manufacturing is. TRAC has successfully implemented W.O.R.C. in several industries, and we will look at two case studies from both an office and manufacturing perspective.

W.O.R.C. Cells

There are three types of W.O.R.C. cells that can be implemented, depending on the operation, work flow, and equipment set.

Physical W.O.R.C. Cells

Certain industries like sheet metal fabrication, plastic injection molding, die-casting, etc., are custom-made for Physical W.O.R.C. cells. The key is to locate all the equipment required to perform a majority (if not all) of the operations into one physical cell. W.O.R.C. cells can be configured in a variety of ways that fit the process, product and/or workspace (horseshoe, linear, circle, etc.). The first key is to design the cell in process sequence with minimal travel and handling waste. The second key is cross training, or to be more accurate, extreme cross training. This means that every single person in the cell can perform every single task and is competent on every single piece of equipment.

Virtual W.O.R.C. Cells

Other operations like printed circuit board manufacturing require specialized equipment, process and environmental conditions that make it problematic to put a single piece of equipment in a cell. For example, multiple plating lines and imaging clean rooms can require mutually exclusive environments. It can be done, and in some cases, it does make sense to have micro-rooms for plating and imaging in a co-located cell, but typically a Virtual W.O.R.C. cell is the solution.

What is a Virtual W.O.R.C. cell? This means keeping the required equipment in the normal work areas and functional departments, but designating one dedicated piece of equipment in each area as belonging to the W.O.R.C. cell. This means, and this is the hard part for many production managers in the beginning, that only work within the W.O.R.C. cell charter can be run on these machines. That means letting them sit idle when needed. This is also hard to swallow, at first, for the financial folks that measure efficiency, ROI and productivity. We will discuss this later.

Hybrid W.O.R.C. Cells

Like many things in business, and life, a hybrid solution often provides the best of both worlds. This means setting up a Physical W.O.R.C. cell for all of the tasks and equipment that can be easily co-located together and combining them with the dedicated Virtual equipment set that do require special environmental conditions. Whenever possible, it is best if the physical cell can be located in close proximity to the virtual cell(s) to maximize the benefits.

Figure 1: The magic of cross-training.

For example, due to weight, size and special controlled environments, it would not make sense to create a cell with all the critical processes needed to build a PCB (drill/rout, plating, image, lamination). These are the cases that fit the virtual W.O.R.C. cell model—allocating a single piece of equipment in each of these critical departments specifically for W.O.R.C. jobs. Virtual cells require much more discipline than physical cells in keeping this equipment set dedicated only to W.O.R.C. jobs.

W.O.R.C. Cell Cross-Training

This is the beauty of W.O.R.C. cells, and it applies to all three models. Unlike traditional department functional silos that usually require a specialized person for each task, they can be fully operated with a minimum of highly skilled workers (Figure 1). There are two collateral benefits of this structure: 1) being both flexible and lean allows rapid adjustment to demand and mix changes, and 2) the cell is totally self-sufficient. Two key points here:

1. Managers underestimate the value of cross-training.
2. Managers overestimate the difficulty of cross-training.

Autonomous

This is another concept that takes a while for traditional production managers to accept; the W.O.R.C. cell members need to be totally autonomous, and I mean totally. They order their own raw materials and supplies, manage the member's time/hours/overtime, are responsible for equipment maintenance, and schedule the jobs through the cell. The good news is, once the managers responsible for the rest of the shop see how well this works, they embrace it 100% because it makes their job so much easier.

Myth-Busting Traditional Thinking

Traditional Thinking

- Everyone will have to work faster, harder and longer hours to get jobs done in less time
- To get jobs out fast, we must keep our machines and people busy all the time
- To reduce our lead-times, we must improve our efficiencies and utilization
- Installing a Material Requirements Planning (MRP) System (or ERP) will help in reducing lead-times
- Since long lead-time items need to be ordered in large quantities, we should negotiate quantity discounts with our suppliers
- We should encourage customers to buy our products in large quantities by offering price breaks and quantity discounts
- We can reduce lead-times by forming teams in each department
- The reason for reducing lead-times is so that we can charge our customers more for reduced lead-time jobs

W.O.R.C. Cell Thinking

This will be the part that challenges your financial folks to think outside of the proverbial box and move outside of their comfort zone, financially speaking. It will mean moving past everything they learned in business school and have been applying throughout their business careers. However, the good ones with open minds will usually see the wisdom in W.O.R.C. cell thinking where it is appropriate in their operations. This will require them to also apply a hybrid approach as the traditional financial metrics will still be appropriate for the traditional production shop processes.

Strategically Plan for Spare Capacity

Traditional Thinking says: "To get jobs out fast, we must maintain a high utilization rate on our machines and people."

This is false: as utilization approaches 100% queues get longer and longer. Let me put this into a personal perspective: looking at Figure 2, in your daily commute to work, would you rather be driving on a freeway that is at 100% capacity (bumper-to-bumper traffic), or one that is only at 70% (65 mph)? We are talking about speed and time, and why would we want anything less in our businesses?

Reduce Utilization (Increase Spare Capacity)

This is not accomplished by adding more resources, but rather by reducing:

- Setup times
- Operation times
- Rework and/or scrap
- Finished goods inventory
- Machine down times
- Absenteeism

"Plan for a 70 – 85% capacity utilization sweet spot and avoid the temptation to fill up the spare capacity with more work!!!"

Bigger Is Not Better: Reduce Batch Sizes

Traditional Thinking says: "In order to reduce our lead times, we have to improve our efficiencies."

This is false, not because efficiency in itself is not bad, but because most measures of efficiency work counter to lead-time reduction. A lot size of one is the holy grail of lean operations management, but is not practical. However, smaller is better and results in improved:

- Control/traceability
- Quality levels
- Flexibility
- Risk management
  - Inventory
  - ECNs
  - Obsolescence
  - Scrap & Rework

Figure 2: Which freeway would you rather be on?

Five Simple Accounting Strategies to Support W.O.R.C.

1. Use lower overhead rates for W.O.R.C. cells
2. Assign overhead using more than just direct labor
3. Apply overhead at the time of shipment
4. Apply overhead based on critical path or other lead-times measures
5. Reassign some overhead costs specifically to large batches

Note: All the above are completely consistent with GAAP (generally accepted accounting principles)!

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Cycle Time Reduction Starts in the Office

One of the biggest "Aha" moments resulting from a TRAC comprehensive assessment is just how much lead-time is consumed by office functions (sales, order entry, engineering, and CAM). This is the fastest and easiest way to begin a W.O.R.C. implementation with a payback that begins immediately. The following case study illustrates just how much cycle time can be regained with only a small process change and the reorganization of a few cubicles.

Office Case Study: Company A

Company A is a $24 million manufacturer of custom sheet metal components serving the industrial, medical and instrumentation market sectors. Company A reported a gradual loss of market share over the past two years along with increased customer pressure to reduce their standard 4–6-week lead time to be more in line with their competition's 3–4 weeks. TRAC was contracted to perform a comprehensive "order entry to shipping" assessment and develop a cycle time reduction implementation plan.

Office Process Assessment

The assessment discovered that, on average, 2½ weeks of Company A's lead-time was being consumed by office functions: sales, order entry, CAM, engineering and purchasing. A major collateral impact of this was that production was always put in the position of having to build product in a 3–4 week timeframe. Orders flow through the office functions in a linear fashion that tended to be batch processed.

For example, each inside salesperson would wait until they had a pile of orders before moving them to the order entry folks, which was repeated through the other functional groups. Sales booked an average of six quick turn jobs per week, which became the top priority in each department, delaying every other standard production order in the queue regardless of due date. Another major cause of delay was technical questions from engineering that were filtered through sales back to the customer. Because of poor communication, it was frequently discovered that raw materials or components were not ordered in time to meet the delivery dates. Finally, every order went through the same path regardless of complexity.

The Office W.O.R.C. Cell Solution

The first step was to analyze the type of orders coming into sales based on the production steps required to build them. The results showed that roughly 25% of all orders only went through about 55% of the process steps with the balance requiring most of the steps. A designator was set up in the ERP system to differentiate between these two categories, using "L" for low complexity orders and "H" for high complexity.

The next step was to set up an Office W.O.R.C. cell (Figure 3), which physically located a person in the cell from sales, engineering/CAM, purchasing, scheduling, manufacturing, and quality. The key is to have these functions in an open, collaborative work cell where communication is instant, engineering can hear and participate with sales on technical discussions with customers, and drawings can be reviewed with all the major stakeholders at the same time.

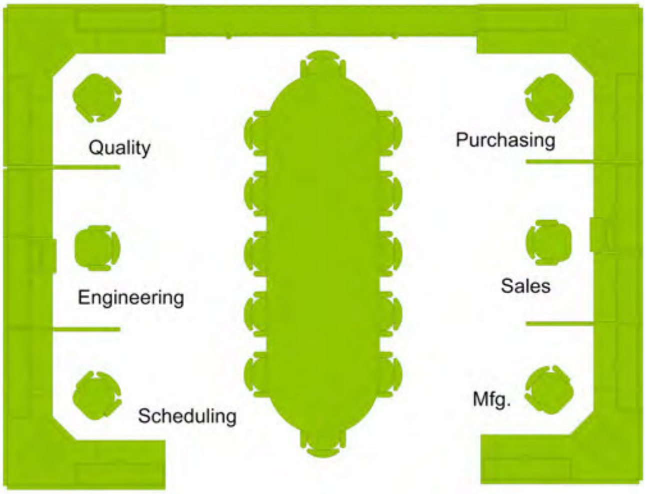

Figure 3: Office W.O.R.C. cell.

The final step was to route all "L" jobs and "Q" (quick turn) jobs through the Office W.O.R.C. Cell. It is critical that the type of jobs designed for the cell is of sufficient volume to sustain the cell; if not, the scope should be expanded. The key here is that the personnel in the cell are dedicated to only "L" and "Q" jobs with any downtime being spent cross training in the other cell functions to handle surges.

Results

The results were significant; cycle times on "L" & "Q" jobs through the "office" were reduced from 12.5 days to 3 days, giving production an extra 9.5 days to actually build the product! Because these orders were no longer running through the standard office path, a collateral cycle time reduction benefit was also realized on "H" jobs.

Collateral Benefits

The proximity of the cell structure dramatically improved communication between all members, in real time. A byproduct was assimilation by the group of conversations between one person and a customer or employee, which created some synergy and team problem-solving that wouldn't have existed before.

Manufacturing Case Study: Company B

Company B is a $17 million manufacturer of printed circuit boards serving the commercial, medical, telecom and military/aerospace market sectors. Company B reported a stagnation of improvement in on-time delivery over the past four years and has been unable to meet customer expectations for 95% or greater delivery service level. TRAC was contracted to perform a comprehensive business process assessment and develop a cycle time reduction implementation plan.

Routing Analysis

The first step was to perform a Routing Analysis to determine the mix of Company B's product, technology and processes. This critical first step would drive the direction for which of these three make the most sense to evaluate configuring dedicated W.O.R.C. Cells. The results will typically point to one of the three, however, a combination of more than one may also make sense. Depending on how many part numbers a shop processes a day, three months of routings is usually sufficient for the analysis.

A simple spreadsheet is usually the simplest tool for this exercise, listing all the possible (major) process steps in the shop across the X-axis and Part Numbers on the Y-axis. It is important to capture the layer count, raw material and technology in the analysis. Next, the spreadsheet was to be populated with the information from the routings (aka travelers, process sheets, etc.) collected from the sample months. An excerpt of this analysis is shown in Figure 4.

Now comes the analysis part; what we are looking for is a significant percentage of the traveler routings that can be grouped into one of the following:

A. short process routing sequence
B. One particular material type
C. One particular technology

Note: A family of very similar routings/material/technology can be combined into a single group if there is no appreciable difference.

Review of the full data set revealed that 18% of the jobs processed through the shop use a standard FR-4 material set, and were 2- or 4-layer technology. This tells us a lot! We proceeded under the assumption that it makes sense to set

Routing Analysis													
P/N	Layers	Material Type	Technology	Issue Material	I/L Prep	I/L Image Subs	Laser Drill	Copper	Planarize	Lam	Drill Thru	E-Less	O/L Image
	2	STD FR4	D/S	x							x	x	x
	10	LOW LOSS	STD M/L	x	x	x				x	x	x	x
	16	HYBRID	Microvia	x	x	x	x	x	x	x	x	x	x
	4	STD FR4	STD M/L	x	x	x				x	x	x	x
	12	STD FR4	STD M/L	x	x	x	x	x	x	x	x	x	x
	4	LOW LOSS	STD M/L	x	x	x				x	x	x	x
	8	STD FR4	Microvia	x	x	x				x	x	x	x
	2	STD FR4	STD M/L	x							x	x	x
	12	TEFLON	B/B Via	x	x	x	x	x	x	x	x	x	x
	8	STD FR4	STD M/L	x	x	x				x	x	x	x
	16	STD FR4	STD M/L	x	x	x				x	x	x	x
	10	LOW LOSS	Microvia	x	x	x				x	x	x	x
	20	HYBRID	Microvia	x	x	x	x	x	x	x	x	x	x
	4	STD FR4	STD M/L	x	x	x				x	x	x	x
	12	STD FR4	Microvia	x	x	x	x	x	x	x	x	x	x
	4	LOW LOSS	STD M/L	x	x	x				x	x	x	x

Figure 4: Company B routing analysis.

up a dedicated W.O.R.C. CELL for this product/process family.

Virtual W.O.R.C. Cell Creation

A Virtual W.O.R.C. Cell was created for 2- and 4-layer standard FR-4 product by identifying a single machine in drill, image, lamination, and inspection for the W.O.R.C. Cell jobs. As a small shop, plating and soldermask were not included as there was only one machine for each of these processes. It was also determined that a standard 18" x 24" panel would be used for all W.O.R.C. Cell jobs, regardless of panel utilization guidelines. Any short-term material waste was eclipsed by the productivity and efficiency savings achieved and increased customer satisfaction from OTD performance.

The next phase was to cross-train a select group of three employees to become process experts in all four departments, so that any of them could proficiently drill, image, laminate and inspect product; in other words, they became "Super Certified Operators." The core cell was comprised of two of these employees, with the third being backup coverage for the other two. The three selected operators were already proficient in one of the processes, and with full disclosure, becoming proficient in all four processes was a 6-month process (eight weeks in each of the three unfamiliar departments).

The final phase was to create a new code in the ERP system for W.O.R.C. cell jobs, so that they would automatically get scheduled through the Virtual W.O.R.C. cell and not get mixed in with the standard jobs for the rest of the company's product.

The Results

The following baselines were established for the 12 months prior to implementing the manufacturing W.O.R.C. cell:

- On-time delivery: 89% (all jobs)
- Yield: 92% (all jobs)
- Customer Satisfaction: 6.5/10.0 (annual survey composite)
- YoY Growth: 3%

And for the 12 months post W.O.R.C cell implementation, the results were all improved by:

- On-time delivery: 98% (W.O.R.C. cell jobs)
- On-time delivery: 94% (all jobs)
- Yield: 96% (W.O.R.C. cell jobs)
- Yield: 93% (all jobs)
- Customer Satisfaction: 8.5/10.0 (annual survey composite)
- YoY Growth: 9%

Collateral Benefits

It stands to reason that the jobs now processed through the W.O.R.C. cell show an improvement in OTD, but what about the improvement in other jobs? Removing the 2- and 4-layer jobs from the standard production process freed up capacity in all departments and resulted in improved delivery across the board. The bump in yield was attributed entirely to the W.O.R.C. Cell jobs, as the three-person team totally owned product quality from start to finish.

Conclusion

Employing W.O.R.C. methodologies to apply the best of all worlds from the current tool set will improve the critical performance metrics of on-time delivery, cycle-time, lead-time and yield. This combined improvement will also result in greater customer satisfaction and new business opportunities that directly impact bottom-line profitability. Implementing W.O.R.C. takes work (pun intended), discipline and some expense, but under the right conditions, the payback can be spectacular! **PCB**

Steve Williams is the president of The Right Approach Consulting LLC. To read past columns, or to contact Williams, click here.

Happy's Essential Skills: Tip of the Month—The NIST/SEMATECH e-Handbook of Statistical Methods

In the 1990s, the National Bureau of Standards was distributing a popular statistical document, Experimental Statistics — National Bureau of Standards Handbook 91, originally written by Mary Natrella of the NBS Statistical Engineering Laboratory in 1963. A request by Patrick Spagon of the Statistical Methods Group of SEMATECH, a consortium of major U.S. semiconductor manufacturers, to update Handbook 91, led to the creation of a project team from NIST and SEMATECH to create a new web-based, statistical e-handbook including statistical software.

The goal of the NIST/SEMATECH e-Handbook of Statistical Methods (also called the Engineering Statistical Handbook), is "to help scientists and engineers incorporate statistical methods into their work as efficiently as possible," according to the website. It is intended to assist engineers and scientists in developing their own expertise, design their own experiments, and use the appropriate statistical analysis.

Numerous case studies are integrated into the text and designed to work with the statistical software, DATAPLOT, available for free download in the "Tools & Aids" section. A fill-in-the-blank worksheet with sample data allows the user to quickly and easily duplicate the calculations with his or her own data. To make the software as useful as possible, it is available for seven operating systems.

To read the entire column, which includes a download link to Handbook 91, click here.

Why is the Developer Missing at BATM Systems' Romania Facility?

by Marc Ladle
VIKING TEST LTD.

I recently had the great pleasure to be working with BATM Systems at their new factory in Romania. The process concept is the brainchild of Steve Driver. For those who don't know Steve, he is a gentleman of many years of experience in the UK printed circuit industry. Even after several decades of circuit production, he has an energy and enthusiasm for manufacturing which are most infectious!

As I walked into the BATM wet process area I had to question why the developer was missing from the set-up. The answer was straightforward enough: Because the etch resist is applied directly by "drop on demand" technology so there is no need for any dry film developer (or photoplotter, dry film laminator or UV exposure).

The clever printing technology has been supplied by a company called Mutracx, based in Holland. The machine they delivered to Romania is the Lunaris, and it can print a panel in not much more than 20 seconds, so it aligns very well to European etching and stripping speeds. It is a machine designed for fitment within the conveyorised image-etch-strip process and can be integrated into the middle of the manufacturing line very easily. The Lunaris is capable of being used for both innerlayer (print and etch) or for outer layer (pattern plate) using the same ink for both process routes. It strips in normal dry film stripping solution, although the temperature may need to be a little higher.

The high print speed, as compared to other drop on demand printers, is possible because of the multi-head print array spanning the complete width of the conveyor which allows each side of the panel to be imaged in a single movement through the print hardware. After print-

Figure 1: An employee makes adjustments to the Mutracx Lunaris machine.

ing the first side, the panel is automatically flipped over to print the second side. The flexibility of being able to print batches of 1 or 100 with virtually no changeover times and a very steady cost-per-print is very attractive.

It also has AOI built in to check the image before it is delivered to the etch machine, so there is excellent security to make sure that there are no issues with any of the jets in the print heads for every panel that is printed.

The etch resist used on the Lunaris machine is supplied by Dow Chemical and this also has a lot of potential for wider use, as it can also be used as an electroplating resist. The nature of the resist once it has been applied to the panel is reasonably robust and it also strips easily and cleanly as long as you are able to achieve stripping temperatures of around 65°C.

The process is not currently a high-density solution. Drop-on-demand printing technology has a limitation on the resolution that can be achieved as each drop must have enough mass to travel across the air gap between the print head and the panel without drifting or distorting. This means there is some limitation on the line and space that can be achieved; 0.150 microns (6 mil) or greater is quite comfortable on this machine. This technology aligns perfectly to the target products for the BATM factory so I must say this looks like it will be an excellent machine for them to use.

I had not previously visited Romania and was not really sure what to expect. I knew the factory was brand new and most of the staff had not previously been involved in making printed circuits. I should not have worried. The Romanian people are a credit to their country. They are hard-working and very conscientious, but also very friendly and helpful towards anyone who is visiting them. I have added Romania to the list of countries that I would visit for pleasure if the opportunity presents itself. There are areas of the country which have staggering natural beauty and, compared to the UK, the cost of accommodation and food is extremely reasonable.

I am sure other companies will follow where people like Driver are leading the way. It makes good commercial sense to manufacture in a country where the labour costs are relatively low—especially in printed circuit production, where the personnel costs are a substantial proportion of the overall cost of the product. I am also sure the future looks good for Romania and the Romanian people, with many companies wanting to invest in a low-cost manufacturing base within the European union. Romania is a perfect option. As I drove south from Hungary into Romania it became obvious that some substantial electronics companies have already established factories to benefit from the favourable economic conditions. I am sure this will be a growing market for years to come.

There are quite a few associated benefits to this new print technology. Factory real estate in Europe is expensive and an opportunity to cut out so many machines in one go makes the small footprint of the Lunaris very attractive. Add in the savings in power and water use and the case gets stronger and stronger. Then there is also the saving in process time, which is a big advantage in the fast turn-around European market. It is possible to be etching the circuit literally minutes after the manufacturing data has arrived in the factory.

I have a lot of respect for people who are prepared to take a step forward and try new technology. This is only the second Lunaris machine working in a production environment and I understand the other machine is mainly printing resist for electroplating. To move our industry on, it is critical that we continue to have people like Steve who are prepared to invest in new technology.

I work for an equipment supplier but I have no commercial interest or influence with either Mutracx or BATM Systems. The equipment I have installed there is much more conventional in its nature. I am genuinely interested in their new process and will be watching closely to see how they progress.

I wish them every success. **PCB**

Marc Ladle is director at Viking Test Ltd. To contact Ladle or to read past columns, click here.

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Electronics Industry News
Market Highlights

New Fast-Charging Flow Battery Aims to Advance the State-of-the-Art in Energy Storage

Masdar Institute researchers have engineered a novel non-aqueous low-cost flow battery equipped with fast-charging that is able to charge itself in half the time it would normally take, which they believe may enable cheaper and more efficient large-scale renewable energy storage.

Dell Helps Future Proof Customers Globally with Internet of Things Technology

Dell Inc. is helping new customers across the globe, as well as its own manufacturing facilities, to future proof their businesses through embracing IoT technology.

Convergence of Blockchain with Emerging Technologies Set to Disrupt the Healthcare Industry by 2025

In the next five to 10 years, a blockchain ecosystem with healthcare-focused use cases involving health data exchanges, smart assets management, insurance and payment solutions, blockchain platform providers, and consortiums will emerge.

5G Wireless and Beyond: From Evolution to Revolution

From a technical standpoint, fifth generation mobile wireless—or 5G, as it's commonly known—is more about "evolution" than "revolution." In many ways, 5G simply builds upon the mobile infrastructure established by the current wireless standard, 4G LTE. From the standpoint of the imagination, however, 5G is poised to reshape the technological world as we know it.

New Design Improves Performance of Flexible Wearable Electronics

In a proof-of-concept study, North Carolina State University engineers have designed a flexible thermoelectric energy harvester that has the potential to rival the effectiveness of existing power wearable electronic devices using body heat as the only source of energy.

Building with Robots and 3D Printer

At the Empa and Eawag NEST building in Dübendorf, eight ETH Zurich professors are collaborating with business partners to build the three-story DFAB HOUSE. It is the first house in the world to be designed, planned and built using predominantly digital processes.

Global Healthcare M2M Market: Demand for Remote Patient Monitoring to Bolster Uptake

Some of the leading players operating in the healthcare M2M (machine-to-machine) market are Telefonica S.A., AT&T Inc., Vodafone Group plc, and GE Healthcare.

A.I. Will Prepare Robots for the Unknown

"The goal is for A.I. to be more like a smart assistant collaborating with the scientist and less like programming assembly code," said Chien, a senior research scientist on autonomous space systems. "It allows scientists to focus on the 'thinking' things—analyzing and interpreting data—while robotic explorers search out features of interest."

Artificial Intelligence and Analytics Accelerate the Pace of Digital Workplace Transformation

New research that examined how organizations are evolving from a traditional office environment to a digital workplace reveals that gaining competitive advantage and improving business processes are among the top goals of their digital transformation strategy.

3D Printing Market worth $32.78 Billion by 2023

The 3D printing market is expected to be worth US$32.78 billion by 2023, at a CAGR of 25.76% between 2017 and 2023. The growth is attributed to the factors such as the ease of development of customized products, ability to reduce overall manufacturing costs, and government investments in the 3D printing projects for the development and deployment of the technology.

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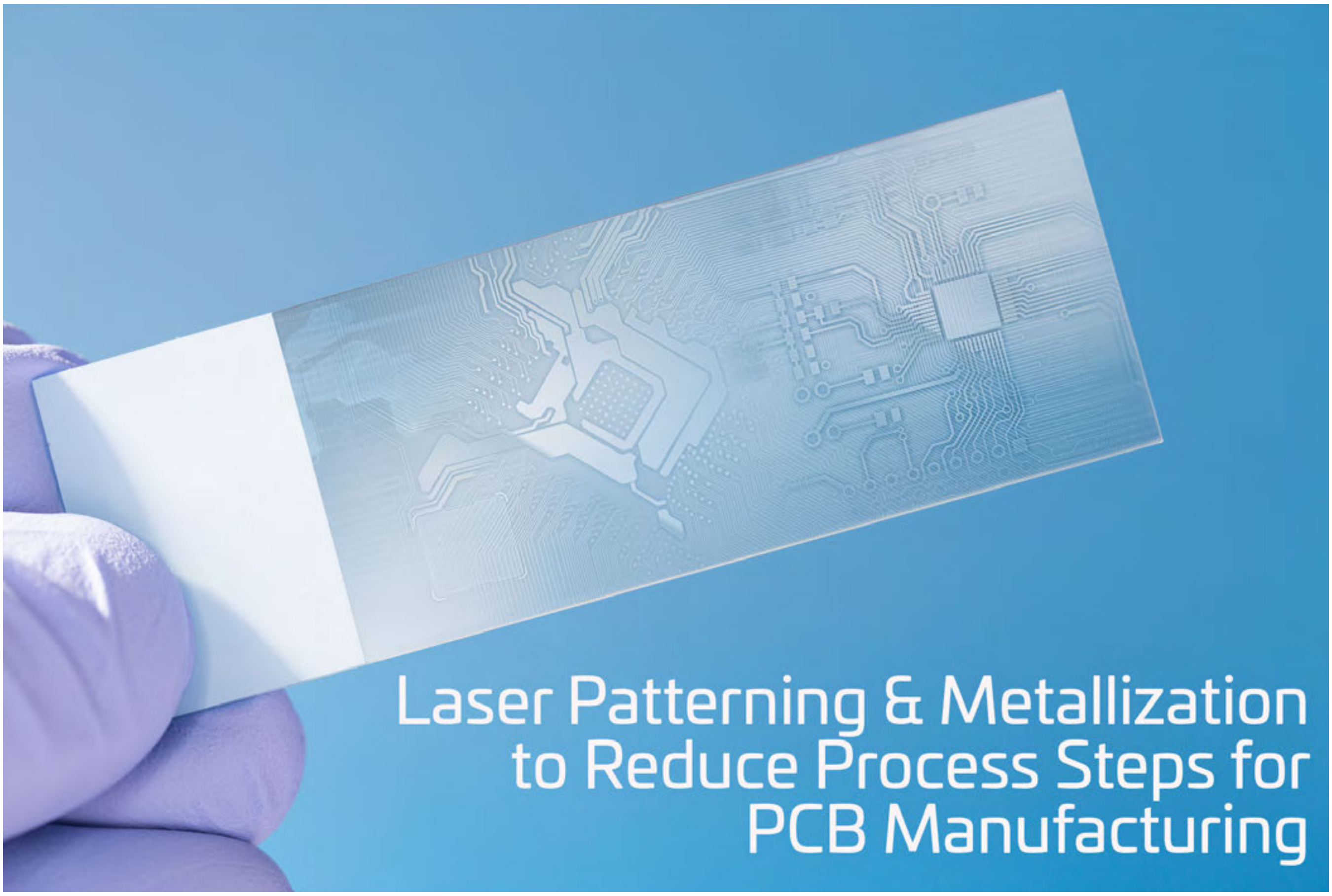


Laser Patterning & Metallization to Reduce Process Steps for PCB Manufacturing

by Joel Schrauben, Cameron Tribe, Christopher Ryder and Jan Kleinert
ELECTRO SCIENTIFIC INDUSTRIES

Abstract

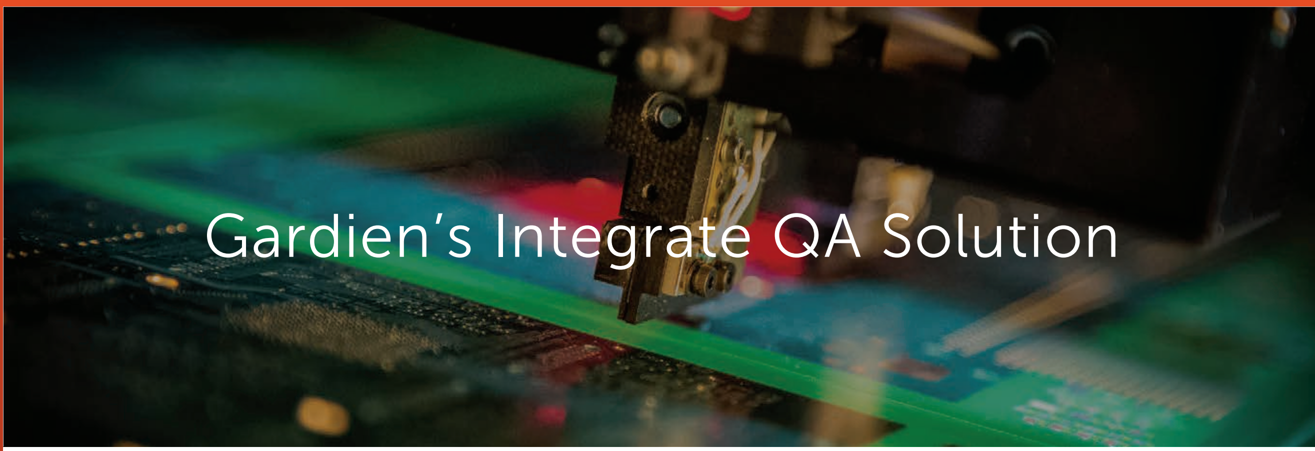
Glass offers a number of advantages as a dielectric material, such as a low coefficient of thermal expansion (CTE), high dimensional stability, high thermal conductivity and suitable dielectric constant. These properties make glass an ideal candidate for, among other things, package substrate and high-frequency PCB applications. We report here a novel process for the production of printed circuit boards and integrated circuit packaging using glass as both a dielectric medium and a platform for wiring simultaneously.

An ultrafast laser is used to etch away the desired pattern (pads, wires and vias) in the glass, and copper plating is "seeded" through the laser-based deposition of copper droplets. The seeded area is then plated using electroless plating followed by electroplating. Demonstrations of fine pitch wires, variable diameter through holes and blind vias, and a multilayer stack are shown. The deposits have a resistivity less than a factor of 1.5x that of bulk copper for 5-10 mm wires. Plated lines in borosilicate glass of 7-10 µm width and 5-20 µm depth and line spacing down to ~10 µm are demonstrated, as well as vias with a top diameter approaching 100 µm for 150 µm glass and 40 µm for 50 µm glass.

The process presents the potential for significant material savings in terms of base materials, process chemicals, and waste disposal/recycling costs (glass is on the order of 100-fold less expensive than some current high-frequency dielectrics, and wet processes account for a large part of standard PCB/substrate manufacturing). Additionally, the processes are amenable toward other dielectric materials such as FR-4, polyimide and PTFE-based materials.

Introduction

Increased demand for high data transmission rates is driving the development of smaller PCB features. Electrical circuits are reaching the physical limitations of traditional PCB dielectric materials under which electromagnetic compatibility can be controlled. Additionally, Gardien



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a high density of features, such as in advanced flip chip packages, require substrates with low CTE, high dimensional stability, high thermal conductivity and suitable dielectric constant. Glass offers a number of advantages in this regard[1], including that it is very stable in terms of electrical properties, moisture absorption, and aging, and has a CTE similar to that of silicon, making it ideal for IC packaging. Furthermore, the dielectric constant of glass is, in some instances, lower than that of FR-4. This, coupled with a low loss tangent, and low materials cost compared to high-performance materials, make glass suitable for high-frequency applications.

Many different approaches have been taken toward the realization of conductive plating of glass substrates, including: chemical vapor deposition, evaporation and sputtering[2,3]; chemical, mechanical, and laser roughening to improve electro- and electroless plating, laser direct-write techniques (vide infra), including sintering of metallic powders[4]; and using self-assembled monolayers to better adsorb catalysts for electroless plating[1]. Difficulties with glass metallization arise from chemical and mechanical incompatibilities between brittle, stiff glass and the metal, such as CTE incompatibility and strong interfacial stresses. Smooth glass surfaces present no possibility of mechanical interlocking, so metal films can easily separate from the substrate.

We report here a novel method for metallization of glass dielectrics involving laser-induced forward transfer (LIFT) of metallic foils to seed electroless plating, thereby forming strongly anchored conductive patterns. The specific techniques examined here allow for plating of conductive traces and vias, multilayer all-glass structures, and multilayer mixed-material structures. In LIFT, the desired material for deposition is adhered to a transparent carrier; this substrate is referred to as the "donor." A laser is focused through the transparent carrier layer of the donor onto the material, resulting in transfer of the material to a "receiving" substrate.

The LIFT technique applied to conductive metals was first described in 1986 by Bohandy et al., for the forward transfer of copper onto silica substrates using an ArF excimer laser[5] and has since been applied to deposit a variety of materials onto many different substrates[6,7], including organic and biological materials[8]. Printing of conductive inks and nanopastes has been a focus of recent research in LIFT applications[9]. Techniques that utilize conductive inks offer the promise of a high degree of shape and size control for the deposited material (for example, using spatial light modulators), but the inks themselves have conductivities several orders of magnitude less than their bulk counterparts, some of which can be mitigated through in situ laser curing of the deposited ink[10].

LIFT has also been used for preparing embedded components, by direct-writing conductive inks to make connections between already embedded components[11], or by using LIFT to place the components themselves[12,13]. Copper beams can be laser cut, bent, and deposited using LIFT, but require conductive glues for adhesion[14]. Most similar to the technique described in this report is an approach that uses LIFT to deposit palladium droplets[15], in which excimer lasers were used to decompose a palladium acetate film on a transparent substrate to palladium particles and deposit them on quartz, ceramic, and polymer substrates. The palladium droplets can act as catalysts for the plating of copper, nickel, and gold. This approach is limited by the low abundance, and correspondingly high cost, of palladium (around $650 per ounce at the time of writing).

Plating on Glass

The seeding methods described below can be carried out on flat, smooth glass substrates, but the metals plated on these surfaces lack mechanical stability and dimensional control. As a result, a typical approach requires laser ablation of the glass substrate to produce unplated features (pads, wires and vias), followed by application of the following seeding method. Laser glass ablation was carried out on a company system, employing a laser operating at 515 nm with pulse duration of 800 fs. A typical glass substrate used in this work is a microscope cover slide (either soda lime or borosilicate glass), cleaned by rinsing with methanol and wiped dry using a lens wipe, and handled only with gloved hands.

The 150 µm glass slides used in this work for the demonstrators are production borosilicate glass coverslips with low iron content. The 50 µm glass is a production alkali-free glass with a thermal expansion coefficient matching that of silicon for chip packaging applications. Typical glass ablation parameters are 1 MHz pulse repetition rate, 3 µJ/pulse and a feed rate of 500-1000 mm/s for a spot size of 12-15 µm. When operating with the focus at the top of the glass substrate, trenches can be made in borosilicate glass using these parameters that are ~ 7 µm wide and 5 µm deep in a single pass; additional passes can be employed to deepen the trench without significantly affecting the width. Narrower and shallower features can be made by lowering the pulse energy or defocusing the beam.

The same parameters can be used for producing pads and vias by utilizing a 7-µm pitch; cross-hatching the fill lines provides the best results. Vias are produced by applying the cross-hatch pattern multiple times or by using a racetrack pattern; scanning the Z range of the substrate while undertaking this process improves the shape of the via. Larger pulse energies are required as the via diameter approaches the thickness of the glass piece (i.e., the aspect ratio nears 1:1). Blind vias can be drilled using either the company system described earlier, or the company's CO_2-based microvia platform, employing a 9.3 µm CO_2 laser.

Laser seeding for electroless plating was carried out as follows. A high-power diode-pump solid state green laser operating at 30 kHz and 50-200 µJ/pulse, with ~11 ns pulse width, was focused to a 30-40 µm diameter spot onto a thin copper foil laminated onto a glass slide, melting the copper and directing the material toward the desired substrate. To prepare this donor substrate, a 4% aqueous solution of polyvinyl alcohol (PVA) was spin-coated onto a 1 mm borosilicate glass slide and the film allowed to dry for several hours to produce a uniform coating about 1 µm thick. The production foil, as received, consisted of a 10 µm copper foil bound to a 35 µm "carrier" layer of copper. The thin foil was laminated onto the PVA layer using a hot press operating near the melting point for PVA for several minutes. For this, the 10 µm copper layer was placed in contact with the PVA layer, and the carrier side is facing out. After lamination, the carrier layer can be easily peeled away leaving the thin layer adhered to the glass supporting substrate.

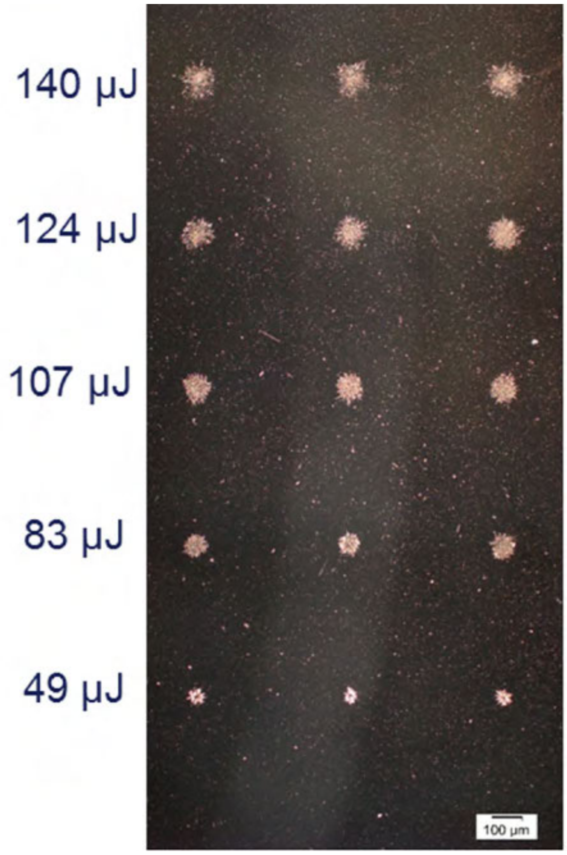

Figure 1: Copper deposits made on a smooth borosilicate glass surface using a 532 nm, 11 ns, 30 kHz Nd:YAG laser focused to a 30 µm spot on a 10 µm copper foil adhered with a 1 µm PVA layer to a 1 mm borosilicate glass slide. The pulse energy used to make each row of features is given in the figure.

Optimum laser processes utilize bite sizes (beam displacement between pulses) that are 50-75% of the focused spot diameter. Figure 1 shows deposited copper on a flat borosilicate glass surface using the method described above, with no offset between the forward transfer substrate and the receiving substrate. The process utilizes a single laser pulse with 30 µm focused spot at the work surface with variable pulse energies. The scale bar is 100 µm. The Figure shows that the method has a resolution (deposited spot diameter) of ~ 50 µm at low pulse energies; at higher pulse energies, the feature size increases. The transferred copper is strongly anchored (it passes a typical tape test), and conductive patterns can be made directly from this technique using multiple passes and/or the proper pitch, although these multiple deposits are not structurally strong on smooth glass surfaces. Figure 1 also shows that there is unbound copper dust between the anchored features. This can easily be removed by gently wiping the surface.

A company micromachining platform was utilized for copper forward transfer in instances that required precise alignment of the donor substrate. The system utilized a third-harmonic Nd:YAG laser (355 nm) with pulse repetition frequencies up to 90 kHz, pulse duration ~10 ns, ~12 µm focused beam diameter, and maximum average power of around 11 W. The same donor substrate described above can be utilized with proper laser dosing conditions, i.e., using sufficiently large bite sizes to minimize damage to the receiving substrate and sufficiently low pulse energies to maintain good resolution of the deposited copper. Other forward transfer processes that employ different lasers, process parameters (including laser wavelength, pulse duration, energy, pulse repetition rate, as well as offset of the substrates), and forward transfer substrates have been successfully implemented toward this approach and can offer seeding resolution below 10 µm. These methods are the subject of a future paper.

The copper deposits made using this technique act as seeds for the electroless plating of copper. A mismatch in resolution between the ablated features and that of the copper seeds may require polishing of the surface after forward transfer such that copper seeds only remain within the features. A second polishing step can be applied after copper plating to eliminate any unwanted connections or growth of the copper outside of the laser ablated boundaries. The entire process is shown schematically in Figure 2.

Electroless copper plating was carried out after seeding using standard recipes[16]. A typical recipe utilizes distilled water as the solvent, copper(II) sulfate pentahydrate as the copper source, potassium sodium tartrate as a chelator, and formaldehyde as a reductant. The pH of the aqueous solution is raised with sodium hydroxide to tune the reduction potentials to drive the plating reaction. The plating was carried out at room temperature in a 200 ml borosilicate glass beaker with magnetic stirring at 200 rpm. All solvents and plating chemicals used in this work were reagent grade. After a thin copper layer is deposited from the electroless plating process, copper electroplating, which offers much faster plating rates than electroless plating, can be carried out to build up thicker copper layers. After plating, polishing can be carried out to prepare a smooth surface with recessed conductive features, suitable for further layer build up. The process can be repeated, drilling blind vias instead of through-holes, to build up layers to prepare all-glass or mixed-material multilayer structures. Modified methods can be used for making structures with embedded components in all-glass structures.

The methods described above (laser ablation followed by laser forward transfer of a thin metallic foil and then plating) can also be applied to traditional and high-performance dielectric materials, as well as to the plating of various metals. Details of this work will be shared in an upcoming paper.

Resistivity measurements of the copper deposits after electroless plating were done using 4-point probe measurements. A simple design of two 1000 × 400 µm pads connected by a 5 mm or 10 mm long wire 25 µm wide was used (Figure 3, A-C). Prior to plating, the areas of the cross sections of the wires were determined using a scanning laser microscope. The resistivity is calculated according to equation 1.

$$\rho = (V*\sigma)/(I*L) \qquad \text{(eq 1)}$$

Where V is the measured voltage across the wire, σ is the cross-sectional area of the wire, I is the applied current, and L is the length of the feature.

Profile measurements were carried out on a production scanning laser microscope. Cross-sections of the engraved features were analyzed using the production analysis application. For the resistivity measurements, cross-sectional

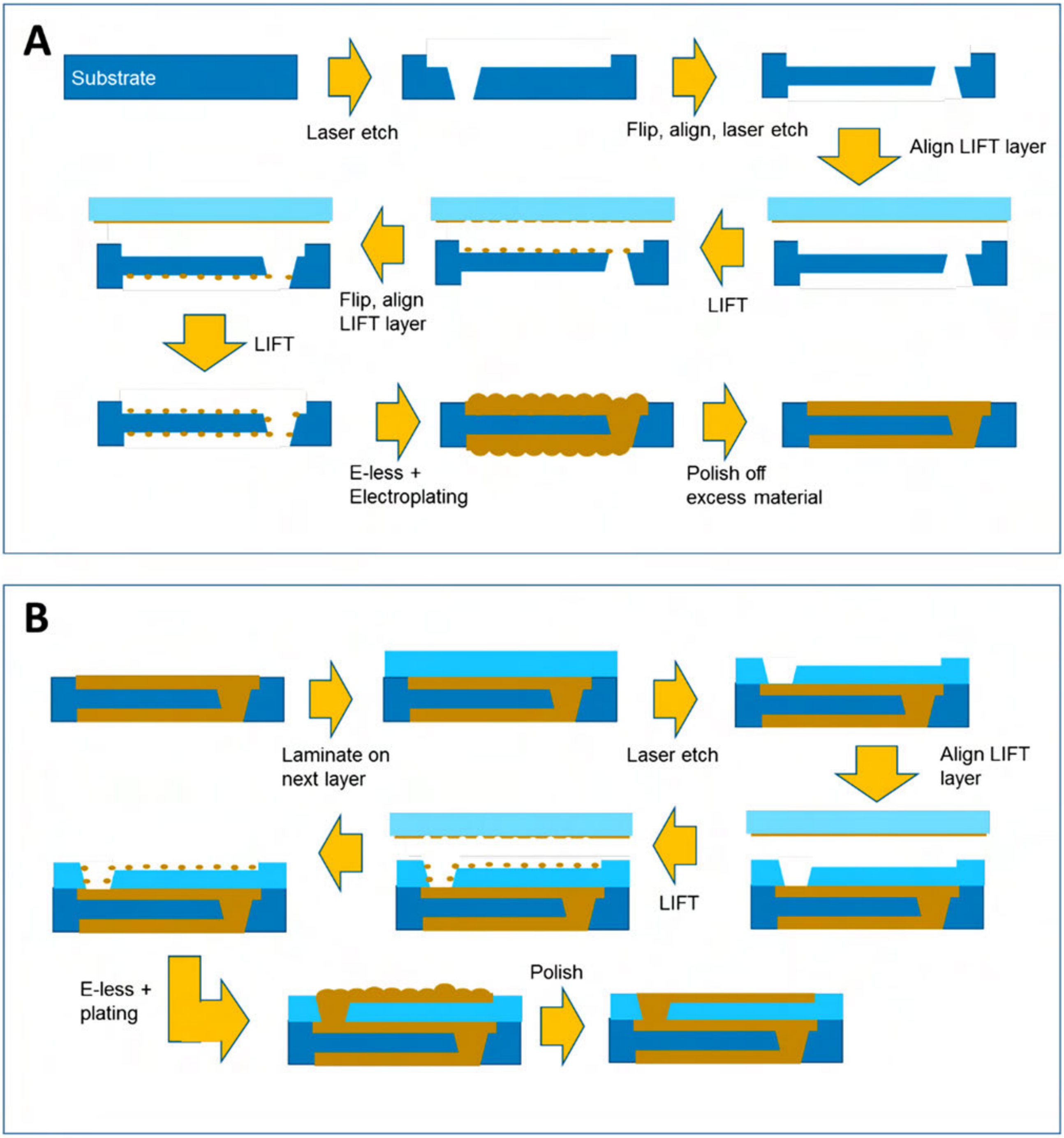

Figure 2: Glass/copper process steps for preparing (A) a two-layer structure from a single piece of dielectric material and (B) the general technique for creating multiple layers. In (A), features (wires, pads, and through holes) are made on both sides of the substrate using a laser. Copper seeds are then planted using laser forward transfer of a thin foil. The copper droplets have good adhesion to the substrate but are too dispersed to make a conductive feature. The substrate is placed in an electroless copper plating bath and copper grows on the seeds, and excess copper can be polished off to make a smooth surface suitable for further layer build up or passivation. To make multilayer architectures (B), additional layers are laminated onto the completed construct from (A), and laser etching, seeding, and plating steps are repeated.

Sample	Wire Length (mm)	Resistance Ω	Resistivity Ω·m×10^{-8}	% bulk value
1	10	0.593±0.003	2.08 ± 0.23	124
2	10	0.723±0.005	2.55 ± 0.28	152
3	5	0.284±0.003	2.01 ± 0.22	119
4	5	0.279±0.002	1.97 ± 0.22	117

Table 1. Resistivity measurements of 10 mm and 5 mm wires embedded in glass.

areas were measured at 10 different locations in the wire to obtain an average value, which is reported with ±1σ. The wires have a cross-section that is an isosceles triangle approximately 25 µm wide and 25-30 µm deep, with a measured cross-section of $3.53 \pm 0.38 \times 10^{-10}$ m^2. Four-point probe measurements employed a production DC power supply for both establishing currents from 50-200 mA across the plated features and recording the voltage drop. The reported resistivity values are the average of four measurements carried out at different applied currents for each sample to gauge the error in the resistance measurements; standard deviations of the resistance were less than 1% of the average (Table 1). The calculated resistivity values were between 1–1.5x the bulk copper value of 1.68×10^{-8} Ωm (at 20°C). Most of the error in the resistivity measurements arises from uncertainty in the wire's cross section.

A second pattern was employed for resistivity testing (Figure 3, D-E) that consisted of 5 mm lengths of wire separated by 100 µm with a total length of a 411.14 mm. The dimensions of the wire were measured at 10 different positions, yielding a width of 24.3 ± 2.2 µm, depth of 38.9

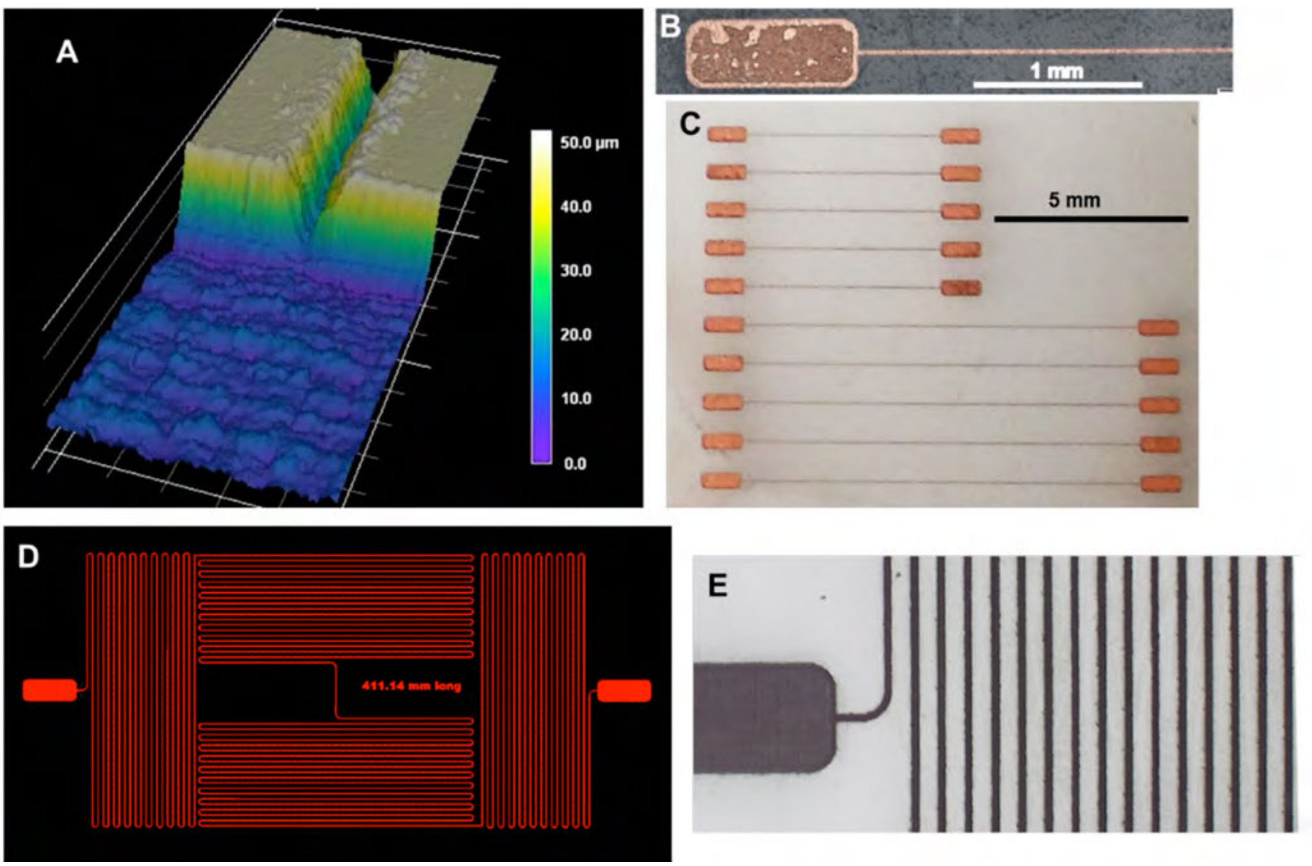

Figure 3: Resistivity measurements. A) Height measurement of the intersection of the laser-etched wire and pad. B) Optical microscope image of a plated wire and pad. C) Patterns with 5 and 10 mm long wires used for resistivity testing. D–E) Long wire pattern and detail under optical microscope after laser patterning. The pitch between the lines is 100 µm and the total length 411.14 mm.

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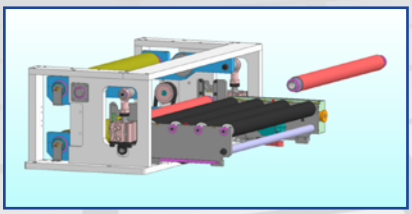

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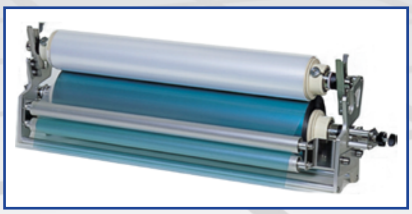
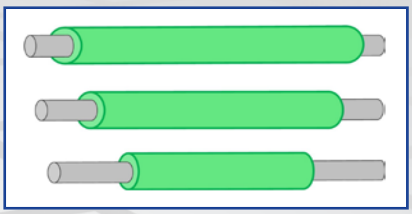


Cassette Film Load Off-line



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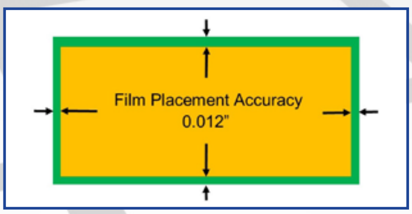

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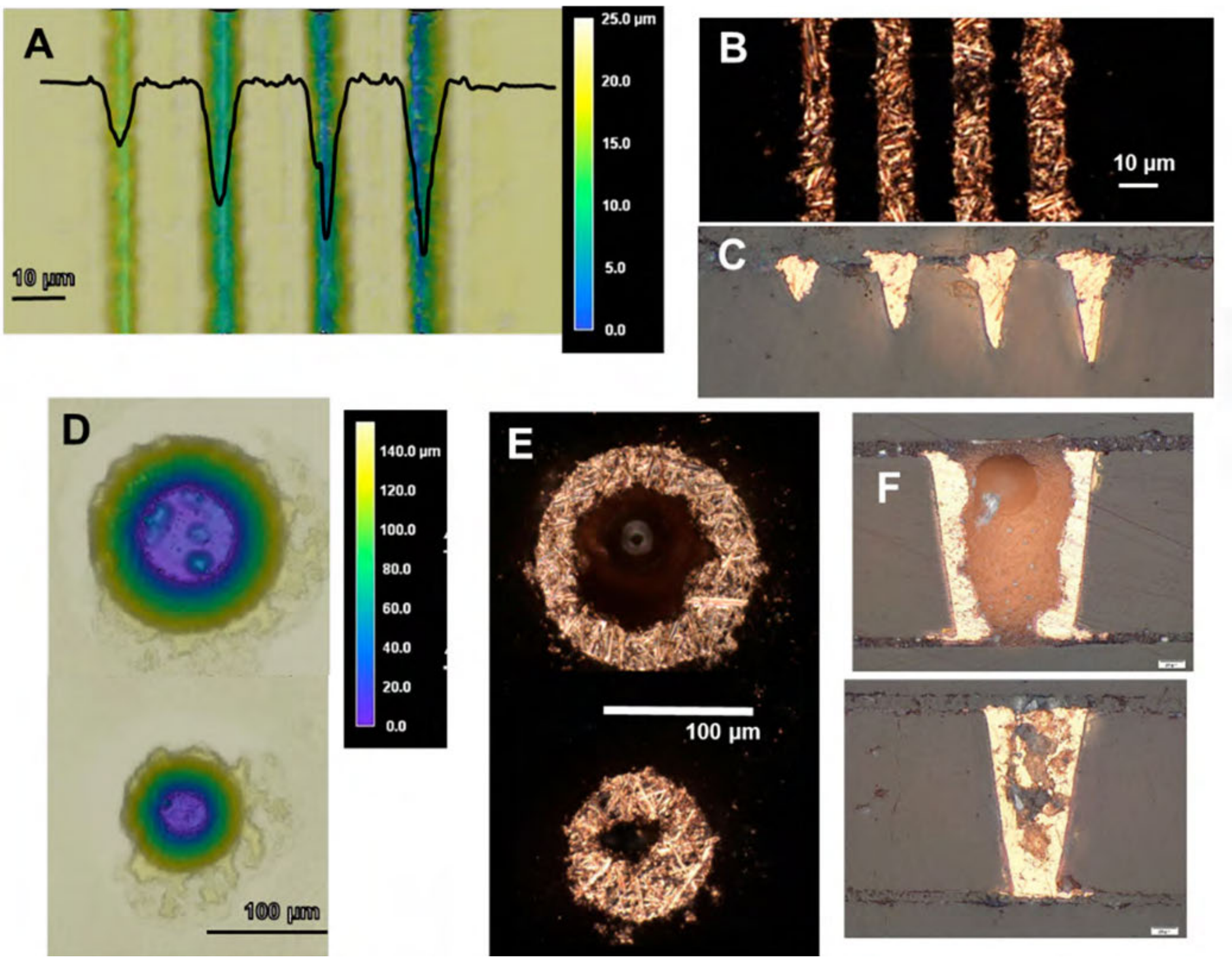

Figure 4: A–C) Fine pitch lines and variable via sizes. Trenches in the glass are made with 3 µJ, 1 MHz, 500 mm/s and 1–4 repeats of the pattern on the company system. A) Height measurements of the etched glass. B) Dark field optical microscope image of the wires. C) Cross-sections of the wires. D–F) Through-holes in 150 µm borosilicate glass with 150 and 100 µm top diameters.

± 2.9 µm and cross-sectional area of 6.08 ± 0.51 × 10^{-10} m^2. For these dimensions, a pattern consisting of bulk copper would have a resistance of 10.7 ± 0.9 Ω. Resistance measurements using a multimeter for four of these patterns gave a value of 24.1 ± 0.6 Ω, about 2.25 times the value expected for bulk copper in this geometry.

A major advantage to having wires embedded in a dielectric material is the ability to finely control the geometry of individual wires and the pitch between wires, thereby enabling a more predictable total copper volume for any given pattern. Figure 4 demonstrates wires having a very fine pitch and controllable depth. The lines are 1–4 passes using 3 µJ, 1 MHz, 500 mm/s on the company system. After one pass the trench is about 8 µm wide and 7 µm deep. The width increases somewhat upon subsequent passes, and the increase in depth saturates with the number of passes such that at the fourth pass the trench is 9.5 µm wide and 20 µm deep. The lines are separated by about 10 µm. Figure 4 also demonstrates plated through-holes of 133 and 87 µm diameter (at the laser entrance side) in 150 µm borosilicate glass. In both cases the sidewall angle is around 82°, such that at the exit the diameters are 85 µm and 41 µm, respectively. Through-holes have also been drilled in

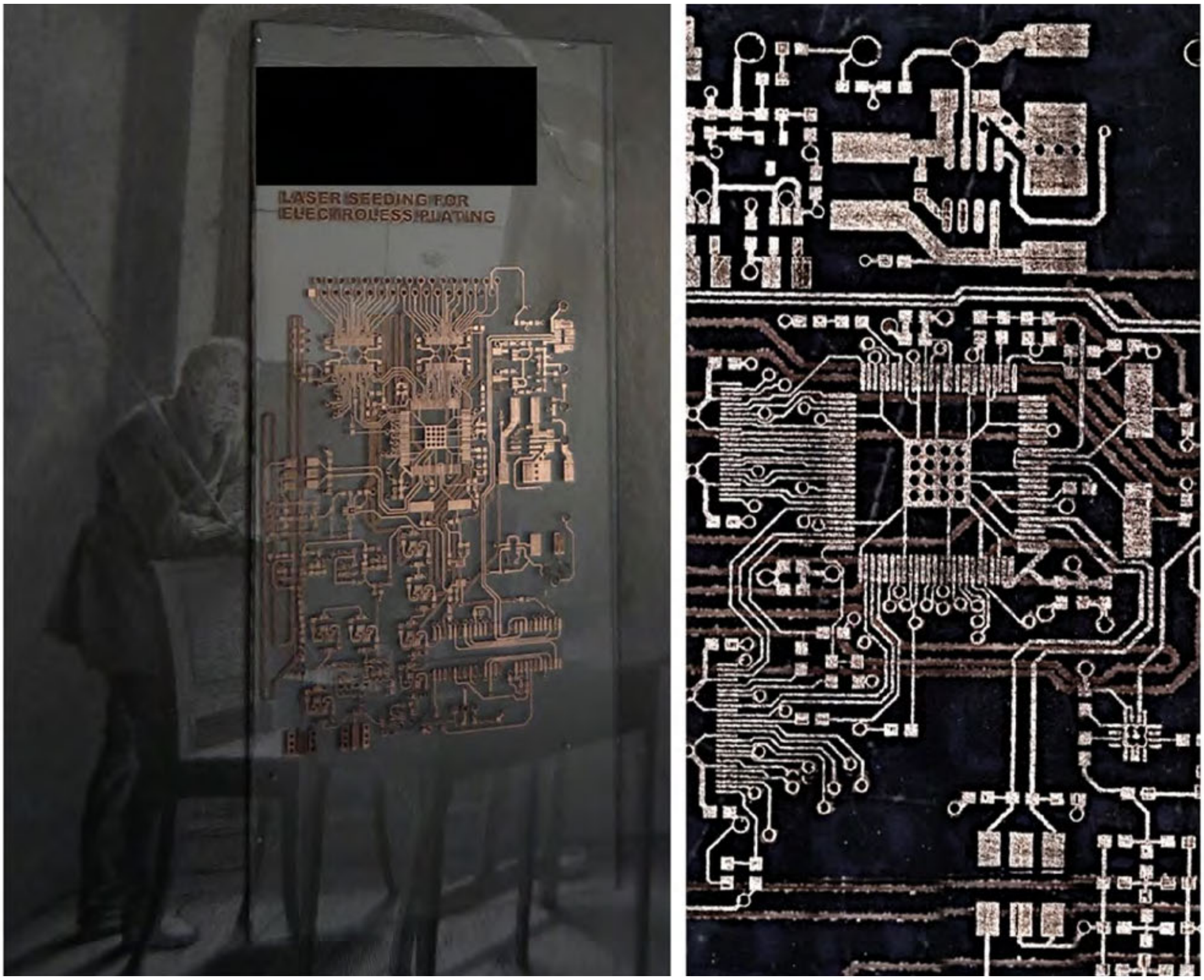

Figure 5: Images of a two-sided demo pattern on a 150 µm glass cover slip. The total pattern is approximately 20 x 35 mm and the glass is ablated using a 7 µm crosshatch pattern within the individual polygons. Left: Photo of the plated design imposed against a grayscale image. Right: Composite optical microscope image detailing a portion of the pattern.

50 µm glass with a top diameter of 40 µm and an exit diameter of 16 µm using the company system (not shown).

Applying the laser-based glass etching and copper seeding methods outlined above, a two-sided PCB pattern measuring 20 x 35 mm was prepared (Figure 5). The pattern is an actual circuit design, albeit scaled down to ~25% of the original size so that it can fit on a 22 x 50 mm borosilicate glass coverslip 150 µm thick. The smallest features in this design are ~ 35 µm wide. The pads, wires and alignment points of the design were machined using a single set of laser parameters, utilizing a 7 µm crosshatch pattern within the individual polygons. Next, the vias were drilled using a different set of parameters. The piece was flipped over and aligned using the alignment marks made on the top of the glass piece, and the wires, pads and additional text on the bottom were machined. After the forward transfer process, both the top and bottom were gently polished to remove excess copper from the surface, leaving only copper seeds in the laser machined areas. Plating was carried out in an electroless plating bath.

To illustrate the capabilities and gain insight as to whether the adhesion of copper to a glass substrate holds up to direct heat from a soldering iron, a two-layer circuit board was designed and built. This circuit, known as a "Joule Thief," operates in a similar way to a boost converter, in that it takes a smaller DC voltage and uses inductive spiking to generate a larger voltage via a transistor used for switching and a transformer. The design has three parallel circuits, which control an individual color of a common cathode RGB LED, and a resistive touch pad activates each circuit. A 1.5-volt button cell battery was used to power the circuit, and the switching frequency was measured to be approximately 400 kHz. Although the circuit itself has a relatively low parts count and does not require a two-layer PCB design, a two-layer board was designed to demonstrate the capabilities of creating plated through-holes. Trace widths on the board range from 100 µm to 400 µm (4 mils to 16 mils), which were created without issue using the methods described above.

During the assembly of the circuit board, the quality of the adhesion of copper to the glass substrate was observed to be similar to that of copper on FR-4. There were no traces or pads

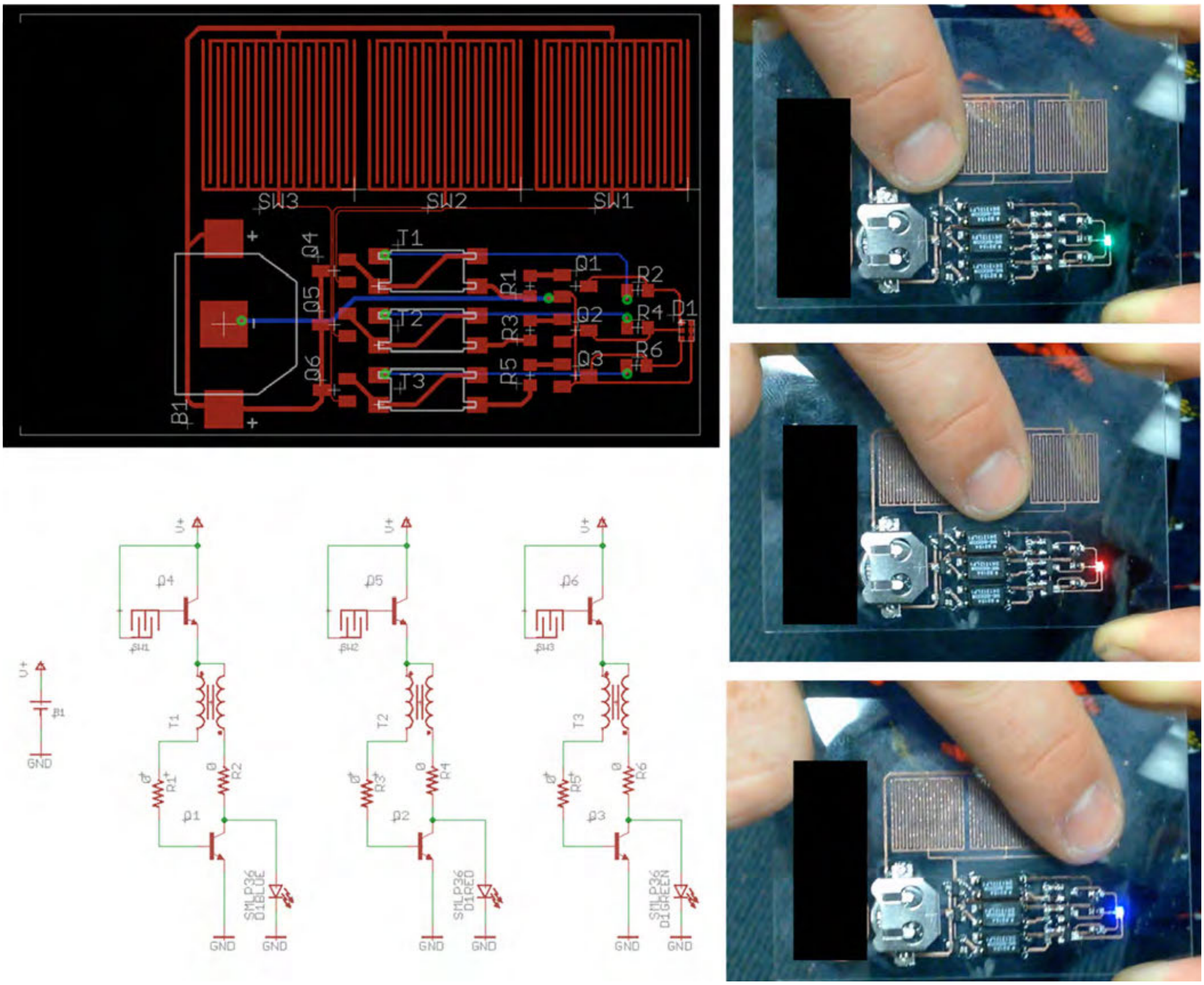

Figure 6: Resistive touchpad RGB LED demonstrator, plated on 1 mm borosilicate glass. In the upper left picture, the red features are on the front side of the board, the green circles are through-holes, and the blue features are on the back side of the board. The series of photographs shows that each touch pad activates a single LED.

that peeled off and some pads underwent multiple temperature cycles (up to approximately 300°C) with no issues. The design of the board and photographs of the completed board operating are shown in Figure 6.

Multilayer PCB architectures can be built up by aligning and gluing additional layers of glass onto plated glass layers and repeating the methods outline above. Figure 7 demonstrates drilling and plating of blind vias to build up multiple glass layers. A pattern with a 200 µm diameter pad with 50 µm diameter through-via was made in 50 µm glass using the company system operating at 1 MHz, 3-4 µJ with a feed rate of 1 m/s. The piece was then seeded and plated as described above. Optical glue was spin-coated onto a second piece of glass such that the thickness of the glue was less than 5 µm, and this piece of glass was then affixed to the plated piece. The pattern was aligned and blind vias drilled such that the glass was removed without damaging the copper pad underneath. Blind via drilling with the company system was carried out using parameters similar to those used for the through holes.

Alternatively, the high reflectivity of copper and the high absorption cross-section of glass to mid-IR wavelengths makes the company's CO_2-based microvia platform an ideal solution for blind via drilling in this application. 50 µm top diameter vias with 35 µm bottom diameter were drilled using the company system. For both blind via drilling methods the vias prepared were amendable toward forward transfer of copper and subsequent plating, as shown in Figure 7.

Comparison with Standard Practices

Besides describing a unique method for creating PCBs and IC packaging with few of the current lithographic and wet process constraints, the process described in this paper represents a facile method for the introduction of glass dielectric materials into traditional PCB fabrication lines. As an example, a multilayer board with a high-frequency glass layer could be built up by first applying the etching, seeding, and plating techniques described herein to a thin glass substrate, followed by lamination of additional glass or more traditional dielectrics onto the glass layer. The laminated layers would then be etched, drilled, and plated using typical processes. Furthermore, the method can be modified to prepare embedded components in all-glass structures.

An important point of comparison between laser seeding for electroless plating and typical PCB fabrication techniques is that, unlike typical processes, the laser seeding for electroless plating process requires no photolithography

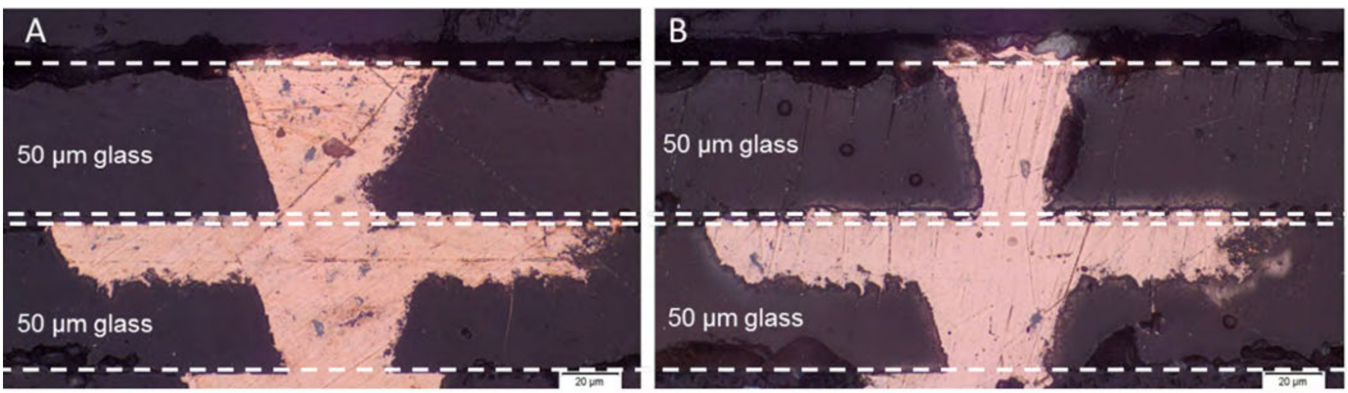

Figure 7: Blind vias and multilayer stack using 50 µm glass. The dashed lines indicate the edges of the glass pieces and middle glue layer. In both A and B, the bottom 50 µm glass was machined using a company system to prepare an embedded pad 20 µm deep and 200 µm in diameter. A through-via was then drilled from the bottom of the pad, and the piece seeded and plated using laser forward transfer followed by electroless plating. After gluing on the top 50 µm glass, blind vias were drilled using either the company 1 system (panel A), or the company's CO_2-based microvia platform (panel B).

steps, no catalyst for electroless plating, and no copper etching steps:

- Rather than undertaking photolithographic steps, the pattern of wires, pads and vias is directly etched by laser ablation into the dielectric material. The line width and spacing of the features is limited by the processing laser, process parameters, and the physics of the laser-material interaction. Rather than developing an entirely new chemical/material set for further advancing the miniaturization of PCB features, advances in laser technology, pulse shaping, and beam positioning can drive this trend.
- Tin and palladium chemistry are removed from the electroless plating process. Cleaning, conditioning, microetching, catalyst pre-dip, catalyst activation, and acceleration steps are all eliminated from the electroless plating process line. Hazardous and costly chemicals are removed from the process stream.
- There is no copper etching required. The copper that is deposited represents all the copper in that layer of the board.

It is apparent then that this process represents a "green chemistry" approach (i.e., an approach that aims to minimize both the use and disposal of hazardous materials: the best green chemistry approaches are those that avoid hazardous materials altogether). The process also presents the opportunity for substantial base material savings, with glass being up to 100-fold more affordable than current high frequency dielectrics, and energy savings through the absence of thermal lamination processes.

The best analysis would be a total life cycle analysis for an all-glass or glass core PCB to explore the process rates, throughput, and energy and material requirements for the laser seeding process compared to those of typical PCB fabrication. An effort is currently underway to make this analysis, but the biggest difference between the two processes is readily apparent: there are currently no methods in place for incorporating glass dielectrics into traditional PCB fabrication lines, and the methods described in this paper offer a pathway to make this possible.

Conclusions

This paper details a new methodology for the plating of conductive features onto glass dielectrics. A laser is used to ablate material from a glass substrate in the desired pattern, and copper is "seeded" into these features using laser-induced forward transfer of a copper foil. The copper droplets, or seeds, that are deposited act as sites for the growth of copper in electroless plating processes. Using thin borosilicate glass substrates, we demonstrated this process for the preparation of conductive thin wires, through-holes, blind vias, and multiple-layer architectures. The process can be applied toward dielectrics other than glass as well. Material costs, hazardous waste, and waste recycling streams are significantly reduced compared to traditional PCB fabrication processes. Future work will be aimed at better understanding the throughput and yield of this process, especially with comparison to typical PCB fabrication. **PCB**

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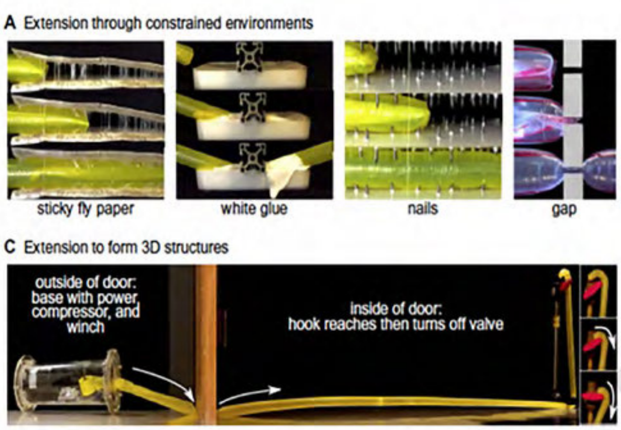
(From left to right) **Joel Schrauben** is research scientist, **Cameron Tribe** is electrical engineer, **Christopher Ryder** is director of product management, and **Jan Kleinert** is laser optics engineering manager, all with ESI.

A Robot That Grows

At first glance, robots would appear to have exactly nothing in common with sweet peas or other climbing vines. Thanks to some innovative scientists, they now share at least one trait: the ability to extend their reach.

Inspired by the growing action of plants and other living things, researchers at UC Santa Barbara and Stanford University have developed a tubular robot that navigates its environment by extending its tip and controlling its growing direction based on what it senses externally. Such a machine lends itself well to a variety of purposes in constrained environments, from clearing arterial blockages to tunneling through rubble for search and rescue operations.



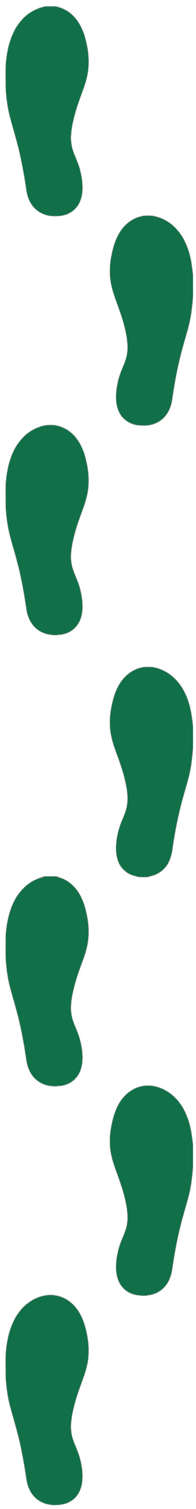
"When you think about robots today, most of them are in the world of factories," said UCSB mechanical engineer Elliot Hawkes. "But there's a big push right now to see if we can create robots that could live and help out in the human world." Robots, known for their precision and consistent, repeatable action in highly controlled spaces, are now being explored for their potential to work under variable circumstances. For instance, said Hawkes, these so-called "soft" robots may adapt their actions to the presence of obstacles (including humans) or change shape to interact in a variety of spaces. Research on this project, titled "A soft robot that navigates its environment through growth," appears in the journal Science Robotics.

No Missed Steps: 5S Methodology for a Smarter Workplace

by Todd Kolmodin
GARDIEN SERVICES USA

In today's work environment, a company should strive to produce quality product, maximize margins and reduce cost as much as possible. At times, this can be very difficult. Work ethics and methodologies of "how to do things" have developed over many years and can be deeply rooted in many manufacturing theatres. We find at times the "way we have always done it" may not be the most practical way today. This is apparent with the advances in automation, labor force reduction and shifting market demands.

Of course, automation has a role in the manufacturing world today as it has taken the task of repetitive processes that are tedious and not best suited for intelligent human interface. However, when evaluating tasks our operators and technicians perform, there is a question we should ask ourselves as managers. "Are they working hard?" In most cases we can answer "yes." However, the other real question to ask is, "Are they working smart?"



"Work Smarter, Not Harder!"

This does not mean simply read the work instructions and perform the task as written. It's much more than that. Sure, the work instructions outline the task to be performed correctly but how about efficiently? Many times, work instructions are written by process engineers and released to operators based on the engineer's knowledge of how the machine operates and how to go about making the machine produce acceptable results. That is all fine and good, but sometimes the process can be overwritten and have many extra steps that may not actually be required or can be combined to make the process more efficient. We should not try to write an operator into a corner when designing effective work instructions or processes. This also can cause issues during a process audit where operators have figured out more efficient means of carrying out the process but it is not documented.

With that in mind, let's elevate this a bit and look at efficiency from a higher altitude. When we talk about steps in the context of this column we are talking about steps in a process and steps in movement. For example: Step 1—Turn on machine; Step 2—Walk (step) to cart A and retrieve product. When an operator is at his machine or equipment, he is following steps to complete a task and most likely reset and repeat. Step 1, turning on machine, is solid. Not much we can change there. However, Step 2, walk and retrieve product, does deserve a second look.

What I'm getting at here is this: Are we sure the operator is working smart or is he working hard? We all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know we need to keep the equipment and work area clean but are we just wiping down the machine and sweeping the floor? This is where the 5S system comes in[1].

What is 5S?

5S is the name of a workplace organization method that uses a list of five Japanese words: seiri, seiton, seiso, seiketsu, and shitsuke as a guide for work space efficiency and effectiveness. The 5S discipline really gets down to the heart of working smarter and not harder. When designing a process or reviewing a workstation, it is advantageous to keep 5S in the back of your mind. Let's look at 5S in a little more detail and see how it can affect both "steps."

Seiri (Sort)

Here is where we look at the area and decide what is needed and what can be discarded. It is a good idea to take a "before" photo so it can be reviewed later. During this phase, it is a good idea to tag items that are not necessary in the area. Some use the term Red Tagging during this phase so that unneeded items stand out. These items should be removed from the work area to a holding area for review and possible disposal. What should be left are the needed items for the area.

Seiton (Systematize)

Now that we have only our needed items we need to put them in their place. Prioritize the items necessary for the task. How often is the item used? More frequently used items should be stored close to the operator to reduce "step movements." Label the storage locations. If carts or tables are required, label their locations on the floor. Also, label safety hazards or requirements.

Seiso (Sweep)

With everything now in its proper place it's time to clean! This should be a daily 10–15-minute task. Clean inside and out. Create a cleaning log sheet and empower your employees' ownership. Allow comments or problem alerts.

Seiketsu (Standardize)

Here is where we verify the effectiveness of the first three Ss. We evaluate and make sure our organization is correct. We finalize work flow diagrams, daily cleaning sheets and assign ownership for work areas. Create an audit team to periodically inspect the work areas to praise strong ethics and provide guidance for observed nonconformance.

Shitsuke (Self-Discipline)

This final "S" involves the training of personnel on the 5S discipline. When successful team members will practice the first four Ss without thinking about it and without being forced. Ownership of the workplace as if it were their own home becomes apparent once the system begins to work.

In conclusion, the focus here is maximizing throughput while minimizing the amount of effort required. Whether this means reducing or optimizing process steps and encouraging feedback by operators/employees, or reducing movement steps by optimizing workspace, tools and removing clutter. Remember, too many steps may be a missed step if a process is overwritten or a workspace is cluttered and operators/employees need to constantly make unnecessary moves or constantly hunt for missing tools.

In my daily routine, I find myself correcting myself on certain tasks by thinking of the above disciplines and quietly whisper to myself, "Todd, work smarter, not harder." **PCB**

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1. Wikipedia, 5S Methodology.

Todd Kolmodin is the vice president of quality for Gardien Services USA, and an expert in electrical test and reliability issues. To read past columns, or to contact Kolmodin, click here.

MilAero007 Highlights

First-Ever Helicopter-Based Firing of High Energy Laser

Raytheon Company and the U.S. Army Apache Program Management Office, in collaboration with U.S. Special Operations Command, recently completed a successful flight test of a high energy laser system onboard an Apache AH-64 at White Sands Missile Range, New Mexico.

All About Flex: Etchback on Type 3 and Type 4 Flexible Circuits

Through-hole etchback is a requirement that is sometimes specified on medical, military and aerospace procurement documents for multilayer flexible circuits and combination multilayer flex/rigid board circuits. It specifically relates to the copper plated through-holes and the relative dimensions between the dielectric layers and copper layers.

Mil/Aero Electronics Supply Chain Facing New Challenges

For this month's issues of I-Connect007 publications, we invited a sampling of professionals whose experience centers on the electronics industry in the military and aerospace world, including experts from design, PCB manufacturing, and the assembly arena, to sit down with us for a frank discussion. Our discussion centered on the challenges associated with military work, including the new regulatory requirements for cybersecurity, dealing with leaded vs. lead-free components, and the differences and similarities with the commercial world.

PNC Inc. Invests in LED Laser Direct Imaging system from Miva Technologies

This 2000L 2LE model is capable of imaging a maximum size 24" x 24" PC board or film size. With any large format film, positional accuracy can be a challenge but the Miva's dynamic scaling feature can increase accuracy to minimize tolerance build-ups during the imaging process.

A.I. Will Prepare Robots for the Unknown

"The goal is for A.I. to be more like a smart assistant collaborating with the scientist and less like programming assembly code," said Chien, a senior research scientist on autonomous space systems. "It allows scientists to focus on the 'thinking' things—analyzing and interpreting data—while robotic explorers search out features of interest."

American Standard Circuits Promotes Tim Hudson to Flex, Rigid-Flex and Special Products Manager

American Standard Circuits CEO Anaya Vardya has announced the promotion of industry expert Tim Hudson to the position of flex, rigid-flex and special products manager. Hudson was formerly the company's plant manager. During his 31-year career in the printed circuit board industry, he has held key positions with several companies including Midwest Printed Circuits, DEH and Bartlett.

Rockford Region Cultivates Opportunities at Paris Air Show

More than a dozen aerospace organizations and companies promoted the strength of the Rockford Region's aerospace supply chain and pursued opportunities to expand their scope worldwide June 19–22 at the 52nd International Paris Air Show.

Greg Papandrew to Lead Advanced Circuits' Offshore Division

Offshore PCB sourcing expert Greg Papandrew has been tapped as the offshore sales director for Advanced Circuits' newly created offshore division. Papandrew is responsible for creating a seamless process and providing the most cost-effective offshore manufacturing solution for high-volume PCB production to customers in the North American market.

Smart Quadcopters Find their Way without Human Help or GPS

Milestone series of tests have quadcopters slaloming through woodlands, swerving around obstacles in a hangar and reporting back to their starting point all by themselves.

Eltek Receives $1.4 Million Loan from Nistec

Eltek Ltd has obtained a loan of NIS 5 million (approximately US$1.4 million) from Nistec Ltd, the company's controlling shareholder.

Need Better RF Performance? FR-4 No More!

Demand for wireless data is growing exponentially, driving a need for substantially higher levels of mobile network capacity and performance. This demand will grow further in support of the upcoming 5G IoT ecosystem where billions of devices will be communicating with each other, and connectivity is immediate and uninterrupted. FR-4 was historically a material choice for many less demanding RF applications, but changes in the wireless infrastructure related to growing performance requirements, especially in small cells and carrier-grade WiFi/Licensed Assisted Access (LAA), have resulted in instances where the properties of FR-4 are lacking, and RF performance and consistency is compromised. There's no longer a need to sacrifice your PCB performance.

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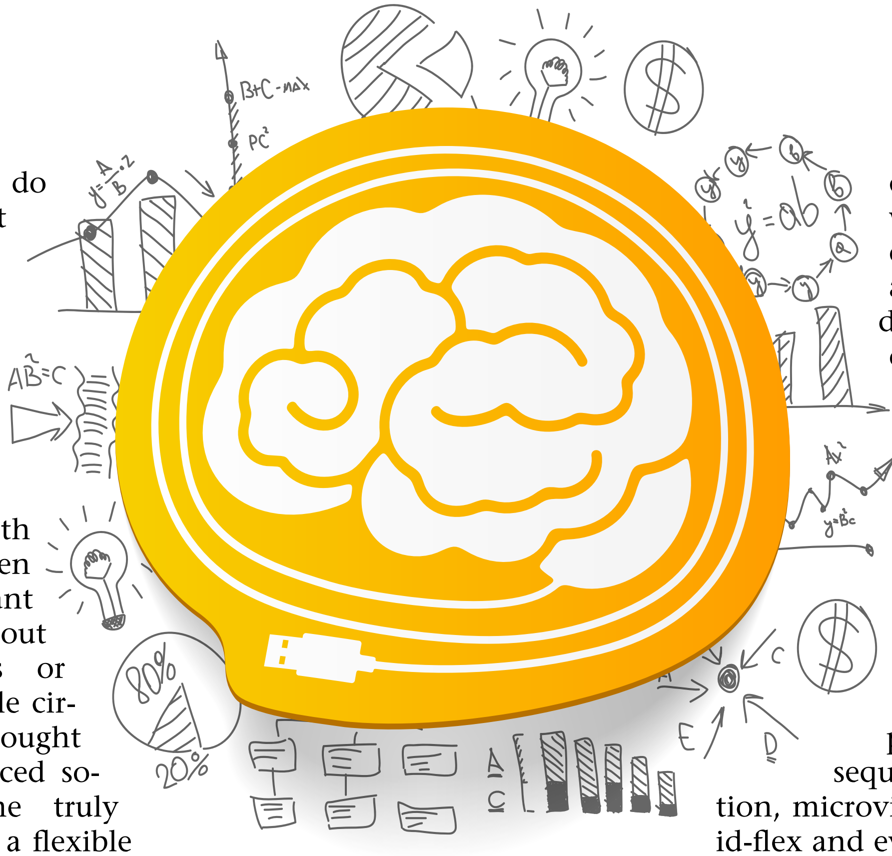
Knowledge is Power

by Tara Dunn
OMNI PCB



"What can I do to help drive cost from my design?" This is a question that I am asked routinely. That question is often followed by, "Can I get these faster?" Both questions are even more predominant when talking about flexible circuits or rigid-flex. Flexible circuits are often thought of as a high-priced solution and one truly wouldn't design a flexible circuit without needing to utilize that technology for some reason. That reason may be space, weight, packaging, flexing requirements or even aesthetics.

I think that most will agree that a quality product that is available when you need it is the primary concern when launching a new design. But, that said, designing the most cost-effective solution to meet your needs is always going to be critical. Today, I want to share my top three tips for reducing cost and shortening lead-time when working with flex.

Understand Fabricators' Capabilities

In today's fast-paced electronics world, designers and engineers rarely have time to visit a board shop for a facility tour to better understand the circuit board manufacturing process. In a perfect world, everyone would have a chance to understand not only the basic process steps that these custom-built products go through, but also understand the complexities that are involved with specialty products such as sequential lamination, microvias, flex and rigid-flex and even flex and rigid-flex with sequential lamination and microvias.

In today's market, there are many companies that manufacture flex and rigid-flex. There is also a significant difference in capabilities across the market. Some manufacturers specialize in single-sided and double-sided flex, some in multilayer, some in rigid-flex. Within each of these specialties, there are companies that work with leading edge technology and some that do not. All can produce quality product. But when looking at ways to ensure you are not adding cost to your design, regularly working with your fabricator and understanding their capabilities and sweet spot in the market and then matching those capabilities with the requirements of the design can have a significant impact.

Here are a couple of examples. First, you are working with two different designs. One is a single-sided flex with 0.010" line/space. The second is a complex, 16-layer rigid-flex with stacked microvias. Your approved supplier list consists of three fabricators who offer flex: Company A manufactures primarily single- and double-sided designs, Company B manufactures both flex and rigid flex, but typically works with designs that are 10 layers or less and Company C specializes in complex rigid-flex. It can get a little tricky. It is very likely that the company that will have the best lead-time and pricing for a complex rigid-flex will not have the best pricing for the simple flex. If cost isn't a factor, it can be easier to order both from the same fabricator, but if cost is a factor, then finding the best fit for each technology level is going to be most cost-effective.

The second example has to do with understanding the capabilities matrix for each supplier. It is important to understand for each supplier that you work with, what is considered standard, advanced and emerging technology. Using drilled hole size as an example, certain manufacturers consider a 0.10" drill to be standard and increased costs are incurred at 0.008". With others there is no increase in cost until you reach .006" drill. This in no way reflects on the quality of the product at each manufacturer, but more reflects their comfort level and their specific cost drivers at a certain level of technology. Once you understand where those thresholds are, you can thoughtfully weigh the cost vs. benefit of moving beyond the standard technology.

Select common materials that are in stock

There are many different types of material available for flexible circuits, and that number grows exponentially when you consider rigid-flex construction. To simplify, using the standard copper/polyimide laminates as an example, the laminate is available in two types: adhesive-based and adhesiveless material. For both types, there are a vast number of combinations of materials. Copper is typically available in ¼ oz. to 2 oz. copper and polyimide thicknesses typically range from 0.5 mil to 6 mil. Sounds great, right? Absolutely! But while these options are available, it does not mean that they are all commonly stocked at a fabricator or that they are low cost. The best advice I can give when designing

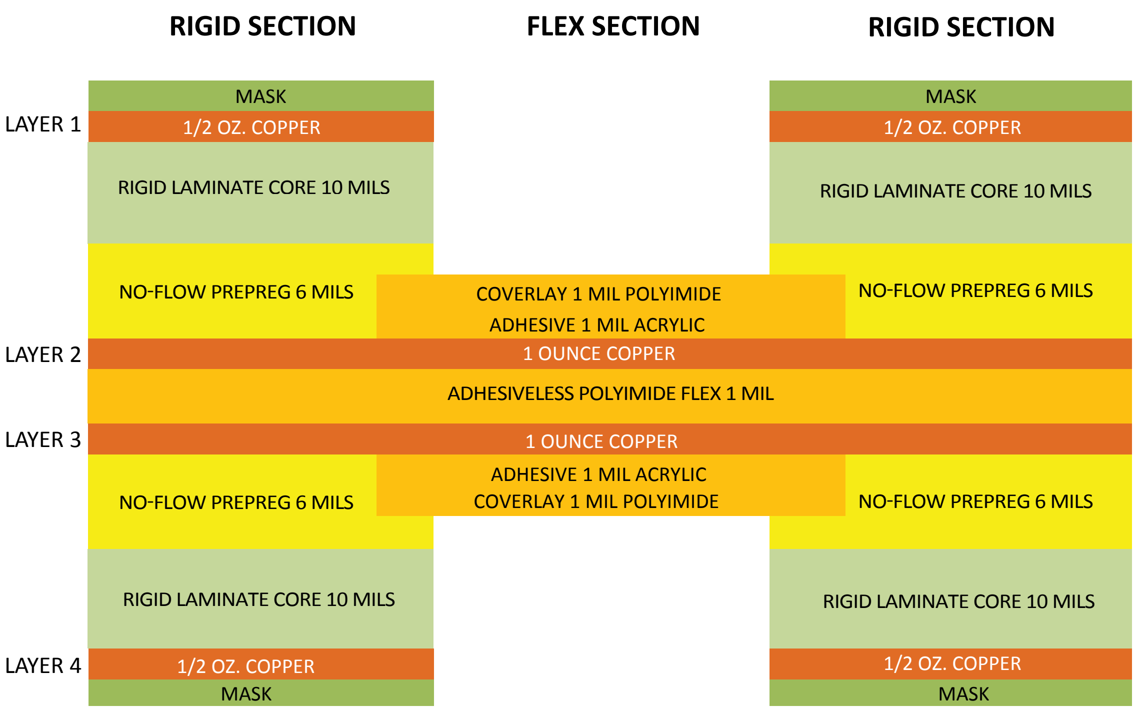


Figure 1: Example of a rigid-flex stack-up. Image source: I-007eBooks, *The Printed Circuit Designer's Guide to...Flex and Rigid-Flex Fundamentals.*

for cost and reduced lead-time is to work closely with your fabricator to develop a stack-up.

In general terms, laminates with ½- or 1-ounce copper and 1- or 2-mil polyimide will be less expensive than other combinations. However, cost and lead-time will boil down to the materials that your selected fabricator works with most regularly. Please don't spec an adhesive-based laminate just because it should be less expensive. If your fabricator manufactures with more adhesiveless materials (highly recommended for rigid-flex), they may be purchasing laminate in enough volume that pricing is reduced and that savings will be passed along to you. The same thing is true for lead-time; designing with materials that are in stock will eliminate the delays from material lead-time when the prototype is placed and lead-time is critical.

My recommendation is to work with your fabricator for a stack-up and be clear about your requirements. Let them know if materials are not critical and ask that they use commonly stocked materials. That eliminates all assumptions and will result in the lowest cost, best lead-time scenario.

Communicate clearly in the fab notes

Typically, 75% of flex and rigid-flex designs go on hold while being tooled at the fabricator. A significant portion of those questions that need to be asked stem from unclear fab notes. An unclear stack-up is a very common issue with rigid-flex. Make sure that you are clearly calling out which layers are flex and which are rigid. If you have asked for the stack-up prior to releasing the design, this is simple to include. Flex and rigid-flex designs can make people unsure and the basics are sometimes overlooked.

Another requirement that can be easily overlooked on the fab notes is the UL requirement. There are many examples where after failing a burn test and investigating the cause, it is found that the UL requirements are clear in the assembly drawings, but not in the fab notes. Your fabricator will not necessarily default to UL materials in the absence of the spec and the contract manufacturer will routinely separate the fab notes from the assembly drawings when asking for a flex quotation. Always clearly state any quality requirements in both the assembly drawings and the fab notes.

What do these have in common? I believe the best way to reduce cost and lead-time is to work with your fabricator throughout the design process and communicate requirements clearly. They say experience is the best teacher and they work with new designs every day. Take advantage of that knowledge! **PCB**

Tara Dunn is the president of Omni PCB, a manufacturer's rep firm specializing in the printed circuit board industry. To read past columns or to contact her, click here.

Moving into Microvias: The Interaction of Materials and Processes, Part 1

by Michael Carano
RBP CHEMICAL TECHNOLOGY

In the first part of a series of columns focused on microvias, the importance of adopting HDI technology as a strategic initiative for the PWB fabricator is presented. The major drivers for HDI are listed.

Introduction

Let's face it. If you are in the printed circuit board fabrication business (and want to stay in—assuming you want to make money as well), acquiring HDI capability is very important. Part and parcel to this is adopting enabling processes and technologies that encompass design, material selection, improved wet processes and imaging technology, laser formed microvias and equipment packages. If designed with the proper architecture, printed circuit boards with microvias offer the most significant opportunity to reduce the layer counts and overall board thickness. In addition, the cost may be reduced while improving electrical performance and density of the interconnect.

Design for HDI

Blind microvias are a surface feature. With the optimum architecture, routing densities are increased and some of the layers in a traditional through hole designed multilayer board layers can be removed. An example of this is illustrated in Figure 1.

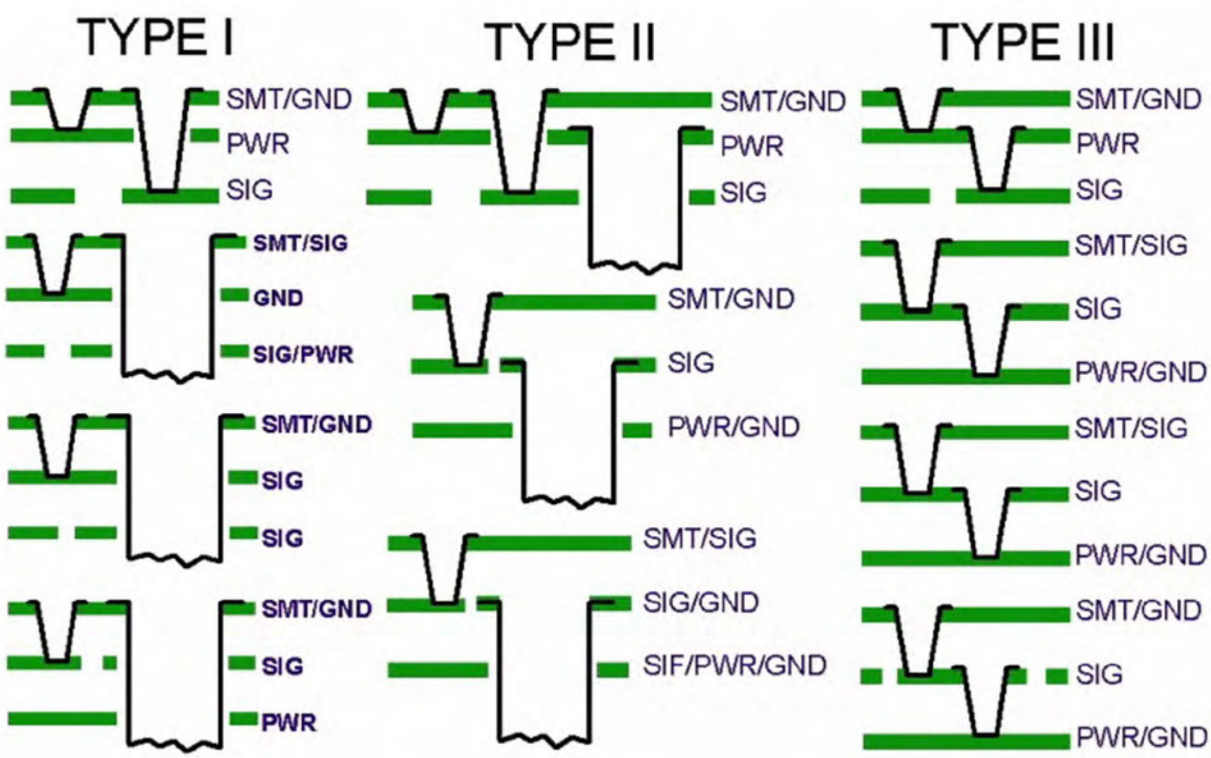


Figure1: Various layer assignments available when using HDI and microvias (Source: Happy Holden).

First priority is to reduce and elliminate through-vias. These block routing channels on the innerlayers. By eliminating 25% of the TH, 2-3X as many traces can be routed on the innerlayers. One way to do this is to move the ground plane (that is usually on layer 2) to the surface and use the microvias as via-in-pad (VIP) or near-via-in-pad (NVIP). This eliminates the most abundant vias on the boards- the ones to ground. As a consequence blind vias will have more conventional aspect ratios. More on this in a futue column.

Drivers for HDI

One needs to fully understand end user requirements prior to making capital investments for HDI production. It is a given that electronic systems and packages are becoming denser. All one has to do is look at the latest smart phones and tablets. However there are other drivers for this miniaturization trend that may not be obvious to the reader. Fine-pitch packages (QFPs and BGAs) and increasing pin counts of packages are driving the interconnect designs for military-aerospace, medical, telecom and industrial electronics. HDI, when properly designed into the PWB structure, improves signal integrity as well as via reliability.

Again, let's list the main drivers for HDI:[1]

- Integration of high-I/O and fine-pitch devices
- Higher component density and component I/Os
- Reduction in layer count for thickness control and RoHS compliance (LF assembly)
- Improved electrical performance and SI (reduced noise, EMI and RFI)
- Effective integration of embedded passives
- Lower costs through less layers and smaller boards

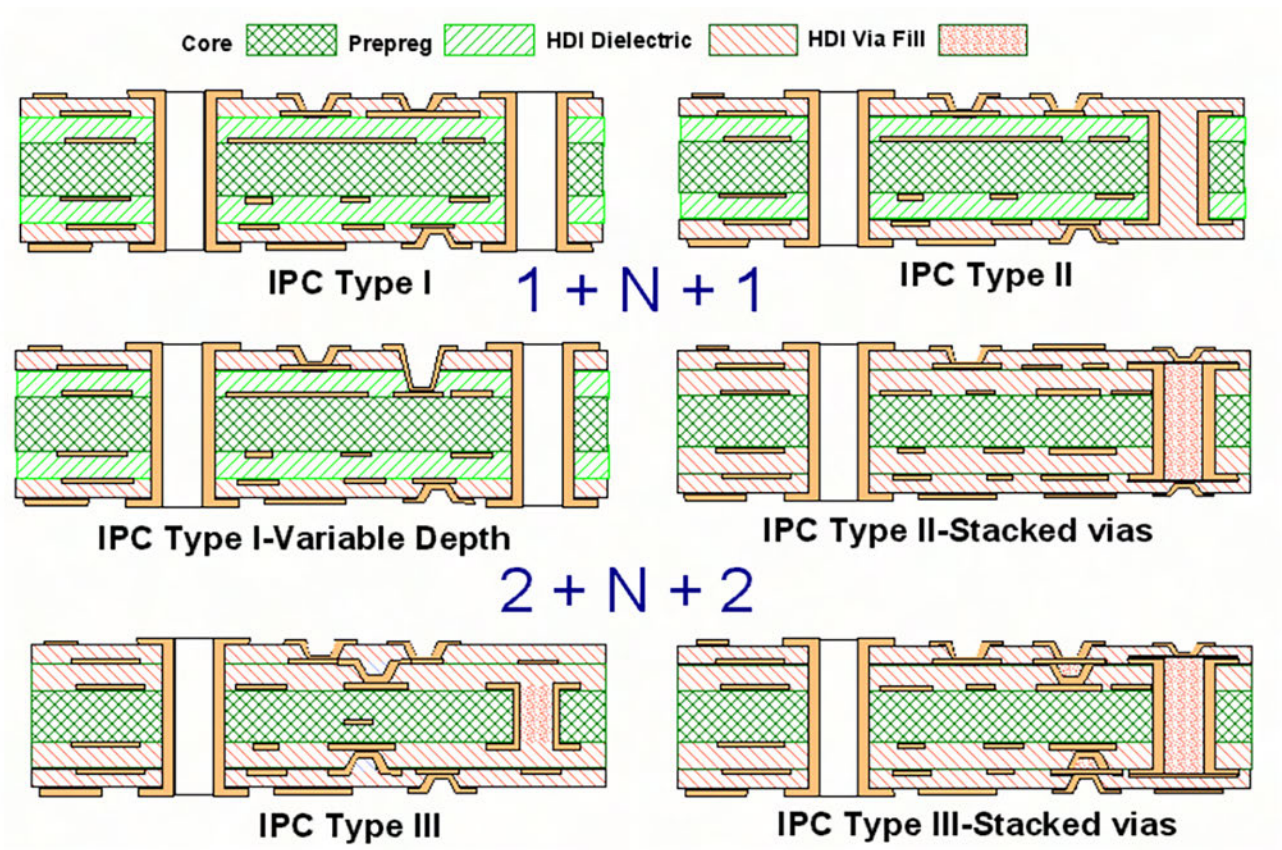


Figure 2: The IPC HDI Type I to Type III are the most common microvia structures used—from the simplest (Type I) to the most complex (Type III with stacked vias)[2].

So why is this important? First, don't look at HDI as something "just for mobile phones." When you hear someone capitulate to that way of reasoning, that person is not looking at HDI from a strategic point of view. And this is not to say that all fabricators should simply rush into HDI for to be fashionable! This is all about technology and go-to-market strategy for the business. So think it through and assess one's capabilities. Don't expect that the fabricator already possesses the competencies to successfully implement an HDI manufacturing technology. That would be a mistake. Thus, it is important to remember that there are several disciplines to master including material selection, blind via and microvia formation, circuit formation, lamination and metallization. Even though microvias are the primary feature for HDI constructions, thinner dielectrics, ultra-thin copper foils and finer lines and spaces are key features as well. There is also a movement to coreless lam dielectrics and dielectric build-up materials in place of copper clad laminate. These last two are also enablers for finer lines and spaces. Basically, getting into HDI requires changing one's thinking about PWB fabrication. And that must first start with getting familiar with standards.

HDI Standards

As one decides to adopt HDI, the IPC-2315 HDI Design Standard will be required reading. This critical document outlines the simplest architectures for HDI (Figure 2).

Keep in mind that there are tradeoffs when designing interconnects with blinds vias. In addition, PWBs with only through-holes designed in limit the density one can achieve. Without microvias, layer counts and costs will increase to support higher pin counts. **PCB**

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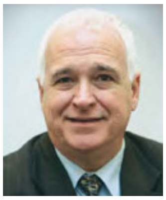

Michael Carano is VP of technology and business development for RBP Chemical Technology. To reach Carano, or read past columns, click here.

Bringing Neural Networks to Cellphones

The best-performing artificial-intelligence systems—in areas such as autonomous driving, speech recognition, computer vision, and automatic translation—have come courtesy of software systems known as neural networks. But neural networks take up a lot of memory and consume a lot of power, so they usually run on servers in the cloud, which receive data from desktop or mobile devices and then send back their analyses.

Last year, MIT associate professor of electrical engineering and computer science Vivienne Sze and colleagues unveiled a new, energy-efficient computer chip optimized for neural networks, which could enable powerful artificial-intelligence systems to run locally on mobile devices.

Now, Sze and her colleagues have approached the same problem from the opposite direction, with techniques for designing more energy-efficient neural networks. First, they developed an analytic method that can dete mine exactly how much power a neural network will consume. Then they used the method to evaluate new techniques for paring down neural networks so that they'll run more efficiently on handheld devices.

The researchers describe the work in a paper next week at the Computer Vision and Pattern Recognition Conference. In the paper, they report that the methods offered as much as a 73% reduction in power consumption over the standard implementation of neural networks, and as much as a 43% reduction over the best previous method for paring the networks down.

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India Makes Manufacturing Gains to Participate in a Global Economy

by John Mitchell
IPC—ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

The manufacturing industry is truly a global one. While the past few decades have seen the rise of manufacturing in China and countries throughout Europe and South America, the last 10 years have been marked by significant progress in India. While the greater Asian area has flourished, India has been hampered by many factors including a struggling infrastructure.

These difficulties with infrastructure won't impede growth in India, but still need to be addressed to ensure expectations don't fall short of desire. Especially considering the "Make in India" initiative, launched in 2015 by Indian Prime Minister Narendra Modi, which pitches India as a business-friendly destination to attract foreign businesses to invest and manufacture in the country.

While the Indian government has taken several initiatives to promote a healthy environment for the growth of the manufacturing sector, they are cognizant of the local communities' needs and how the implementation of new projects will impact cities versus remote villages.

With that said, according to Industry Week, India is predicted to be in the top five manufacturing nations in the world by 2020. Currently, India is the third-largest economy in purchasing power parity after the United States and China. On top of that, it has a large population of engineers and factory workers, its intellectual property is widely respected, and it is easy to find English-speaking managers from India. Despite this, India still faces a workforce issue.

Like the United States, Europe, and much of the world, India is facing a skills gap and workforce development issue. Because of the "Make in India" program, many foreign companies are vying to bring manufacturing to India. Apple's recent announcement of opening a manufacturing plant in Bengaluru means big things for India and its economy. However, like many new manufacturing facilities, Apple will likely take advantage of both advanced manufacturing and the Industrial Internet of Things (IIOT)

to create an automated plant. While this still means jobs for India, those jobs may be out of the technical range of those currently trained to traditional manufacturing practices.

This is of serious concern to India, as by 2020, the country will boast more than 900 million people of working age[1]. It is estimated that two years later, India will pass China to become the most populous country in the world. To add to these concerns, the Labor Ministries' data estimates around one million people will enter India's workforce every month.

Along with this growth, India continues to excel in the automotive sector. The Indian automotive industry is one of the largest in the world with an annual production of 23.96 million vehicles in 2015–16, following a growth of 2.57% over the last year. The automobile industry in India also accounts for 7.1% of the country's gross domestic product (GDP)[2]. The government also has a plan for the faster adoption and manufacturing of electric and hybrid vehicles, known as the National Electric Mobility Mission 2020. The goal of this is to encourage progressive introduction of reliable and affordable electric vehicles into the country.

As business leaders, we should continue to watch the burgeoning manufacturing economy of India as they work hard to achieve success in the global community. IPC will continue to work hard to support the manufacturing economy in India as the country grows to further become a participant in the international electronics industry. **PCB**

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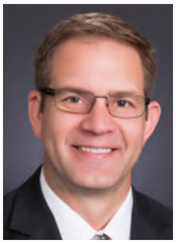
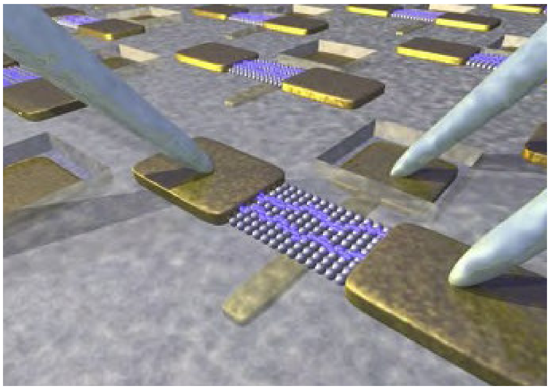


John Mitchell is president and CEO of IPC—Association Connecting Electronics Industries. To read past columns or to contact Mitchell, click here.

Researchers Develop New Transistor Concept

Transistors, as used in billions on every computer chip, are nowadays based on semiconductor-type materials, usually silicon. As the demands for computer chips in laptops, tablets and smartphones continue to rise, new possibilities are being sought out to fabricate them inexpensively, energy-saving and flexibly. A group led by CUI scientist Dr. Christian Klinke (Universität Hamburg) has now succeeded in producing transistors based on a new principle. The research results have been published in the scientific journal Science Advances.



The transistors developed by Klinke's group use metal nanoparticles so small they no longer show their metallic character under current flow, but exhibit an energy gap caused by the Coulomb repulsion of the electrons among one another. Via a controlling voltage, this gap can be shifted energetically and the current can thus be switched on and off as desired. In contrast to previous similar approaches, the nanoparticles are not deposited as individual structures, rendering the production very complex and the properties of the corresponding components unreliable, but, instead, they are deposited as thin films with a height of only one layer of nanoparticles. Employing this method, the electrical characteristics of the devices become adjustable and almost identical.

ARTICLE

High-Throw DC Acid Copper Formulation for Vertical Continuous Electroplating Processes

by Saminda Dharmarathna, Ivan Li, Maddux Sy, Eileen Zeng, Bob Wei, William Bowerman, and Kesheng Feng
MACDERMID ENTHONE ELECTRONICS SOLUTIONS

Abstract

The electronics industry has grown immensely over the last few decades owing to the rapid growth of consumer electronics in the modern world. New formulations are essential to fit the needs of manufacturing printed circuit boards and semiconductors. Copper electrolytes for high throwing power applications with high thermal reliability and high throughput are becoming extremely important for manufacturing high aspect ratio circuit boards.

Here we discuss innovative DC copper metallization formulations for hoist lines and vertical continuous plating (VCP) applications with high thermal reliability and throughput for high aspect ratio PCB manufacturing. The formula has a wide range of operation for current density. Most importantly, plating at high current density using this DC high-throw acid copper process offers high throughput, excellent thermal reliability, and improved properties for present-day PCB manufacturing. The operating CD range is 10–30 ASF where micro distribution of ≥ 85% for AR 8:1 is achievable. This formulation offers bright ductile deposits where plating parameters are optimized for improved micro-distribution and the properties of the plated copper deposit such as tensile strength and elongation. The thermal reliability and properties of the deposits were examined at different bath ages. Measured properties are: Elongation ≥ 18% and tensile strength ≥ 40,000 psi. All the additives can be easily controlled by cyclic voltammetry stripping (CVS) analysis.

Introduction

Copper has a high electrical conductivity and is relatively inexpensive compared to other high conductive metals such as silver. Therefore, the use of copper in the mass production of PCBs and semiconductors grew exponentially in the last few decades[1]. With today's complex circuit board designs an even deposition with specific physical properties is necessary to meet the standards. Especially with high aspect ratios, through-hole plating to obtain desired plating distribution is much more challenging. During the quality control inspection, a board can be rejected if there is insufficient copper on the center walls of the through-holes. Moreover, plated copper should meet the minimum requirements of physical properties such as tensile strength and elongation (T&E) to withstand the high temperature applications[2].

Sulfuric acid copper baths are heavily used in the PCB industry due to their low maintenance cost as compared to other acids like MSA (methane sulfonic acid). Typical sulfuric acid copper baths contain copper sulfate, sulfuric acid, chloride ions, and organic additives. These additives play a crucial role in controlling the deposit distribution as well as the properties. To meet specific objectives of a plating process these additives should be monitored and controlled properly. The additives work in combination and when controlled within a given range improve thickness distribution, mass transfer, eliminate nodule formation and can fill blind vias. Namely these additives are levelers, brighteners, and suppressors. The leveler is a mild suppressor that adsorbs onto specific locations such as corners and peaks of base materials[2].

In the presence of a micro profile the diffusion layer tends to be thin at the peaks and thick at the valleys. In this case, if plated without a leveler the micro profile will be exaggerated. On the other hand, if a leveler is present the plating on the peaks will be suppressed and the micro profile will be diminished. Brightener is also called an anti-suppressor and as the name implies it reduces the suppression. Most importantly, it also acts as a grain refiner to deposit copper with a fine grain structure in random orientation[4]. Therefore, brightener has the most influence on final structure and physical properties of the deposit such as tensile strength and elongation.

The suppressor works in the presence of chloride ion to adsorb onto the cathode and increase the effective thickness of the diffusion layer[3]. Consequently, the plating current increases and the deposit becomes more uniform and a densely packed copper deposit can be obtained without burning. This modified diffusion layer improves the distribution of the deposit especially in high throw applications. Owing to the growth of high aspect ratio circuit board manufacture, the demand for high throw acid copper electrolytes has increased dramatically over the past few decades. Especially DC copper plating for high aspect ratio electroplating is extremely desirable due to simplicity of the process and inexpensive equipment requirements[1, 2].

In this work, we present an innovative DC high throw acid copper electroplating system with high thermal reliability and even copper metallization in high aspect ratio PCBs. This system also allows the plating to be done at high current density without surface imperfections. The allowable CD ranges from 10–30 ASF and the micro distribution(MD) measured is ≥ 85% for the AR 8:1.

Parameter	Range	Optimum
Anode Current Density	1.0 – 3.5 ASD (10-32 ASF)	2.2 ASD (20 ASF)
Temperature	20 – 27°C (68 - 80°F)	23°C (73°F)
Material A Wetter	3 – 8 mL/L	5 mL/L
Material A Brightener	0.7 – 1.3 mL/L	1 mL/L
Material A Leveler	7 – 13 mL/L	10 mL/L
Copper Sulfate ($CuSO_4 \cdot 5\ H_2O$)	60 – 80 g/L	70 g/L
Free Sulfuric Acid 66°Be Electronic Grade	190 – 210 g/L	200 g/L
Chloride Ion (Cl^-)	50 – 70 ppm	60 ppm

Table 1: Bath components.

Numerous tests were performed to obtain high MD at various current densities with enhanced mechanical properties of the plated metal such as tensile strength and elongation. Thermal reliability and structure of plated copper was also studied.

Conditions and Bath Components

Table 1 shows the operating conditions and optimum additive levels. Typically, the high throw bath has high acid to achieve higher conductivity inside the holes.

Test Vehicles

Various test panels with different thicknesses and hole diameters were used covering a range of aspect ratios. The test vehicles used in the process evaluation were 1.6 mm, 2.4 mm and 3.2 mm thick boards and the through-hole diameters were 0.2 mm, 0.25 mm and 0.35 mm. The through-hole aspect ratio (AR) varied from 4.6:1 to 16:1. All geometries for each test board thickness were plated at the same time in the same tank and throw power was later calculated by using cross section analysis.

The process flow included the following operations:

- Acid cleaner—wets the hole and remove any organic contaminants
- DI water rinse
- Micro-etch—further smooths the surface and ensures excellent copper to copper adhesion
- DI water rinse
- Acid dip—acidifies copper surface prior to plating
- Electroplating of copper in acid copper bath

Cross-Section Analysis

Cross-section analysis was started with the sample preparation process by punching or routing sections from a desired area on the board or test panel. Pre-grinding of the coupon was done to get a flat surface closer to the through-holes. Plastic index pins were used to align the coupon vertically to the grinding surface. A fast-cure acrylic resin was used to mount the coupons. A ratio of 1-to-1, hardener-to-resin, was used to provide optimum penetration and a quick cure rate (10–15 minutes). After the sections hardened they were subjected to grinding, polishing, and microscopic inspection to obtain micro distribution. Figure 1 shows a cross-section of a through-hole indicating the points of thickness measurements.

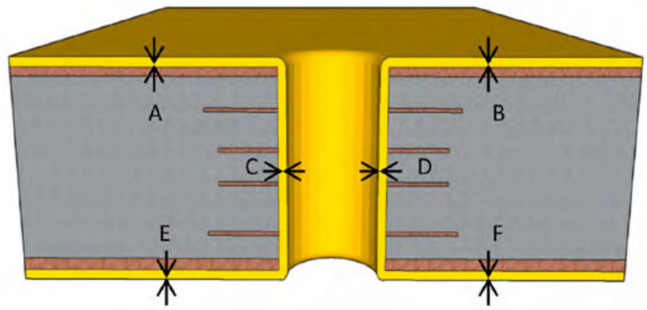


Figure 1: Cross-section of plated panel.

Microdistribution

The micro distribution is defined as the ratio of the average copper deposit thickness in the center of the through-hole to the average copper deposit thickness at the surface. It is calculated according to the following equation:

Eq. 1:

$$Microdistribution = \frac{(C+D)/2}{(A+B+E+F)/4} \times 100\%$$

Results

Microdistribution

Microdistribution (MD) is the ratio between the average plated thicknesses in the middle of the hole to the average plated thickness on the surface as shown in Figure 1. Care should be taken when using MD % due to the difference in the board thickness, as the same diameter hole will be more difficult to plate in the thicker board as shown in Figures 2, 3, and 4. At the same current density, the same diameter hole has lower MD in a thicker board. For instance, a 0.2 mm hole in a 1.6 mm board at 10 ASF gave 90% MD measurement, while a 0.2 mm hole in a 2.4 mm board at 10 ASF gave only 75% MD measurement. Furthermore, a 0.2 mm hole in a 3.2 mm board gave 61% MD. Therefore, aspect ratio should be used to define the difficulty of the plating.

Another crucial factor which determines the MD % is the mass transfer, which is directly proportional to the diffusion. While several factors influence diffusion, one significant factor is the current density at which the plating is done. At high cathodic current density, the abundance of electrons at the cathode accelerates the reduction reaction of copper ions to copper metal at the cathode. Due to this the copper ions in the diffusion layer will exhaust rapidly. If the copper ions in the diffusion layer continue to drop without replenishment from the bulk electrolyte, the deposit could show severe surface burning and cause poor distribution. On the other hand, at relatively low current density the plating rate will be low with the depletion of copper ions in the diffusion layer due to the reduction reaction. Since the plating rate is low there will be enough time for the copper ions in the bulk electrolyte to replenish the diffusion layer. Owing to this equilibrium there will be an even distribution and no burning will occur.

This phenomenon is clearly shown in Figures 2, 3, and 4. As an example in Figure 2, at 10 ASF a 0.35 mm hole showed 99% MD whereas when the CD increased to 20 ASF the MD dropped to 95% for the same hole in the same board thickness and further, at 30 ASF the MD dropped to 87%.

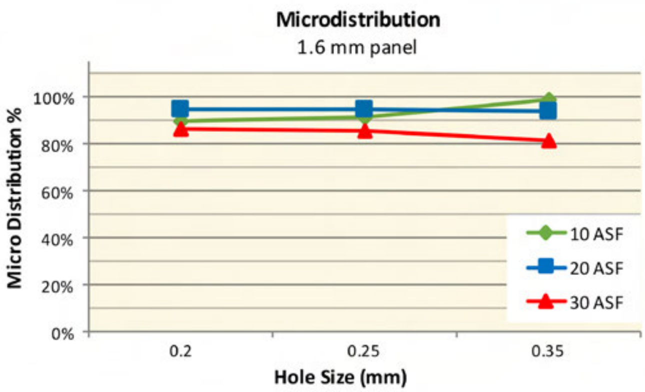


Figure 2: Micro distribution for 1.6 mm panel aspect ratio: 8:1, 6.4:1, and 4.6:1.

Surface, Structure, and Morphology

All the plating conditions produced smooth, ductile, uniform, and mirror-bright surfaces. Excellent leveling was seen inside the hole as shown in Figure 5. Further, Figure 5 shows no thin copper at the knee in the cross-sectional images for the 1.6 mm thick board plated at current densities 10, 20, and 30 ASF respectively. Uniform fine-grained copper layers throughout the hole is observed. After the microscopic evaluation, the sections were further evaluated using scanning electron microscopy (SEM). Figure 6 shows the results from the SEM analysis where three different areas were analyzed; inside the hole, corner, and the surface. Despite the current density difference at the corner and inside the hole or at the surface, the morphology shows the same fine equiaxial grains. No preferred orientation like columnar grains were observed.

Physical and Thermal Properties

Final deposit plated under the influence of additives suppressor, grain refiner, and level-

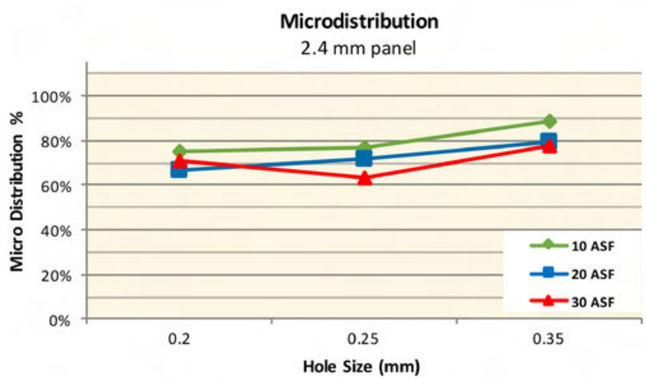


Figure 3: Micro distribution for 2.4 mm panel aspect ratio: 12:1, 9.6:1, and 6.9:1.

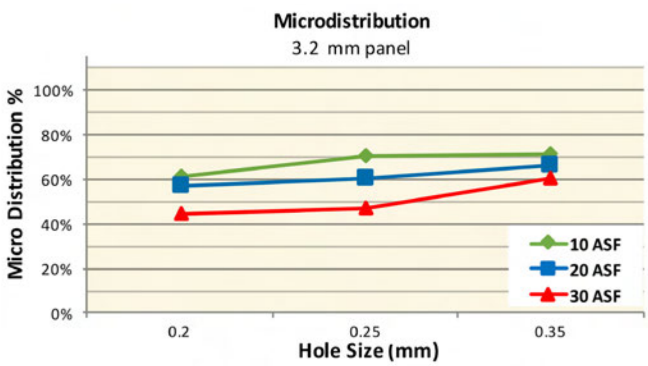


Figure 4: Micro distribution for 3.2 mm panel aspect ratio: 16:1, 12.8:1, and 9.1:1.

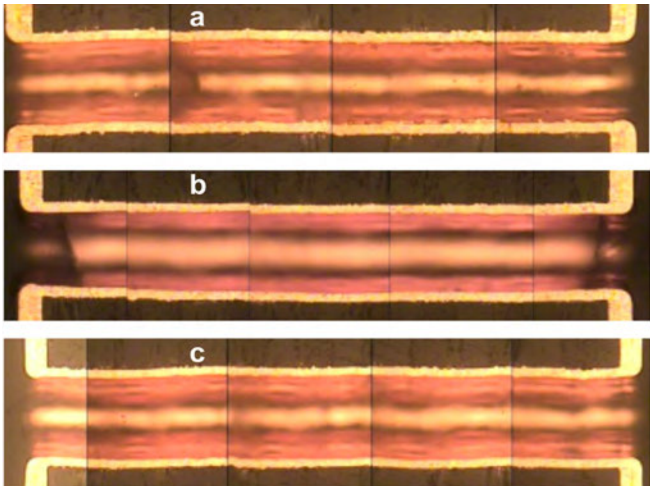


Figure 5: Cross-sections of through-holes plated at a) 10 ASF; b) 20 ASF; c) 30 ASF; 1.6 mm test panel.

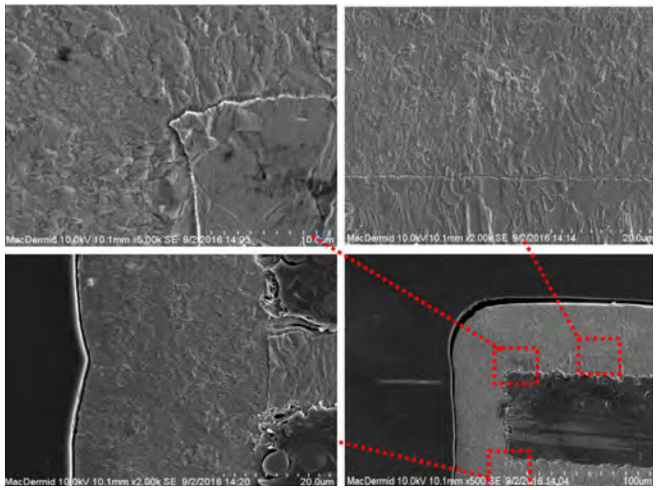


Figure 6: Scanning electron microscopy (SEM) of IST 22-layer through-holes plated at 10 ASF with 2.4 mm test panel.

er will show characteristic physical properties. These properties also depend on the plating rate or current density, temperature at which the plating is done, and the morphology. For instance, a densely packed equiaxial deposit will have better physical properties than a columnar deposit. Most important to PCB manufacturing are tensile strength and elongation %, where these properties show the tolerance of the deposit for thermal stress.

Physical properties were measured according to the IPC TM-650, 2.4.18.1 test method. Sample strips were extracted and baked in an oven at 125°C for four to six hours. An industry mechanical test instrument was used to test the strips. The measurements were used to calculate tensile strength and elongation % using equations 2, 3, and 4. Table 2 shows the results at two different bath ages, fresh bath and bath aged around 50 Ah/L. According to the results properties did no change much with the bath age.

Property	Fresh Bath	Aged Bath
Tensile Strength (psi)	43,120	44,470
Elongation %	22.18	26.35

Table 2: Physical properties.

Further, to evaluate thermal characteristics of the deposit, the 6X solder shock resistance test was performed on plated through-holes in accordance with IPC TM-650 2.6.8. Solder shock (SS) conditions were 10 seconds float at 288°C for six times on the same side of the test coupon. Results are shown in Figure 7. After 6X SS testing, no corner cracks, barrel cracks, or hole wall pull-away was observed.

Eq. 2: $$\text{Mean average cross-sectional area } (in^2) = \frac{\text{Weight of the sample (lbs)}}{\text{Length of tensile sample (in) x density of copper } (g/in^3)}$$

Eq. 3: $$\text{Tensile Strength} = \frac{\text{Maximum load (lbs)}}{\text{Mean cross-sectional area } (in^2)}$$

Eq. 4: $$\text{Elongation} = \frac{\text{(Length at break – Original gage length)}}{\text{Original gage length}}$$

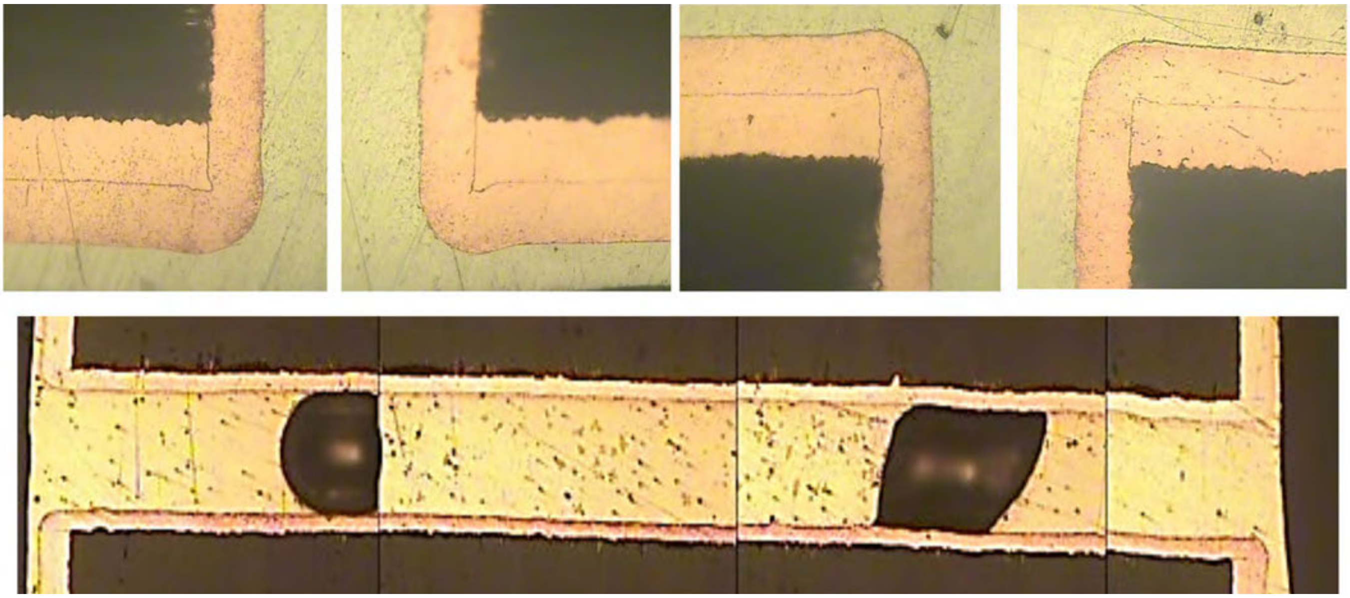


Figure 7: 6X thermal shock test.

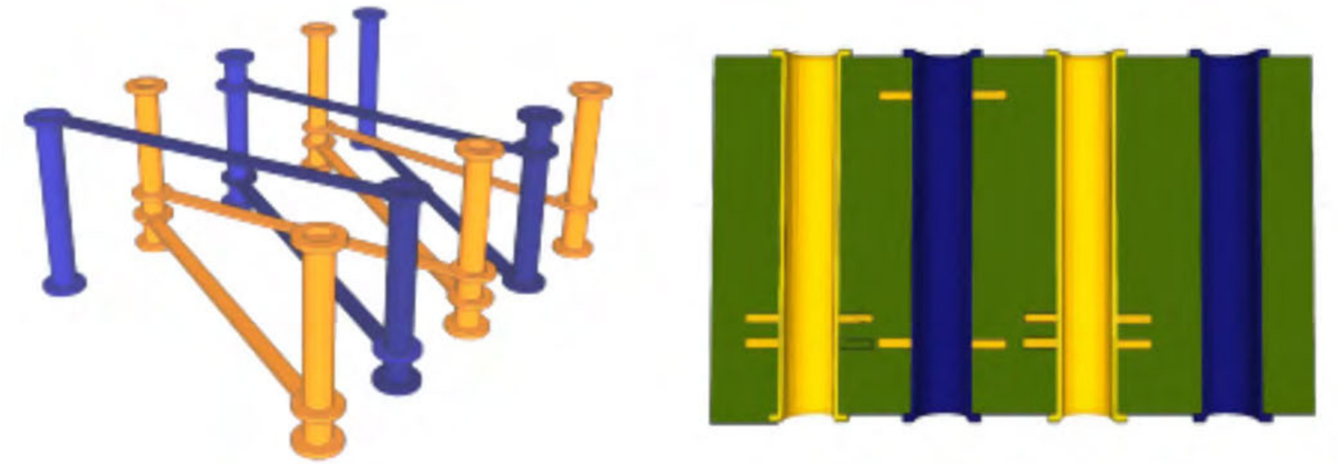


Figure 8: Assembly of through-holes in an IST coupon. Power is shown in gold and the sense is in blue.

Interconnect stress testing (IST) was also carried out to further characterize the deposit. IST testing is an accelerated test method used to evaluate the integrity of interconnects and plated through-holes. This method utilizes electrical currents passed through a circuit in the board at sufficient resistance to increase temperature. Coupons were run through assembly simulation called preconditioning prior to cycling. Coupons were tested prior to preconditioning for continuity. Figure 8 shows the assembly of through-holes in an IST coupon and the electrical continuity.

A coupon was sacrificed to determine the current needed for preconditioning. All coupons were preconditioned six times to 260°C prior to cycling at 150°C to 500 cycles or to failure. After preconditioning, baseline resistance readings were established and the temperature cycling was started. Each thermal cycle consists of passing sufficient current through the internal power circuit to elevate the temperature to 150°C, then subsequent cooling down to ambient temperature. During the temperature cycling, resistance is monitored on the power circuit and the sense circuit. If the re-

Material A bh, p2-s2, 6xpre cond_dat.csv					
Coupon #	#2	#4	#6	#9	#11
Cycles	500	500	500	500	500
%P	0.430	0.267	0.405	0.264	0.462
%S	1.243	1.240	3.038	2.878	1.392
Material A - p2s2, 6xpre_dat.csv					
Coupon #	#2	#3	#6	#9	#11
Cycles	500	500	500	500	500
%P	0.000	-0.380	0.072	-0.462	-0.393
%S	-0.070	-0.280	-0.069	-0.355	-0.591

Table 3: Interconnect Stress Testing (IST) data.

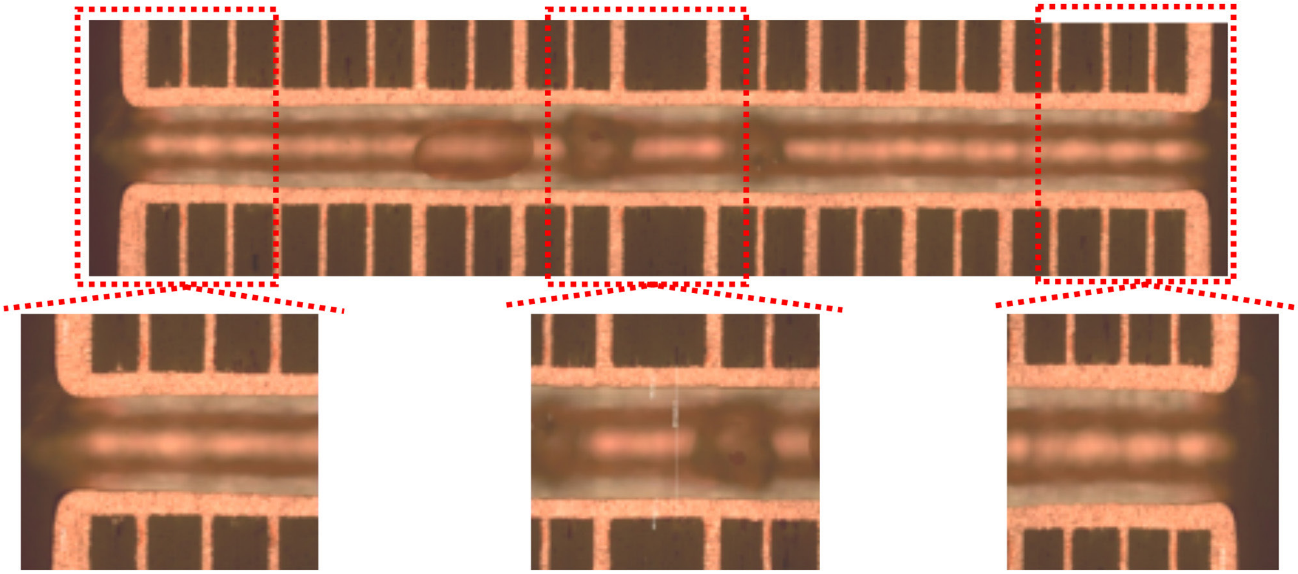


Figure 9: Cross-sections of IST 22-layer through-holes plated at 10 ASF with 2.4 mm test panel.

sistance is >10% over the established baseline on either circuit, it is considered a failure and the test is halted. Material type and complexity of the build have an influence on the cycles to failure. Table 3 shows the results from the IST test and all five coupons tested passed the 500 cycles test. This test also confirms and agreed with the 6X solder shock test. Figure 9 shows a cross-section of a through-hole with 22 layers extracted from the IST test panel after plating.

Conclusions

An excellent formula was developed for DC copper metallization for hoist lines and VCP applications. The operating CD range is 10–30 ASF where, micro distribution of ≥85% for AR 8:1 is achievable. Deposits were bright and ductile and also met IPC standards for the properties such as tensile strength and elongation. The thermal characteristics of plated copper also met the IPC standards and showed no failure during the solder shock tests. Coupons also passed the 500 cycles in IST testing. All the organic additives can be easily monitored by industry CVS analysis. **PCB**

This paper was originally presented at the IPC 2017 APEX EXPO conference and was published in the proceedings.

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Soft and Stretchy Fabric-Based Sensors for Wearable Robots

Wearable technologies—from heart rate monitors to virtual reality headsets—are exploding in popularity in both the consumer and research spaces, but most of the electronic sensors that detect and transmit data from wearables are made of hard, inflexible materials that can restrict both the wearer's natural movements and the accuracy of the data collected. Now, a team at Harvard's John A. Paulson School of Engineering and Applied Sciences (SEAS) and the Wyss Institute for Biologically Inspired Engineering at Harvard University has created a highly-sensitive soft capacitive sensor made of silicone and fabric that moves and flexes with the human body to accurately detect movement.

"We're really excited about this sensor because, by leveraging textiles in its construction, it is inherently suitable for integration with fabric to make smart robotic apparel," said corresponding author Conor Walsh, the John L. Loeb Associate Professor of Engineering and Applied Sciences at SEAS and Core Faculty member at the Wyss Institute.

"Additionally, we have designed a unique batch-manufacturing process that creates custom-shaped sensors that share uniform properties, making it possible to quickly fabricate them for a given application," said co-author Ozgur Atalay, a postdoctoral fellow at the Wyss Institute. This research is published in the current issue of Advanced Materials Technologies, and the protocol is available as part of the Harvard Biodesign Lab's Soft Robotics Toolkit.

Professor Plum in the Library with the Candlestick...Right?

by Keith M. Sellers
NTS-BALTIMORE

Who knew that a phrase from a decades-old popular board game could have some relevance in today's ever-changing world? In the game of Clue, simply put, evidence is collected and then used to solve a mystery. In my world, testing is performed to gather data/results (evidence) and then this information is used to determine the root cause of some issue that is under investigation (solving the mystery). The recommendations made as a result of a failure analysis investigation commonly lead back to some step along the manufacturing process that now needs to be scrutinized and evaluated and then possibly improved and/or changed. To effectively do this, having information from the steps in that process (evidence, again) is a key component of the potential solution. This latter idea is the main subject of this month's column, or in a simpler way, how traceable is your process?

When a manufacturing process is humming along, widgets whizz through many pieces of equipment and through many sets of hands until they eventually find their purpose out in the real world. Initial loading, component population, reflow, hand soldering stations, installation into a housing, cabling, functional checks, and potentially many, many more operations... are just some of the steps that a widget might be exposed to during its manufacturing. The process, by its nature, requires a myriad of steps, one potentially very different from the next. Some steps are likely to be very repetitive in nature and very repeatable in execution from lot to lot, while others, maybe not so much.

Regardless of the operation being performed and whether it's heavily automated or not, having traceability of each individual step through the process as a whole is vitally important. Knowing who did it, when they did it, what

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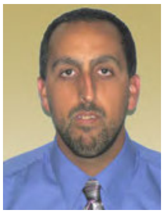
tools/materials/supplies they used to do it, and the conditions under which they did it are just a few bits of information that should be known and readily available to someone investigating a process that has produced some bad widgets.

For example, let's say our widget is a sealed unit that has a printed circuit assembly inside that is sensitive to moisture. The unit itself has a cover on it that is attached via screws with a gasket for sealing purposes. The client is experiencing failure of the widget when it is installed in a humid/wet environment. As a result of testing that would have been performed to investigate the issue, let's say that the root cause of the field failures was determined to be water/moisture ingress around the cover.

From here, the owner of the widget would likely go to the manufacturing line to investigate the cover attach process. So, at this point, the more information that the investigator can get about that step in the process the better. A simple bit of information would obviously be to know which operator installed the screws and which screwdriver they used, but that might only be the tip of the iceberg in respect to what information could be known. Other examples of bits of information that would likely be of interest in this situation would be...How much torque was applied to the screws? What is the material (lot) traceability of the cover plate? What is the material (lot) traceability of the gasket? What is the material (lot) traceability of the screw? What were the environmental conditions on the line when the unit was sealed?

Those are just a few of the questions that the investigator might ask to try to solve the issue at hand. Thus, having complete traceability of your process will allow for easy dissemination of the needed information. Who knows... maybe the solution is as simple as a bad lot of gaskets? Or, maybe, the torque setting on the screwdriver was incorrect from 9–11 a.m. on a given Tuesday? These are all very plausible answers to our example, but finding these answers would be impossible if the traceability information wasn't being recorded and/or stored.

Traceability is not designed to be a blame game, although that does unfortunately sometimes happen given the world we all live in. From an analytical vantage point, establishing a mentality in which everyone understands that traceability allows for quicker and more efficient problem solving and troubleshooting when/if things go awry is really the greater theme. If you knew it was Professor Plum in the library with the candlestick from the very beginning....wouldn't the game be much easier to play? **PCB**



Keith M. Sellers is operations manager with NTS in Baltimore, Maryland. To read past columns or to contact Sellers, click here.

Designing Computer Software of the Future

Quantum computers of the future hold promise for solving complex problems, like factoring large numbers, exponentially more quickly than ordinary computers, allowing them to break codes in commonly used cryptography systems. Other applications for quantum computers include solving complicated chemistry problems involving the mechanics of molecules. But exactly what types of applications will be best for quantum computers is still an open question.

In a new Caltech study, accepted by the Institute of Electrical and Electronics Engineers (IEEE) 2017 Symposium on Foundations of Computer Science, researchers have demonstrated that quantum computing could be useful for speeding up the solutions to "semidefinite programs," a widely used class of optimization problems. These programs include so-called linear programs, which are used, for example, when a company wants to minimize the risk of its investment portfolio or when an airline wants to efficiently assign crews to its flights.

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Southern California Territory Sales Engineer

Technica, USA, a Western regional manufacturer's representative/distributor, has an open sales position for our Southern California territory. The position will be responsible for selling and servicing our entire product line within the specified territory to the PCB manufacturing industry.

This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Required Skills:

- BA/BS degree-desired, in a technical area is preferred
- Two years of outside/inside sales or manufacturing experience in the PCB manufacturing environment is desired
- Self-motivated self-starter with the ability to initiate and drive business with little supervision
- Independent worker with a strong commitment to customer satisfaction
- Understanding of consumable sales process
- Ability to organize activities and handle multiple projects simultaneously with effective and timely follow-up
- Ability to solve problems and make decisions for which there are no precedents or guidelines and be resourceful in nature
- Positive attitude while operating under pressure and be an independent problem-solver
- Computer skills in Windows, Outlook, Excel, Word and PowerPoint
- Must have a valid driver's license with good driving record

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Western Regional Equipment Service Technician

Technica, USA, a Western regional manufacturer's representative/distributor has an opening for an equipment service technician covering the Western USA, including but not limited to, California, Oregon, Washington, Utah, Colorado, and Arizona. The position will be responsible for servicing our PCB fabrication equipment product line, including installation, troubleshooting, repair service, rebuild service, etc. This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Key responsibilities are to install and service equipment, conduct equipment audit, and provide technical service when appropriate to solve problems.

Required Skills:

- 2+ years of experience in a PCB manufacturing environment or similar
- Willing to travel
- Positive "whatever it takes" attitude while operating under pressure
- Self-motivated self-starter with the ability to initiate action plans
- Ability to work independently with a strong commitment to customer satisfaction
- Excellent communication and interpersonal skills
- Strong ability to use all resources available to find solutions
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  - Quantity and delivery requirements
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  - Philosophies and finance
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- Planning job travelers based on job release, customer purchasing order, drawings and data files and file upon completion
- Contacting customer for any discrepancies found in data during planning and CAM stage
- Consulting with director of engineering regarding technical difficulties raised by particular jobs
- Informing production manager of special material requirements and quick-turn scheduling
- Generating job material requirement slip and verify with shear clerk materials availability
- Maintaining and updating customer revisions of specifications, drawings, etc.
- Acting as point of contact for customer technical inquiries

Candidate should have knowledge of PCB specifications and fabrication techniques. They should also possess good communication and interpersonal skills for interfacing with customers. Math and technical skills are a must as well as the ability to use office equipment including computers, printers, scanners, etc.

This position requires 3 years of experience in PCB planning and a high school level or higher education.

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Recent Highlights from PCB007

1 Weiner's World—June 2017

On the return from Hong Kong last week I had the good fortune of meeting an officer of Allegro Microsystems and enjoyed a wide-ranging discussion with him. One of the "take home" items was concern about an expanding shortage of rare earth metals used to make ICs for the burgeoning automotive sensor market.

2 Mr. Laminate Tells All: PTFE is about to be Banned by IEC TC111

Technical Committee 111 of the International Electrotechnical Commission (IEC) is preparing to effectively ban PTFE (polytetrafluoroethylene) materials from electronics. As history goes, the electronics industry has focused on only two of the four halogens (bromine and chlorine) to be limited to be called "halogen-free" or more accurately "low-halogen."

3 EPTE Newsletter: Transparent Flex Circuits, Stretchable Flex Circuits

Most of the products on display at the JPCA Show were related to electronics, the electronics industry, packaging and electronic circuits. Flex circuit manufacture and material companies that featured flexible circuits at the exhibition focused their attention on transparent flex circuits and stretchable flex circuits.

4 One World, One Industry: Three Ways to Close the Skills Gap in U.S. Manufacturing

The skills gap is a chronic problem in the manufacturing sector. Most manufacturing companies have a hard time aligning the talent needed to run their businesses with the talent that is available to work locally. And as new innovations emerge, new skills requirements emerge as well.

5 All About Flex: Etchback on Type 3 and Type 4 Flexible Circuits

Through-hole etchback is a requirement that is sometimes specified on medical, military and aerospace procurement documents for multilayer flexible circuits and combination multilayer flex/rigid board circuits. It specifically relates to the copper plated through-holes and the relative dimensions between the dielectric layers and copper layers.

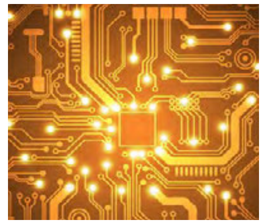
6 Happy's Essential Skills: Tip of the Month—The NIST/SEMATECH e-Handbook of Statistical Methods

In the 1990s, the National Bureau of Standards was distributing a popular statistical document, Handbook 91. A request by Patrick Spagon of the Statistical Methods Group of SEMATECH to update the NBS Handbook 91, Experimental Statistics, has resulted in a new web-based statistical handbook including statistical software.

7 The Significance of the PCB in the Value Chain of the European EMS Industry

At SMT Nuremberg, Pete Starkey meets with Dieter Weiss, who comments upon the significance of the PCB in the value chain of the European EMS industry, and looks to a future where we embrace an open-minded attitude and a willingness to work together.

8 Megasonic Acoustic Surface Treatment Process for Enhanced Copper Electrodeposition in Via Interconnects



A printed circuit board is populated with a multitude of electro-mechanical components plus various active and passive devices such as transistors, capacitors, inductors and resistors, which enable the functionality and assembly of the PCB.

9 Review of the 2017 IPC Reliability Forum

IPC continues to lead our industry by example with their inaugural Reliability Forum, held in Chicago in April. The event was focused on manufacturing high-performance products and featured industry royalty from both a speaker and audience standpoint.

10 Jill Scadden Joins Advanced Circuits as Business Development Manager

Advanced Circuits welcomes Jill Scadden as business development manager. She will be responsible for discovering new business opportunities and enhancing Advanced Circuits' offerings by working closely with customers and prospects to create customized solutions for their unique PCB fabrication needs.

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Events

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August 9–10, 2017
Denver, Colorado, USA

NEPCON South China 2017
August 29–31, 2017
Shenzhen, China

24th FED Conference
September 15–16, 2017
Bonn, Germany

SMTA International 2017 Conference and Exhibition
(IPC Fall Committee meetings held in conjuction with SMTAI)
September 17–21, 2017
Rosemont, Illinois, USA

IPC Fall Standards Development Meetings
September 16–21, 2017
Rosemont, Illinois, USA

electronicAsia
October 13–16, 2017
Hong Kong

IPC Flexible Circuits: HDI Forum
October 17–19, 2017
Minneapolis, Minnesota, USA

TPCA Show 2017
October 25–27, 2017
Taipei, Taiwan

productronica 2017
(IPC Committee meetings held in conjuction with productronica)
November 14–17, 2017
Munich, Germany

HKPCA/IPC International Printed Circuit & South China Fair
December 6–8, 2017
Shenzhen, China

47th NEPCON JAPAN
January 17–19, 2018
Tokyo Big Sight, Japan

DesignCon 2017
January 30–February 1, 2018
Santa Clara, California, USA

EIPC 2018 Winter Conference
February 1–2, 2018
Lyon, France

IPC APEX EXPO 2018 Conference and Exhibition
February 27–March 1, 2018
San Diego, California, USA

KPCA Show 2018
April 24–26, 2018
Kintex, South Korea

Medical Electronics Symposium 2018
May 16–18, 2018
Dallas, Texas, USA

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Signal Integrity and Controlled Impedance
Why these are critical to PCB manufacturers

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Today, tomorrow and the future