I-Connect007
GOOD FOR THE INDUSTRY

ENGINEERING SOLUTIONS FOR PCB MANUFACTURING

SMT® MAGAZINE

SEPTEMBER 2017

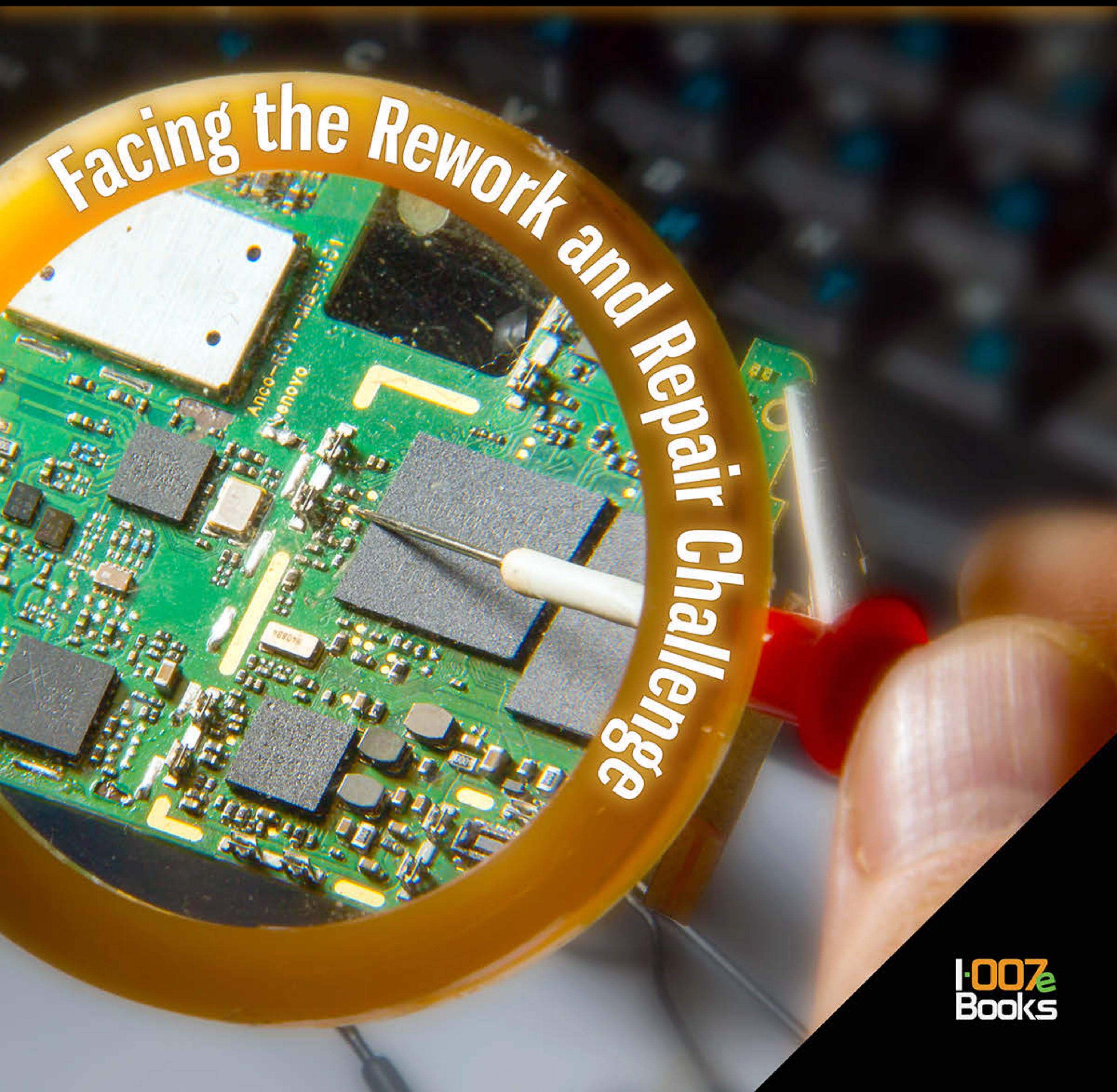
A Look into PCBA Rework and Repair p.12

BTC and SMT Rework Challenges p.36

Rework and Reball Challenges for Wafer-Level Packages p.50

Much More!

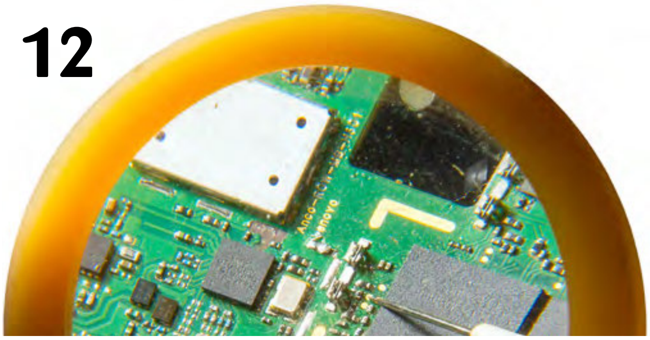
Facing the Rework and Repair Challenge

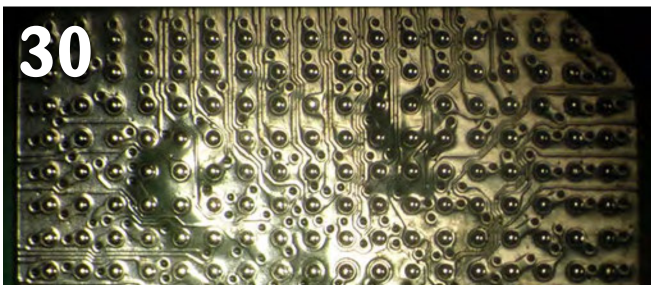


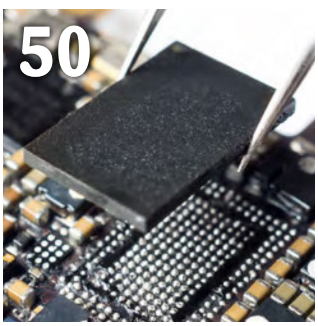

quick
QUOTE
POWERED BY
PCBNET.COM

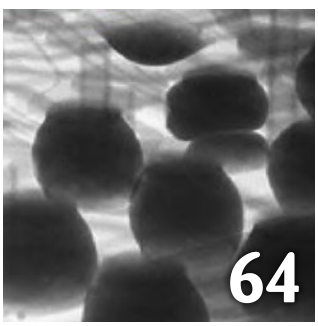
SMT MAGAZINE

September 2017 • Featured Content









Rework & Repair

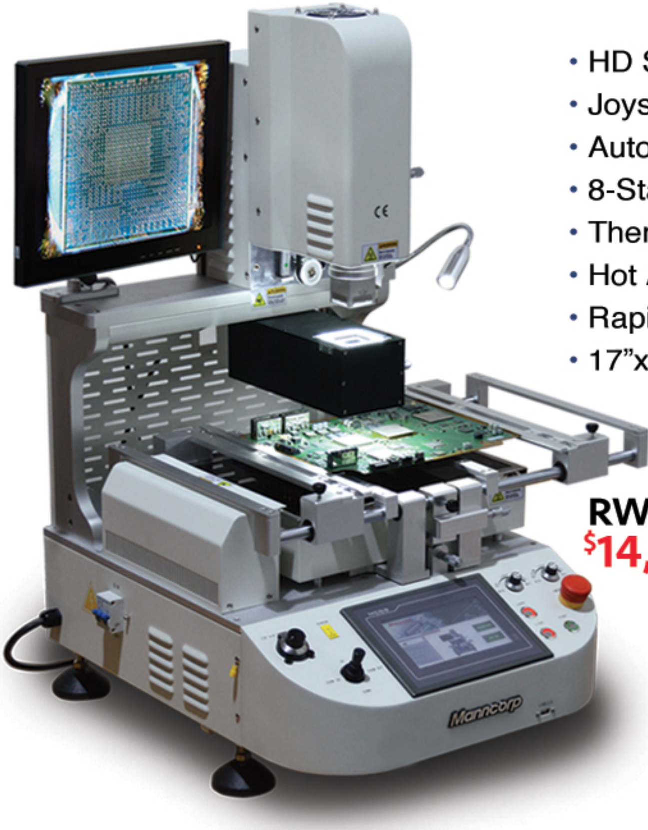
This month, *SMT Magazine* looks into the many challenges associated with rework and repair of PCB assemblies, and highlights strategies to improve the process.

FEATURE COLUMNS

The SMT Source™ Latest News About Manncorp SMT Assembly Equipment Sept. 2017

REWORK VALUE REDEFINED

Tackle Any SMT Repair Application...FOR LESS!



- HD Split-Vision for BGA/QFPs
- Joystick-Controlled Zoom
- Auto Remove, Place, Solder
- 8-Stage Top/Bottom Heating
- Thermocouple Input/Control
- Hot Air Flow Control
- Rapid IR Underheater
- 17"x 14.25" PCB Capacity

RW1210
$14,995

RW1500
$29,995

- 21.6"x 18.5" PCB Capacity
- Easy X-Y Heater Positioning
- Multiple Repairs w/ Single Setup No PCB Repositioning Needed
- 4 Thermocouple Inputs
- 01005 & Nitrogen Capability
- HD Side-Viewing Camera
- All Other Features of RW1210

FREE SHIPPING & INSTALLATION

Special Offer Thru September 30, 2017 - U.S. Only

Text or Call
Chris - East: 215.869.8374
Ed - West: 215.808.6266

Manncorp™
www.manncorp.com

Email
sales@manncorp.com

Huntingdon Valley, PA • San Diego, CA • Mexico • China

Improving the Rework Process

by Stephen Las Marias
I-CONNECT007

An optimized SMT assembly process typically provides a yield of nearly 100%. Technology advancements—from the solder paste printing process, SPI, and parts placement, to reflow and wave soldering and AOI—have pushed the efficiency and accuracy of these steps in the SMT process such that a board assembly should be perfect at the end of the line.

Still, EMS providers continually face the need to rework and repair PCBAs even after dialing in the perfect set-up; there will always be that insufficient solder, or excessive solder, or missing component on the board, among other issues. Chief among them is the continuous trend toward miniaturization in the industry—the ever-shrinking component sizes being placed and soldered onto boards with finer and finer pitch and spacing—which is putting a lot of pressure even in the rework and repair of such boards.

Also, with reliability being one of the top customer requirements, touching boards should be avoided because it increases the chances for damage, such as flexure or shearing of parts with the soldering iron on the back or front side, according to Gary Freedman, of Colab Engineering. He notes that every time a board passes through a repair cycle, that board will be of lesser reliability.

You need rework—there will always be a need for rework—but the more you do rework, the more touches a PCBA receives, the higher the chance its reliability decreases. What a Catch-22 situation.

For this month's issue of *SMT Magazine,* we talked with BEST Inc.'s Dan Patten and Laura Ripoli, Circuit Technology Center's Andy Price, and Freedman to find out more about the critical challenges in rework and repair of PCB assemblies, and which strategies to implement to improve the process and ensure the reliability of the boards.

Interestingly, one of the things they pointed out is the skills of the operators or technicians doing the rework. In the words of Andy Price, they should have "a tremendous amount of experience, hand skills, the ability to work using magnification for hours on end, knowledge, and patience." The skillset, according to him, is just not on the market, so you must find somebody with the right mindset and right capability to do the job. Once they are inside your doors, continuous training is required. You will find out more about that discussion inside.

Also on hand this month is an article from Joerg Nolte of Ersa GmbH, discussing BTC and SMT rework challenges.

In her feature article, Karen Tellefsen of Alpha Assembly Solutions explains why less rework equates to more reliability.

BEST Inc.'s Bob Wettermann provides his view of the top five BGA rework challenges to overcome. Also, in his column for this month,

Wettermann talks about the need for baking out PCBAs post-cleaning and after rework has taken place.

Still on the rework topic, we have an article from Intel Corp.'s Lauren Cummings and Priyanka Dobriyal, discussing rework and reball challenges for wafer-level packages.

David Prunier of MC Assembly relates why a successful capacity planning model should be a part of a company's sales and operations planning system.

Finally, I interviewed David Bergman of IPC to find out more about how the organization helps elevate the industry through its training, continuous education, and standards development.

By the way, our team at I-Connect007 will be at Rosemont, Illinois, this month for SMTA International. We'd love to talk to you about your latest technologies and innovations, so just drop us a note to schedule a meeting, or drop by our booth.

We will also be at productronica in November. Let's start planning our meetings, shall we?

I hope you enjoy this month's issue of *SMT Magazine*. Next month, we will talk about the perfect solder joint. Stay tuned! **SMT**

Stephen Las Marias is managing editor of *SMT Magazine*. He has been a technology editor for more than 12 years covering electronics, components, and industrial automation systems.

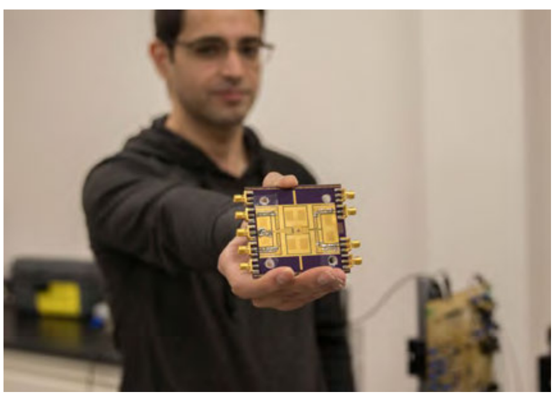
High-Frequency Chip Brings Researchers Closer to Next Generation Technology

A novel, high-frequency electronic chip potentially capable of transmitting tens of gigabits of data per second has been developed by engineers at the University of California, Davis.

Omeed Momeni, an assistant professor of electrical and computer engineering at UC Davis, and doctoral student Hossein Jalili designed the chip using a phased array antenna system. Phased array systems funnel the energy from multiple sources into a single beam that can be narrowly steered and directed to a specific location.

The chip successfully operates at 370 GHz with 52 GHz of bandwidth. For comparison, FM radio waves broadcast between 87.5 and 108 MHz; 4G and LTE cellular networks generally function between 800 MHz and 2.6 GHz with up to 20 MHz of bandwidth.

Most modern electronics are designed to operate at lower frequencies. However, the growing demand for faster communication, and new and emerging applications of sensing and imaging are driving the creation of technologies that function at higher frequencies.

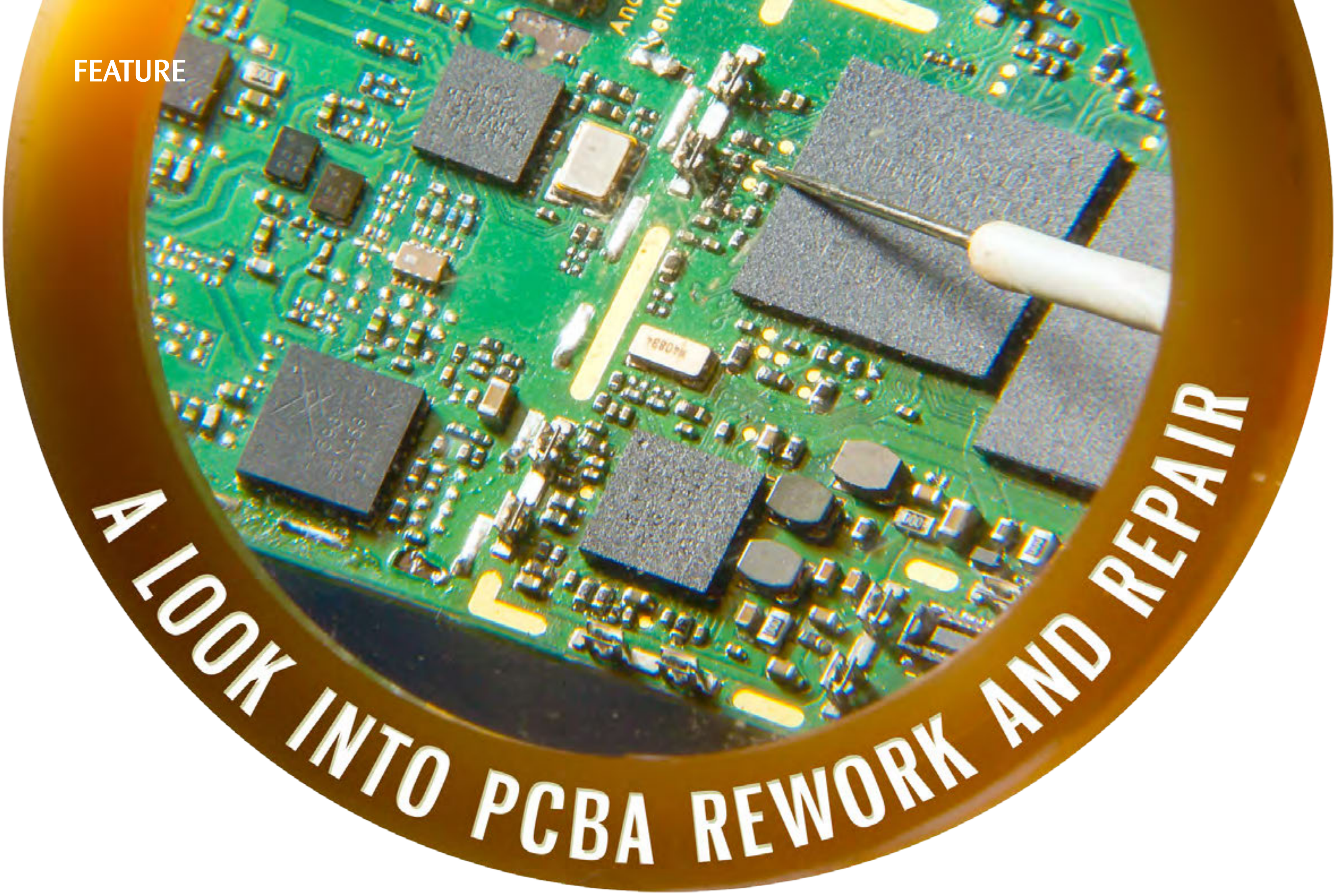


"Theoretically, 4G cellular networks have reached their data rate limit," Momeni said. "As we continue to migrate to systems like cloud computing and next generation cellular networks, the need for speed is growing. Higher frequencies mean more bandwidth and more bandwidth means higher data rate."

The tiny piece of hardware designed by Momeni and Jalili is evidence that it is possible to harness the large available bandwidth at millimeter-wave and terahertz bands on a single, compact chip. This is an important step toward the development of scalable systems that can be used to sharpen technologies like spectroscopy, sensing, radar, medical imaging and high-speed communication.

In future work, Momeni plans to integrate the chip into imaging and communication systems.

FEATURE



A LOOK INTO PCBA REWORK AND REPAIR

by Stephen Las Marias
I-Connect007

Despite the many technology advances in the SMT process, there will always be a need for rework and repair of PCB assemblies. Most especially as the industry trend continues towards finer pitch and spacing, smaller and smaller components, and increasing high-reliability requirements from customers.

Not to mention that fact that the rework and repair processes are already challenging. You have to deal with already-finished boards, wherein improper soldering may cause collateral damage to around the area that needs rework.

So, for this month's issue of SMT Magazine, we interviewed Dan Patten, general manager, and Laura Ripoli, customer service manager for rework/repair, from BEST Inc.; Gary Freedman, president of Colab Engineering; and Andy Price, sales manager of Circuit Technology Center, to know more about the rework and repair of PCB assemblies, the critical challenges, and strategies to improve the process moving forward.

The Challenges

"We're always making more densely populated boards and we're making things smaller and packing more into it and so forth," says Patten.

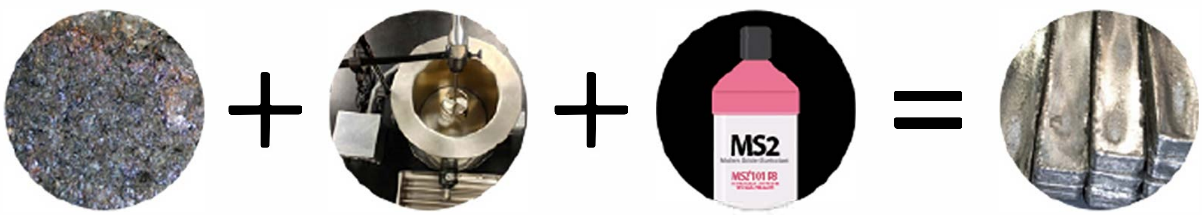
Price notes, "From our perspective, some of the most challenging issues that we confront daily tie in with the circuit board design. The spacing is tighter, the boards are thicker and contain heavy copper planes. Those factors along with the RoHS requirements help create many of the challenging issues that we face in trying to rework components. It also increases the challenge in getting complete solder fill in plated holes. Much of it is directly related to the circuit board design. Some of the other factors include rework and repair on boards that have gone through final processing. They may be field returns or failures that are found after conformal coating application, or through the under-fill process at BGA component sites. There's are many problems that can arise when reworking boards with conformal coating. Often collateral issues to adjacent components can oc-

Do you use High-Volume Wave Solder Machines?

Is dross a major financial headache?

DON'T RECYCLE DROSS FOR PENNIES ON THE DOLLAR, YUAN, WON, YEN, EURO, RUPEE, ETC...

Use MS2 to turn your dross into reusable solder bars and start saving money today!



SOLDER DROSS — MELTING POT & BAR MOLD — MS2 — BARS OF NEW SOLDER

Watch the process online…

MS2® can reduce solder usage by 60 – 85% while also offering additional benefits to the manufacturing process.

PK METAL

For more information, contact us at:

sales@pkaymetal.com +323-585-5058 pkaymetal.com

cur if the area is not prepared properly such as starved solder joints, solder shorts and other problems. Those are just a few general thoughts on some rework issues we confront."

Price notes that board thickness is a challenge. "Years ago, board thicknesses ranged from maybe 0.062" to 0.092". Now, we're routinely seeing boards that are 0.125", and even thicker. There are ground planes involved in the construction of these boards that dissipate heat when you're trying to remove components. Then you add in the fact that you're dealing with a higher temperature reflow with RoHS requirements. These are just challenges that we have to deal with. I don't see it going away. I see it becoming more and more challenging," he explains. "The prevalent issues that we see with circuit boards that are constructed like that relate to the increased heating requirement. Boards require preheating and complete bake-out prior to rework. A lot more heat is needed in the rework area to achieve reflow temperatures. When more heat is necessary you increase the potential for physical damage to the board to occur. You may see baseboard discoloration or more significant base board damage such as delamination. Increased heat at the rework site can also result in lifted lands, surface mount pads and pulled plated through hole barrels. These are issues that anybody involved in rework will see, the most expert companies will see less of it due to experience but there are some designs that are very difficult to overcome."

Dan Patten

One of the problems that Freedman had seen very often was trying to repair things that don't need repair on boards, such as barrel fill that doesn't quite meet IPC spec. "One of the things that I had been driving for years when I was with Digital, Compaq and HP was trying to refine the barrel fill specifications. We have had some success in driving that movement with IPC. If you look at a through-hole solder joint, it's many times stronger than an SMT solder joint. Yet, we're happy to pass SMT solder joints with very little solder. When it comes to through-hole, people are so quick to take a soldering iron to it. It might just be the wrong thing to do," he points out. "What we want to do is minimize the number of heat cycles on a circuit board. Besides the number of heat cycles, we also want to minimize the number of touches. Any time you touch a board, you're likely to damage it, either through flexure or shearing of parts on the back side, or on the front side, with the soldering iron. Or, I see operators with picks all the time, poking and prodding to see if things are soldered. Like I said, anytime you can minimize the number of touches to a board, you're better off. I'm one that is much happier to pass a board that doesn't quite meet IPC than to have it go through a repair cycle. Chances are, the repaired board will be of a lesser reliability.

"A through-hole solder joint is many times stronger than a surface mount solder joint. We get very particular about these massively strong solder joints and yet we're very willing to pass SMT solder joints that have almost no solder. I certainly understand that there are different mechanics involved in expansion of contraction, etc. We turn a blind eye to SMT, whereas with through-hole we get overly particular. I said that there are two issues: number one is the number of heat cycles we apply to a solder joint. That, in part, defines intermetallic characteristics and reliability. The other thing is the number of touches to a board. Any time a board is subjected to rework, you're more apt to create damage than if the board is left alone."

For years, Freedman had done a lot of work on reliability of solder joints, including through-hole solder joints, as well as a lot of modeling and testing of solder joints to revise their specification requirements and to also influence IPC. "And we have done that to some degree," he says. "If you have a very thin board, IPC's very happy with a minimum amount of solder joint. If you have a thick board, they want a very thick solder joint, and yet, if you do the modeling and the reliability testing, you'll find that even a 20% solder joint in a thick board has more than enough reliability. I'm not advocating that we go down to 20%, but I'm saying let's get real about what's actually required. I think we need to move out of the middle ages of soldering in terms of through-hole and consider doing more work in terms of modeling and reliability of the through-hole joint specification."

"On a through-hole board, that's certainly the most common problem that we have in terms of soldering," continues Freedman. "The barrel fill is always an issue. I dealt with very thick boards for a very long time; server boards and telecom boards that are well in excess of 0.093". They're just a bear to repair in all regards. The first thing that is spotted generally for repair is the through-hole solder joint itself. We see nice barrel fill on the signals, of course, and marginal solder joints on powers and grounds. Those are always seeing touches. We have operators calling that out because of either visual or X-ray results, and trying to fill things that are already more than strong enough to last the lifetime of the product."

Ripoli says they quite often find that people who are trying to remove things from the board—especially bottom termination components—and don't have the proper equipment to do that, tend to rip up pads on the boards. "It ends up in our hands to do pad repairs as well as placing that BGA back down. We have people with over 20 years of experience dealing with those types of repairs," she notes.

Laura Ripoli

The majority of BEST's rework and repair involves bottom termination components, says Patten.

"More so than the through-hole," adds Ripoli. "Definitely, the QFNs, LGAs, BGAs are a large percentage of the work we do. We see a lot of those coming in with excessive solder voiding or solder shorts."

Price agrees that bottom termination devices are the most prevalent rework requirement. "Often, what drives larger quantities of component rework, is when there's some issue with a component, whether the manufacturer has determined there's a bad date code on a component that is populated on hundreds or thousands of boards that needs to be reworked, or there are other issues such as mixed chemistry. An example would be a RoHS lead-free component placed into a leaded soldering process, therefore it doesn't get to proper reflow temperatures. There are a variety of things that drive large quantity rework applications like that. By and large, BGA, LGA and QFN rework is very challenging to anybody. The rework itself is difficult, as is the inspection process. There's not a lot of trained eyes that can examine and understand and look at an X-ray with certainty when it comes to 'head in pillow,' or 'solder open' and other defects, it is very challenging.

"I would say that is probably the most challenging rework application out there for the general population of contract manufacturers that are doing rework in-house, especially when you get into the board designs mentioned earlier with increased thickness of boards and tighter spacing of adjacent components. Preventing collateral issues when you're doing a hot air rework is difficult, the hot air doesn't want to stay where it is directed, it wants to spread out, and it does. It will spread out through the board and it will spread out to adjacent components and it will create conditions outside of the target zone that is called collateral damage. Overheating adjacent component, reflowing solder joints and other issues can occur. Add the conformal coating element to it and under fill at that particular rework site, well, now you've elevated the degree of difficulty to the rework application. It is extremely difficult to have 100% success rate with all of those factors."

When it comes to solder voiding, Ripoli says there are many things that can contribute to that issue: one being the customer using mixed alloys when assembling a board. "We'll find evidence of that going on. It could be that the paste is not the right thickness. It could be the profile on the original assembly that's causing the issue. To fix the problem, it's back to the customers to figure out what step in their process is causing an issue," she says.

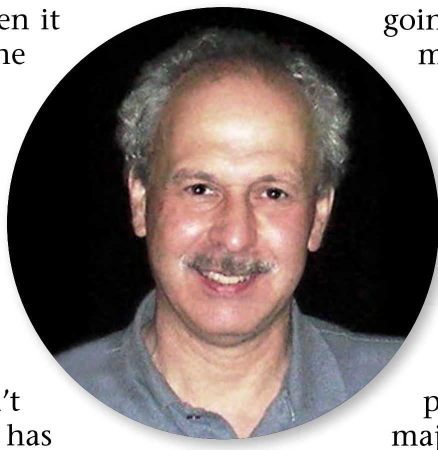
"They're more likely to have the data or the tribal knowledge and the cause of the problem and we might just be able to have the equivalent expertise to solve the problem," says Patten. "We don't always get involved in a recommendation. Sometimes, we do and we certainly can, but to learn that entire process for that build and the profiles and so forth doesn't always go through our hands."

"We have some customers that work with us while they're doing their proto stage of assembly," says Ripoli. "They'll come back to us and send us a board with connectors and have us measure the solder fill percentage, the X-ray. We'll give them that feedback, they'll go back and make changes to their process, send us another batch of boards, and we go through that same process again until they can tweak and find the right solutions to getting that proper fill."

One of the biggest issues when it comes to rework and repair is the temperature cycles.

"The problem is when you have to rework something, it has to go through four or six cycles of heat or something like that. Then it's a problem and they didn't predict that. Nobody predicts reworks on their boards," says Price.

"Not only that, but you won't necessarily know that the board has been repaired multiple times before it gets to you," says Patten.


Gary Freedman

Most of the time, the rework specialists will never find out how many times a customer—the contract manufacturer/PCB assembler—touched the product before they get it. "It is a big mystery," says Patten, "and it's often a cause of unpredictable failures."

But some PCB assemblers/contract manufacturers do track the number of rework/repair cycle that a board goes through.

"When we get larger quantities of rework or repair, we don't see that as often; but when we have the one really special custom board, we get that a lot. They tried and they failed, so they give it to us. We don't know what they've tried or how they failed. We don't get that history usually," says Patten.

Key Considerations

When someone's looking at their rework strategy, what are the important considerations that they should be mindful of? According to Price, it starts with the skill of the operator.

"The folks that you have doing the work must have a tremendous amount of experience, hand skills, the ability to work using magnification for hours on end, knowledge, patience; everything ties in with the operator doing the job. When it comes to rework and repair, every board can be a little bit different. When reworking and repairing circuit boards, the operator must be reading the board all the way through the process. That's why the procedures that you look for repair are fairly generic in nature because you just can't create a procedure that identifies every subtlety that you're going to confront along the way. In my opinion, it starts with the operator and the need to have a well-trained, highly skilled operator doing the work. Secondly, having good modern equipment and tools that allow your skilled operator to succeed. [For example] A soldering station that can drive heat into a board very quickly. Having the proper tools and equipment is a major requirement," Price explains.

"I'll tag onto that," says Patten. "Just as much as I want to sell more training, and I believe in high training, a certification is not enough. It's the experience of the hundreds of situations. You can't have a week of a training class. Sharp mind, sharp tools, and a ton of experience. Finding those people, they're diamonds, they're very hard to find."

He adds that you can train thousands of people, but only one or two of them are really going to be a long-term high-end tech.

Automation in Rework

Will there be some form of automation coming in to replace an element in rework/repair?

"Replace is a strong word," Patten says. "But to assist, for sure; [but] not replace." Still, it will not eliminate the need for all those years of experience.

According to Patten, it will require the operator to have even more experience. Although it will allow them to do higher quantities of rework/repair. "You might have some pick and place type, not for a bare board but for a populated board or touchless removable solder, different things like that. You still need the highly skilled, highly trained tech to run it. With the fight of keeping rework costs as low as possible, and to keep a tech in such a glamorous position at the rates that they would require at that position, is challenging."

How to find such people? Most of the time, the same people with previous contract manufacturing experience.

"We have a work force that has been with us for many years," says Price. "People retire and you have to draw from the talent base that's in the area. We're not recruiting from across the country, so we're drawing from people that have previous contract manufacturing experience who have worked at a bench. Then, it's incumbent upon us to focus their efforts in certain areas to get them started so they're able to help us in certain ways. Then just expand their exposure to different things. It takes more than a couple of weeks, believe me. It's a long-term training cycle."


Andy Price

"The skillset is just not on the market so we have to find somebody with the right mindset and the right capability, and bring them in. But maybe not experience, so that we can train them."

The Future of Rework/Repair

The trend toward miniaturization continues to pressure the electronics manufacturing industry to create products with finer pitch and spacing. Where does this lead the rework/repair process?

"We have been approaching the limits of what we can repair for the last 20 years," says Patten. "So, we'll continue to evolve as they keep getting smaller. But, wow, we are really small, 2mm packages, 40mil balls are very difficult to work with."

"Sometimes it's a matter of context," explains Freedman. "Some of the packages we use routinely can be put down easily and repeatedly if the board is designed for it. Going back to a server board for instance, you have micro BGAs and you have a lot of through-hole devices and thick power and ground planes which complicates the matter. If I had a board that was nothing but QFNs, I could probably come up with a formula to do that all day and all night with no issues at all. When you have other things in the context of the board, that's what makes it difficult. If we were to reduce reliance on through-hole devices, that would go a long way to helping things out. A couple other things that I'd like to mention is that one of the things that I've seen done very poorly in the original assembly and in repair is thermal profiling. I don't see people taking the time or expending materials to do a thermal profile for initial assembly of the board or for its repair. I see people winging it on both sides."

"I want to make a point of that," says Patten. "They don't want to spend the time or the money to test it and make sure that the repair goes right. They're winging it."

"Yet, another thing on my list is automated or semi-automated repair methods," says Freedman. "I hate to see people taking handheld hot air tools to boards; it's such an uncontrollable process. You don't know what you're getting; you don't know what damage you're doing to the board, to the joints, to the things around it. I like to see more controlled methods and metrology so that we know what temperatures are being reached locally, and what's going on with the board. With a programmable

Are these villains wreaking havoc on your processes?
RESIDUE
OXIDE
ELECTRA MIGRATION
ICICLES
Then you need
PROJECT99
WAVE SOLDER FLUXES
Email: Project99@indium.com
Learn more: indium.com/99/SMTUS
TO BE CONTINUED...
INDIUM CORPORATION®
©2017 Indium Corporation

hot air repair machine, you can set up a proper profile, and know what the impact is to the rest of the board. Soldering iron for repair? If possible stay away from it. I know you can't always. Also, I see people hanging boards over solder fountains for extended periods of time, I don't like that. I see people reballing components that aren't spec'ed for reballing. There are just so many areas in rework that are detrimental to the reliability of the board."

So how to ensure the reliability of the boards after rework or repair was done to them?

"There are standards that you have to meet when it comes to rework," explains Price. "Just like if you're assembling a circuit board, there's an acceptability standard that you work to. Typically, when meeting those standards, then your rework activity can be considered reliable. There are also various inspection steps, such as X-ray and in-process visual inspection that are completed to ensure the rework steps are completed and to confirm reliability. In regard to repair, within each repair procedure in the IPC-7711/7721 that we follow there are tests and verification steps that need to be completed. For example, it would include a metering step to verify proper connection when repairing a missing surface mount pad." SMT

Stretchable Biofuel Cells Extract Energy from Sweat to Power Wearable Devices

A team of engineers has developed stretchable fuel cells that extract energy from sweat and are capable of powering electronics, such as LEDs and Bluetooth radios. The biofuel cells generate 10 times more power per surface area than any existing wearable biofuel cells. The devices could be used to power a range of wearable devices.

The epidermal biofuel cells are a major breakthrough in the field. Engineers from the University of California, San Diego, were able to achieve this, thanks to a combination of clever chemistry, advanced materials and electronic interfaces. This allowed them to build a stretchable electronic foundation by using lithography and by using screen-printing to make 3D carbon nanotube-based cathode and anode arrays.

The biofuel cells are equipped with an enzyme that oxidizes the lactic acid present in human sweat to generate current. This turns the sweat into a source of power.

The engineers reported their results in the June issue of Energy & Environmental Science. In the paper, they describe how they connected the biofuel cells to a custom-made circuit board and demonstrated the device was able to power an LED while a person wearing it exercised on a stationary bike.

Professor Joseph Wang, who directs the Center for Wearable Sensors at UC San Diego, led the research, in collaboration with electrical engineering professor and center co-director Patrick Mercier and nanoengineering professor Sheng Xu, both also at the Jacobs School of Engineering at UC San Diego.

Rework and Reliability: Less is More!

by Karen Tellefsen
ALPHA ASSEMBLY SOLUTIONS

Circuit boards are not always perfect after reflow or wave soldering. Scrapping boards with one or two defects is expensive, so rework happens. A good concept for rework is less is more, especially less flux. Use as little rework flux as possible, as in the old Brylcreem ads, "Just a little dab'll do ya."

Liquid flux for rework is often supplied in felt-tipped applicator pens that make applying a few microliters of flux to a solder joint easy. Small squeeze bottles with tiny needle tips also work well. Paste/gel flux can be supplied in small syringes; use a small applicator tip to ensure that only a small dot of flux is applied to the rework site. Of course, using only no-clean, flux-cored solder wire without any assisting flux is the most electrochemically reliable way to do no-clean rework. The core flux in the wire will be properly heat deactivated because it will not flow until the wire is melted. Additionally, because core flux is mostly rosin or resin and hard, any activator remaining will be trapped in the flux residue. No-clean core fluxes are usually light colored and glass-like in appearance, providing nice cosmetics.

Most low solids, no-clean soldering fluxes must be exposed to soldering temperatures to become deactivated. The activator systems of these fluxes contain organic acids that remove oxides and allow solder to wet. When these organic acids are exposed to high enough temperatures for a long enough time, the activators volatilize and go away. If this doesn't happen, the unheated or under-heated flux residues can

allow electrochemical failures to occur, such as corrosion, reduction of insulation resistance, and, worst of all, electrochemical migration (Figure 1). If too much flux is applied to a rework site, some of the flux can move to nearby parts of the board that will not be exposed to the heat of the soldering tool. This often happens when flux is dispensed in large squeeze bottles with coarse tips. All those spikes in the SIR of the unheated flux are caused by the formation of dendrites between conductors.

So, how do unheated flux residues (and other contaminants) allow electrochemical problems to happen? A diagram showing these failure mechanisms is given in Figure 2. Many flux residues are hygroscopic, that is they absorb moisture from the air. This forms an electrolytic film on the board. The presence of this film

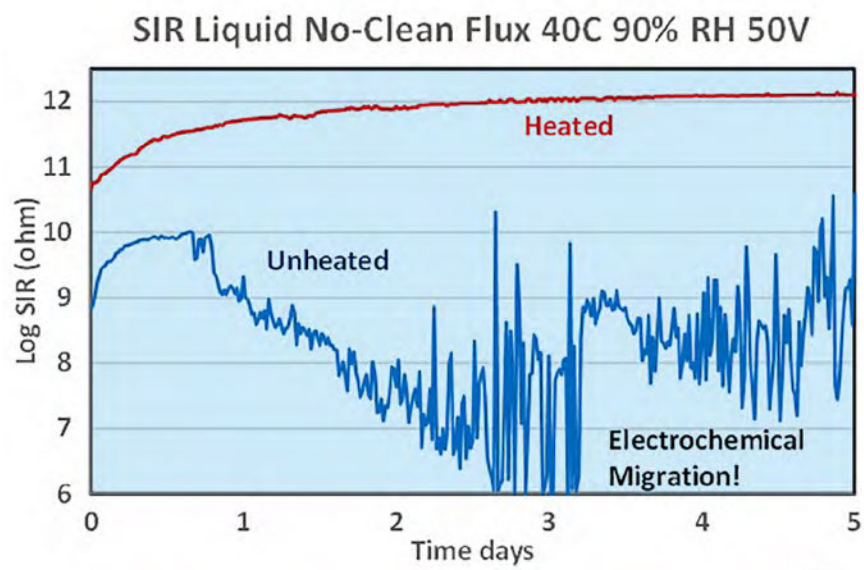


Figure 1: SIR measurement of heated and unheated liquid, low-solids, no-clean flux.

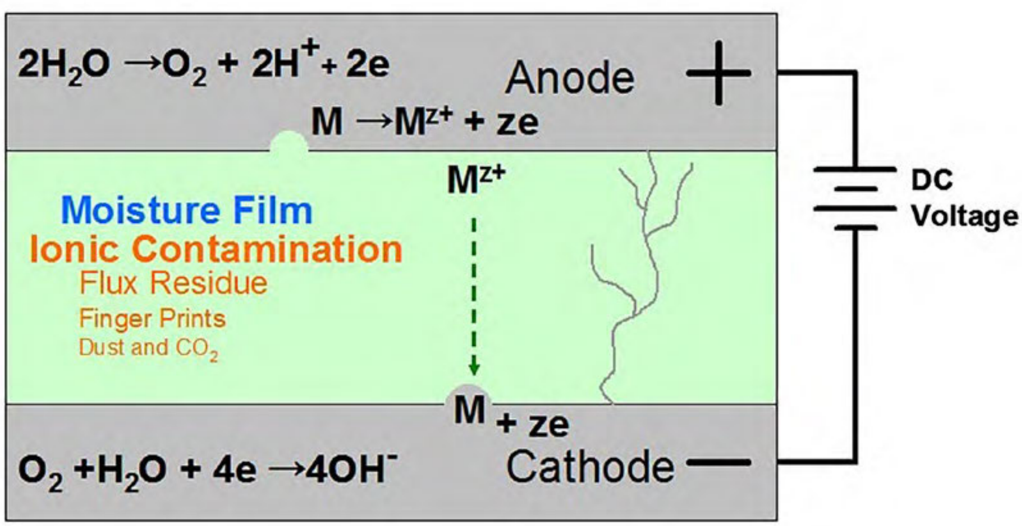
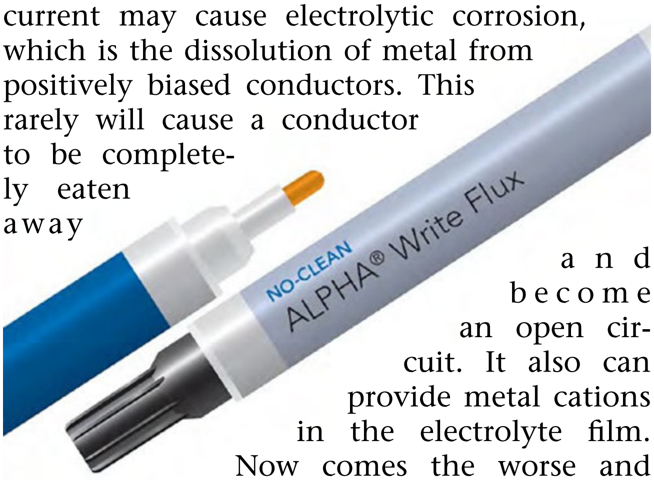


Figure 2: Electrochemical failure mechanisms caused by contaminants on circuit boards.

allows small currents to flow between conductors at different voltages, reducing the surface insulation resistance (SIR). In some cases, the small current may cause electrolytic corrosion, which is the dissolution of metal from positively biased conductors. This rarely will cause a conductor to be completely eaten away and become an open circuit. It also can provide metal cations in the electrolyte film.



Now comes the worse and most destructive failure, electrochemical migration (ECM). Those metal ions in the electrolyte film will migrate to the cathodic, or negatively bias conductor because of the electrical field between the two conductors. When the metal cation gets to the cathode, it can pick up some electrons and deposit on the conductor. This deposition will usually occur at high energy locations, causing the formation of tree-like structures called dendrites. These dendrites will grow all the way to the opposing conductor causing a short circuit. These dendrites are delicate and can be destroyed by the resistive heating current flowing though the thin conductor. Noise results from the repeated forming and breaking of the dendrites, as seen in Figure 1.

Only J-STD-004B type -L0 and -L1 fluxes should be used for no-clean rework; fluxes that contain some rosin or a similar encapsulating resin, such as ROL0 and REL1, are even better. The rosin or resin in the flux will harden and help trap activators that weren't completely heat deactivated.

Some circuit assemblers clean reworked areas with isopropyl alcohol or another solvent. For no-clean material rework, this is usually done for cosmetic reasons and more likely to hurt the electrochemical reliability than help it. No-clean fluxes are designed to be left on the circuit board. Spot cleaning may only move the dirt around. For circuits boards that are usually cleaned, spot cleaning reworked areas are not recommended. The board should be reworked with washable fluxes, and it should be put through the usual washing process again to ensure all rework fluxes are adequately removed from the board. This is especially important if the finished circuit is to be conformally coated, as coating over some flux residues can be worse than not coating at all.

In conclusion, be careful not to leave excessive or improperly heated flux residues after reworking circuit boards, or you might have more problems. **SMT**

Karen Tellefsen is a senior research chemist, R&D, for Alpha Assembly Solutions.

MilAero007 Highlights

Plexus Posts Revenue of $619M for Q3 FY2017

Plexus Corp. has announced a revenue of $619 million for the third quarter of its fiscal year ended July 1, 2017.

Benchmark Electronics Appoints Bruce Carlson to the Board

Benchmark Electronics Inc. recently appointed retired Air Force General Bruce Carlson to the company's board of directors.

Universal Electronics Strengthens Manufacturing Capabilities

Universal Electronics Inc. (UEI) has increased its RoHS-compliant PCB and higher-level assembly electronics manufacturing capabilities with the addition of new capital equipment for its manufacturing facilities in Whitewater and East Troy, Wisconsin.

IPC Welcomes Exec Order on Strengthening the U.S. Defense Industrial Base

President Donald Trump recently signed an executive order on "Assessing and Strengthening the Manufacturing and Defense Industrial Base and Supply Chain Resiliency of the United States."

Digicom Electronics Receives AS9100:2016 (RevD) and ISO 9001:2015 Certifications

Digicom Electronics Inc. has been certified by Intertek for AS9100:2016 (RevD) and ISO 9001:2015.

Zentech Introduces Overmolded Cable Assemblies

Zentech has added overmolded cable assembly manufacturing to its robust resume of capabilities.

Celestica Reports Q2 2017 Revenue of $1.56B

Celestica Inc. has reported revenue of $1.56 billion for the second quarter ended June 30, 2017, up by 5% compared to the second quarter of 2016.

CTS Posts Q2 Sales of $105.7M

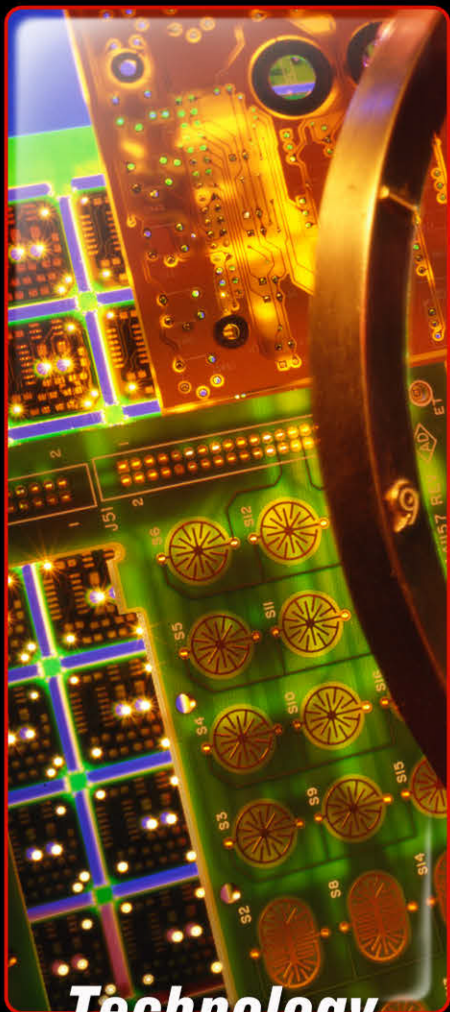
CTS Corporation has reported second quarter sales of $105.7 million, up by 7.1% year-over-year.

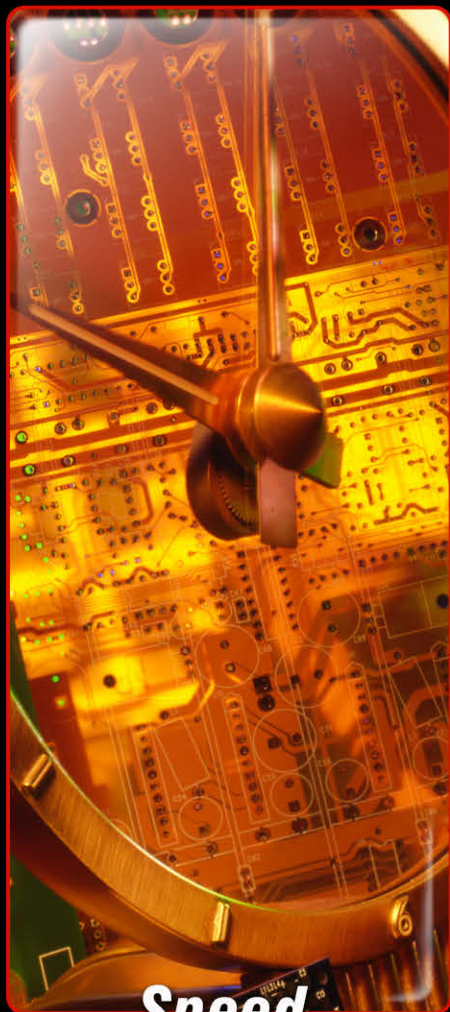
Libra Industries Names Matt Tringhese Director of Program Manufacturing

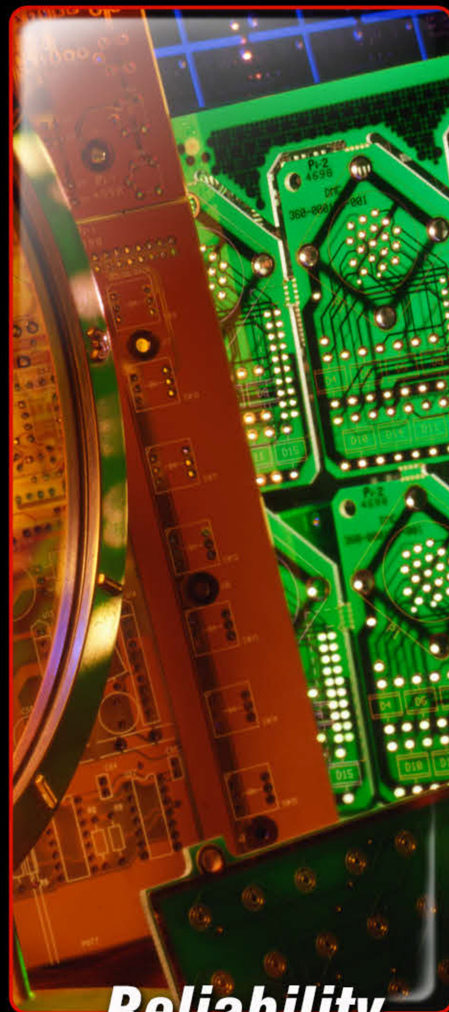
Libra Industries has promoted Matt Tringhese to Director of Manufacturing. Tringhese started out as Libra Industries' production supervisor for second shift back in 2012.

Congressman John R. Carter Discusses Pro-Manufacturing Policies with VirTex

IPC member company VirTex recently held a town-hall-style discussion with Congressman John R. Carter (R-TX-13) on the legislative issues impacting the manufacturing industry.





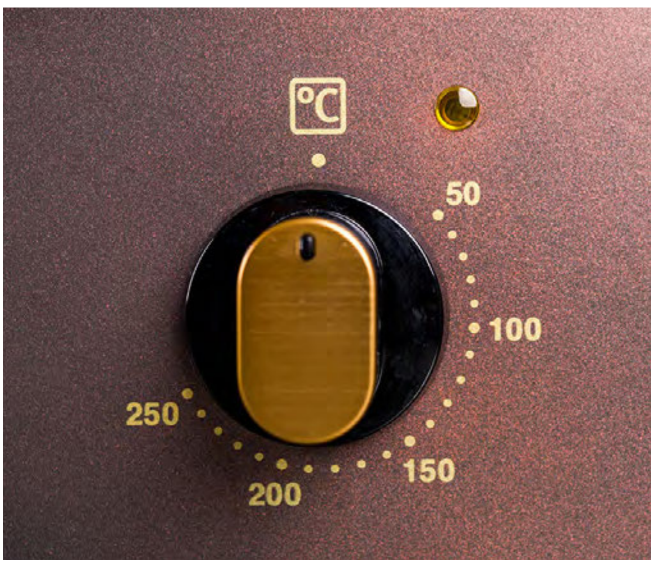


Drying Boards after Rework Cleaning—To Do or Not to Do?

by Bob Wettermann
BEST INC.

As electronic components continue to get thinner, issues related to moisture sensitivity will continue to be front-and-center for electronic assemblies being reworked. In cases where water soluble fluxes are being used in the rework process, in cases where the components (i.e., like in the BGA reballing process) need to have flux residues washed off or in cases where the board needs to be cleaned with water for subsequent conformal coating touchup, proper drying and perhaps even bake out procedures need to be performed. This will properly protect the components from moisture ingress and subsequent damage

There are a variety of factors that influence the need for baking out a printed circuit board post cleaning and after rework has taken place. In the process of diffusion, the amount of time and in what type of environment the board is in determines the maximum allowable "floor time" or open time the board can be in without baking. IPC-1601 will provide guidance for the proper handling, the correct packaging materials and methods, environmental conditions,



Pkg Thickness	MSL	Bake @ 125C		Bake @ 90C/<=5%RH		Bake @ 40C/<=5%RH	
		Saturated @ 30C/85%	@ Floor Life Limit + 72H @ 30C/60%	Saturated @ 30C/85%	@ Floor Life Limit + 72H @ 30C/60%	Saturated @ 30C/85%	@ Floor Life Limit + 72 H @ 30C/60%
<= 1.4 mm	2a	5 H	3 H	17 H	11 H	8 D	5 D
	3	9 H	7 H	33 H	23 H	13 D	9 D
	4	11 H	7 H	37 H	23 H	15 D	9 D
	5	12 H	7 H	41 H	24 H	17 D	10 D
	5a	16 H	10 H	54 H	24 H	22 D	10 D
<= 2.0 mm	2a	21 H	16 H	3 D	2 D	29 D	22 D
	3	27 H	17 H	4 D	2 D	37 D	23 D
	4	34 H	20 H	5 D	3 D	47 D	28 D
	5	40 H	25 H	6 D	4 D	57 D	35 D
	5a	48 H	40 H	8 D	6 D	79 D	56 D
<=4.5 mm	2a	48 H	48 H	10 D	7 D	79 D	67 D
	3	48 H	48 H	10 D	8 D	79 D	67 D
	4	48 H	48 H	10 D	10 D	79 D	67 D
	5	48 H	48 H	10 D	10 D	79 D	67 D
	5a	48 H	48 H	10 D	10 D	79 D	67 D

Table 1: IPC/JEDEC J-STD-033 bake conditions for drying SMDs at the user site.

and storage for printed boards. (Click here for bake out tables.)

Another factor determining if a bake out is required is whether an in-line or batch washer was used for cleaning the assembly (see discussion below). If there are areas of the assembly, such as connectors, which can entrap water, this will also determine whether a board assembly needs to undergo the bake out process. Finally, the type of material the PCB is made of and the degree to which these materials are hygroscopic, will have an impact on the dry out process used. These are the most important, but certainly not all the influences on the need for baking out a board.

There are several reasons that drive the need to bake the PCB after washing post rework. If the boards are processed in an inline cleaning system consisting of air knives to blow off the moisture, there are several component types where this process is not sufficient. Moisture cannot easily be blown out from inside of connector pins, from under flat ICs, in magnetic windings and other components that can entrap moisture. If you then place the assembly


alpha
ASSEMBLY SOLUTIONS
IT'S TIME TO RISE UP AGAINST HIGH HEAT, WARPING AND DEFECTS.
ALPHA® OM-550. The revolution is coming. Heat has taken its toll on your bottom line long enough. Introducing ALPHA® OM-550 HRL1 – the most revolutionary advancement in solder paste since the introduction of lead-free. OM-550 cuts the soldering temperature required for SAC alloys by 50°C, while dramatically reducing power consumption and carbon emissions. The result is a highly reliable, cost effective, energy sufficient soldering process with up to 99% less warpage and significantly fewer defects. AlphaAssembly.com
A MacDermid Performance Solutions Business
A Platform Specialty Products Company

in a sealed bag with moisture still on it for more than a few hours, you have the makings of some reliability problems. If subsequent operations involve the application of coating, epoxy, encapsulation or others, moisture on the board can impede the process of curing. Moisture can also be a problem when you need to perform an electrical test as it will skew the test results, especially in high-voltage or high-frequency assemblies.

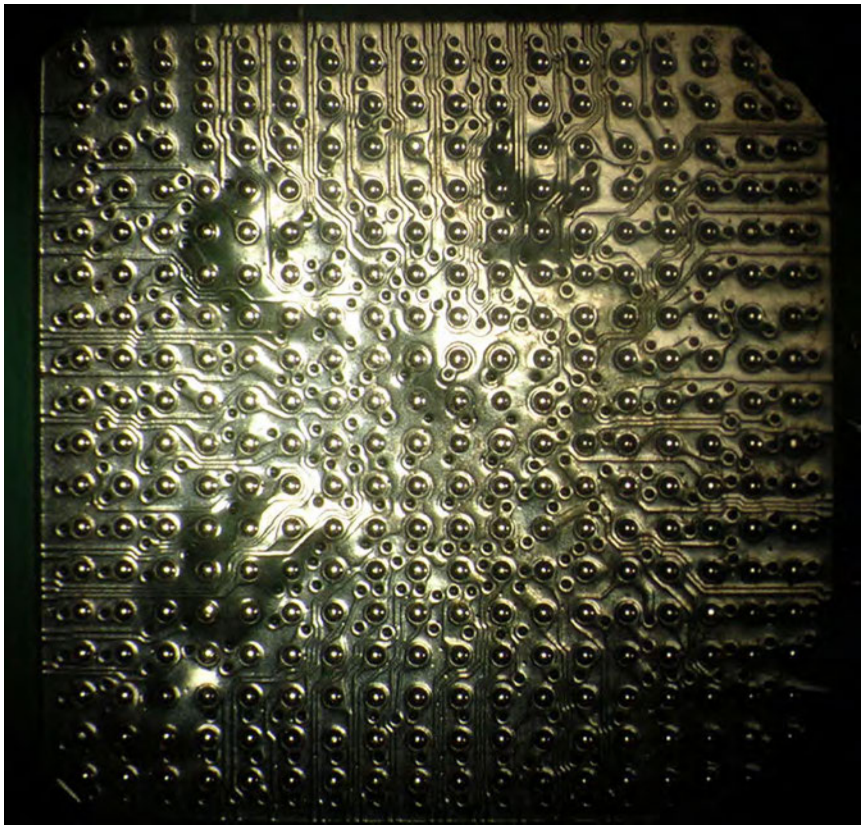


Figure 1: Proper MSD handling prevents defects like this popcorned BGA.

The thermal profile of the wash process will impact the degree to which the PCBs will absorb water. Normal process profiles are such that the temperature of the PCB increases as it goes through the wash system process. This temperature increase leads to molecular expansion, which makes the board more hydrophobic, or less likely to absorb moisture. It is critical to profile your wash systems such that board temperature rises steadily throughout the process by a few degrees.

Overbaking of PCBs after cleaning, post rework, may cause subsequent PCB assembly defects. Heating of the boards will increase the rate of oxidation. You do not want to continue to keep re-baking the PCBs as this oxidation may cause a problem in the wetting action of the solder.

How to Measure PCB Water Absorption

Electronic components, and in some cases PCB materials, are absorbing moisture in the rework process. A good way to monitor the moisture level is by measuring the weight of the board before and post drying. Weigh a small board or sample coupon using a precision balance. Follow this with a pre-bake of the board for two hours at 100°C, allowing it to cool. This is followed by re-weighing the parts, and noting the weight difference. You can use this weight difference to optimize pre-bake temperatures and times. In a thorough drying application, the assemblies should weigh less after cleaning than before cleaning.

You need to allow enough time for any of the moisture adsorbed in the inner board layers to make their way out of the PCB. Depending on the board thickness, this can be more than four hours. Since you want the moisture (and other solvents, possibly) to escape, the best way to do this is to have the boards in a rack, vertically oriented with some space in between the PCBs. If they are stacked on top of one another or flat on the base of the oven, etc., then it can be more difficult for the moisture to escape.

Once you have dialed in the drying process, make sure you keep the board dry by either putting it into a sealed moisture barrier bag or into a dry box. Make sure you seal the moisture barrier bag. If you don't vacuum seal your bag, you cannot count on them maintaining a less than 10% relative humidity inside the bag, regardless of how much desiccant you put in there.

Bake Out after Cleaning?

After cleaning of the reworked PCBs, the boards may need to be baked out. The vast majority of assemblies cleaned in an aqueous process, with or without cleaning materials beyond water alone, are dried but not baked out. A small percentage of printed circuit board assemblies seeing water in their cleaning process are followed by an oven-type extended bake out. If a bake is required, then a 2- to 4-hour bake at 105°C or an 8- to 24-hour bake at 65°C is adequate for typical FR-4 type assemblies.

The need for a bake out is also a function of the type of drying system found in your cleaner. If your cleaner utilizes an airknife to blow off the water from the assemblies, then your chances of requiring a bake process are increased, especially with multilayer boards. Airknife drying systems are most commonly found as part of inline cleaning systems. If your cleaner utilizes a convection/radiant forced heat type technology to dry the assemblies, then there's no need for bake out.

The answer to the question of whether a bake is required after rework and re-washing of a PCB is "it depends." **SMT**

References

1. IPC-1601 Printed Circuit Board Handling and Storage Guidelines.

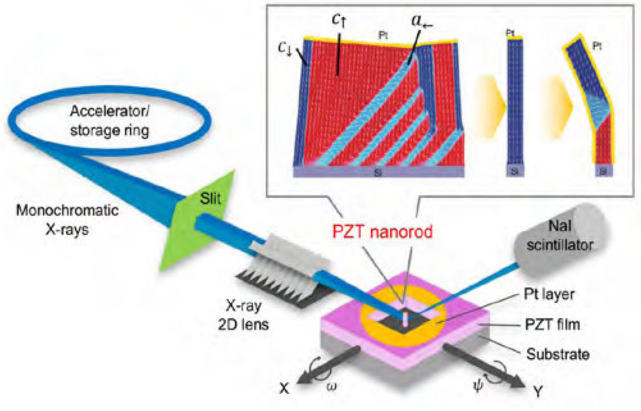
Bob Wettermann is the principal of BEST Inc., a contract rework and repair facility in Chicago.

Nagoya-led Team Flips the Switch on Ferroelectrics

An international team by Nagoya University has developed a new way of controlling the domain structure of ferroelectric materials, which could accelerate development of future electronic and electro-mechanical devices.

"We grew lead zirconate titanate films on different substrate types to induce different kinds of physical strain, and then selectively etched parts of the films to create nanorods," says lead author Tomoaki Yamada. "The domain structure of the nanorods was almost completely flipped compared with [that of] the thin film."

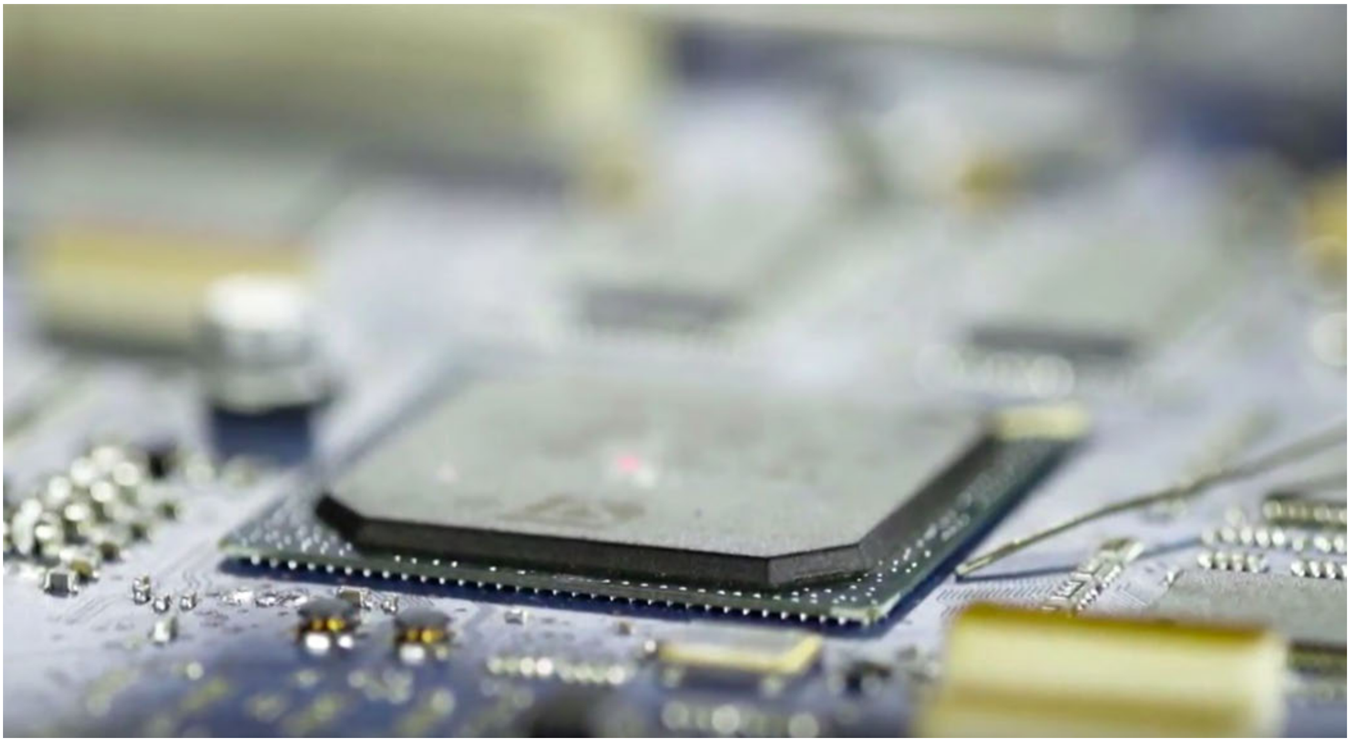
Lead zirconate titanate is a common type of ferroelectric material, which switches based on the movement of trapped lead atoms between two stable positions in the crystal lattice. Parts of the film were deliberately removed to leave free-standing rods on the substrates. The team then used synchrotron X-ray radiation to probe the domain structure of individual rods.



The contact area of the rods with the substrate was greatly reduced and the domain properties were influenced more by the surrounding environment, which mixed up the domain structure. The team found that coating the rods with a metal could screen the effects of the air and they tended to recover the original domain structure, as determined by the substrate.

"There are few effective ways of manipulating the domain structure of ferroelectric materials, and this becomes more difficult when the material is nanostructured and the contact area with the substrate is small," says collaborator Nava Setter. "We have learned that it's possible to nanostructure these materials with control over their domains, which is an essential step towards the new functional nanoscale devices promised by these materials."


STRONG
FOUNDATION



BTC and SMT Rework Challenges

by Joerg Nolte
ERSA GMBH

Introduction

Rising customer demands in the field of PCB repair are a daily occurrence as the rapidly evolving electronics industry follows new trends in a blink of an eye. New strategies and technologies are required to fulfill those demands.

Out of the long list of today's customer demands for efficient BTC and SMT PCB repair, some subjects show up on a daily basis and are generally agreed upon as relevant for the coming years:

- BTC types with new effects: voidless treatment
- Smaller components: miniaturization (01005 capability)
- Large board handling: dynamic preheating for large board repair
- Repeatable processes: flux and paste application (dip and print), residual solder removal (scavenging), dispensing, multiple component handling, and traceability
- Operator support: higher automation, software guidance (human computer interface)
- Cost effectiveness: rework systems for different budgets and ROI situations

Some of the listed topics above have not shown their practical relevance yet. There have been a number of discussions about 01005 rework capabilities, but up to now there is no proven evidence that those technologies that claim to be capable, can truly run successful rework processes on this tiny component in a daily real-world rework situation. Many parameters need to be observed and controlled in precision line-production, including:

- desoldering and lifting of component without affecting very close neighbouring components
- new selective solder paste supply for the small joints
- picking, adjustment and placement of the component
- PCB coating
- PCB cleaning and others

Nevertheless, as the 01005 components exist, the challenge is set. While the component size is shrinking and integration as well as the packing density are rising, on the other hand the PCB size is growing. Mainly driven by telecommunication and internet data transmission (cloud computing, IOT), the processing power of today's computer centers is increasing rapidly. And in the same way parallel processing computer boards are growing in size. One challenge that remains is, how to homogeneously preheat a fully populated 24" x 48" multilayer PCB during rework?

Other topics like tracing and documenting the individual board treatment in the rework area seem to become a must in times of soaring electronic production and as repair processes have become an acknowledged part of electronic assembly. Out of the above mentioned topics, which basically describe a roadmap for rework capabilities until 2021, three subjects will be introduced subsequently. Other than issues that will be important for future repair and rework feasibility they have already reached practical necessity since a while ago and thus need to be fully implemented or improved in today's rework systems.

Voidless Treatment During a Rework Process

In the assembly of bottom terminated components (BTC) the formation of voids has become a serious problem in many applications. A definition for a void is given in the context of soldering defects as:

[…] then solder will quickly fill the opening of the fitting, trapping some flux inside the joint. This bubble of trapped flux is the void; […] the joint, preventing solder from occupying that space. An area inside a soldered joint where solder is unable to completely fill the fittings' cup, because flux has become sealed inside[1].

And in SMT, only one of the possible effects is explained as:

[…] The reliability of solder joints becomes more of a concern, as less and less solder is allowed for each joint. Voiding is a fault commonly associated with solder joints, especially when reflowing a solder paste in the SMT application. The presence of voids can deteriorate the joint strength and eventually lead to joint failure[2].

The following impacts of void formation inside a solder joint have been reported:

- reduced thermal transfer from component to the PCB with risk of overheating the component
- reduced mechanical strength of a solder joint
- possibility of spontaneous out gassing—creation of solder splashes
- impact to the ampacity of a solder joint—connection may overheat because of higher electrical resistance
- impact on the signal transmission—in high frequency applications voids may dampen the signals

Especially in power electronics, the formation of voids in the thermal pad (e.g., QFN packages) is currently an increasing problem. The necessary transfer of energy from the component into the PCB for cooling purposes might be disabled. The components lifetime will be drastically reduced.

Besides other methods like using low-voiding solder pastes, optimizing the reflow profile and applying the correct amount of solder paste with optimized stencils, a void reduction treatment of the entire assembly while the solder is in its liquid phase is an option to choose.

So the question is, how is it possible to implement a void treatment technology into an open environment of a rework machine? The vacuum technology known from reflow ovens is not an option. The technique used is based on a sinusoidal actuation of the PCB substrate (Figure 1). Primarily the PCB is stimulated by a longitudinal wave with an amplitude of less than 10 µm on the PCB level. During this sinusoidal actuation of the PCB in a defined frequency range, the self-resonances of this area are stimulated regardless of the PCB layout and population. When the PCB is in sweep motion, the component remains in its location and the

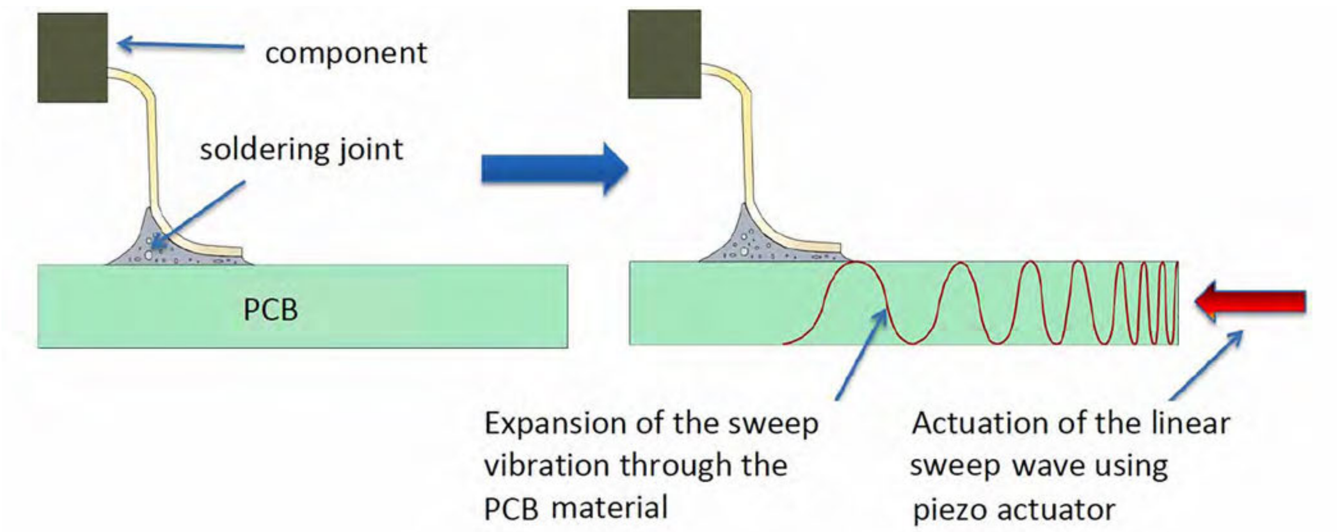


Figure 1: Voidless treatment of a PCB with piezo actuator.

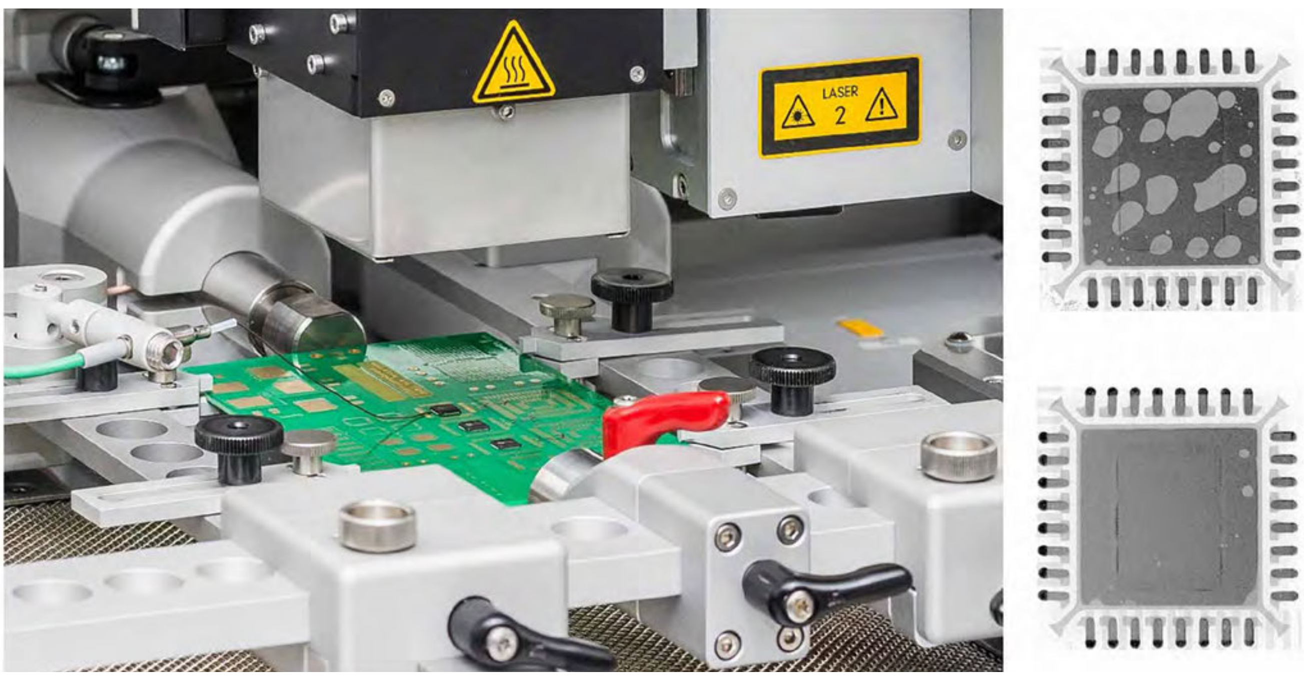


Figure 2: Actuation of a PCB during reflow, to reduce the void rate in an MLF (results before and after treatment).

voids, trapped in the boundary layer, the liquid solder, have the ability to escape.

By this method, void reduction during new component installation down to void rates of 2% is possible (Figure 2). Even a significant void reduction can be achieved during a second reflow on an existing assembly. As in the case of a voidless rework treatment, only a selected area of the PCB is heated up to reflow and only this section is treated with the actuation, with no negative side effects to the assembly can be expected.

Residual Solder Removal—Scavenging

Other than in production, one important step during the repair of a printed circuit board

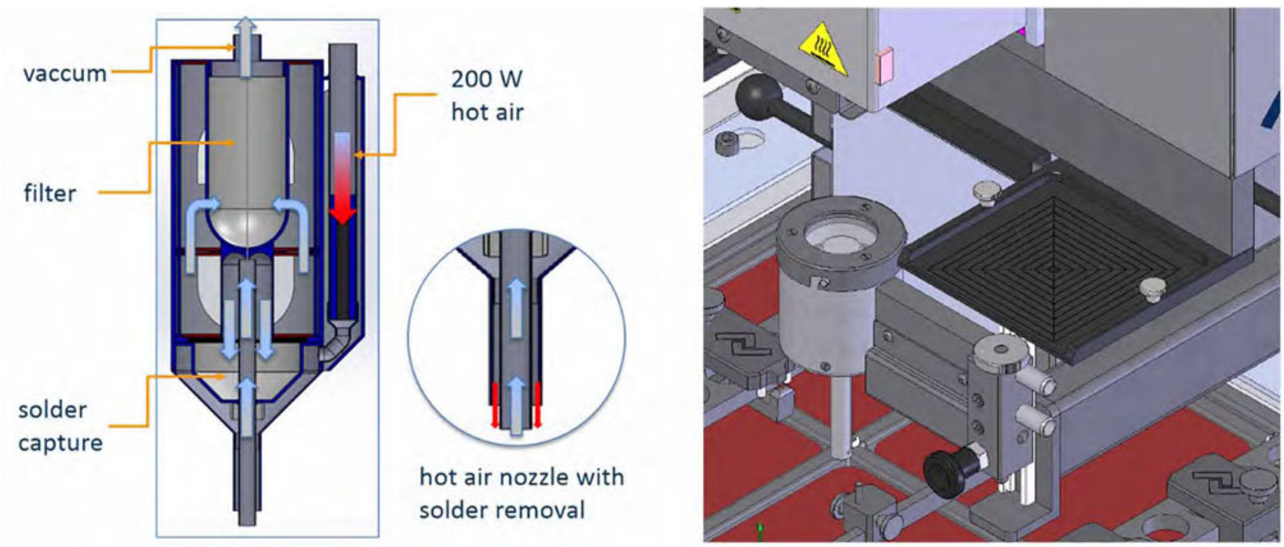


Figure 3: Scavenging system for residual solder removal during SMT rework and mounting.

is the removal of residual solder on top of the components board land pads. It is necessary to properly reinstall a new component onto a defined surface and achieve repeatable and reliable soldering results. Today's hand-operated methods are related to the operator's skills and thus are a hidden risk.

A manually operated, but non-contact residual solder removal module has many benefits:

- repeatable process and non-contacting suction of the solder
- no risk of pad damage or rip off
- no solder mask damage
- no contamination of the PCB with flux or solder residues

The method is to use a gentle air flow along with the PCB bottom side preheating to melt the remaining solder on the PCB and suck off the liquid solder with a vacuum nozzle shortly above the PCB surface (Figure 3).

Besides the known technology of melting the solder with a gentle air flow and cleaning off the solder from the PCB with vacuum, it is necessary to control the height above the PCB in order to keep the boards undamaged. In first applications the height adjustment will be manual, in advanced systems there will be an automatic height adjustment based on pressure control or with a laser triangulation sensor.

Solder separation and flux filtration as well as an acceptable maintenance of the unit are crucial features for successful daily operation.

This module cannot be seen as completely independent from a rework machine, but an integrated part. The board temperature should be known and the PCB bottom side preheating must be active and controlled during the process.

Operator Guidance—Software Assisted Operation

The market clearly asks for flexible and easy to operate rework systems and at the same time for high automated, user independent equipment. For all of them a clearly structured interaction with the operator or the system administrator is essential.

One clear customer expectation towards rework processes is achieving user-independent, high-quality results. This is why more automated process steps are implemented into rework units and improvements on the HCI (human computer interface) are requested. It is obvious that operator guidance and assistance is decreasing operator failures during the rework procedure. Clearly structured software surfaces provides all necessary information along

Figure 4: Clearly structured profile selection for a rework process.

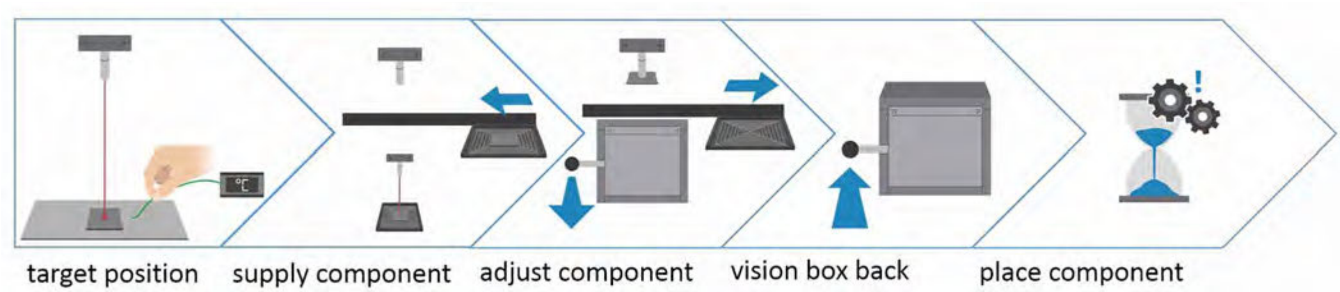


Figure 5: Placement process with pictograms guiding the operator step by step.

the single operations from profile selection, component removal until the final installation with flux or solder paste (Figure 4).

All process steps are assisted, the operator is guided through the process and instructed about the next working step. Pictograms show the next manual procedure if the system is not automatically executing the operation (Figure 5).

Computer aided placement (CAP) is another tool, supporting the operator by means of image processing to achieve the best results. In the example the so called "comparator mode" shows coloured images of pads and pins and the best overlay in false colours (Figure 6). Component pins are shown in red, pads on the PCB are shown in green. Once the pins overlap to the pads the colour changes to blue and indicates to the operator when the best placement condition is reached.

Other than in a live camera image, the computer aided placement uses means of image processing to provide best contrast pictures. Like for an air traffic controller (Figure 7), the system clearly visualizes the relevant data for

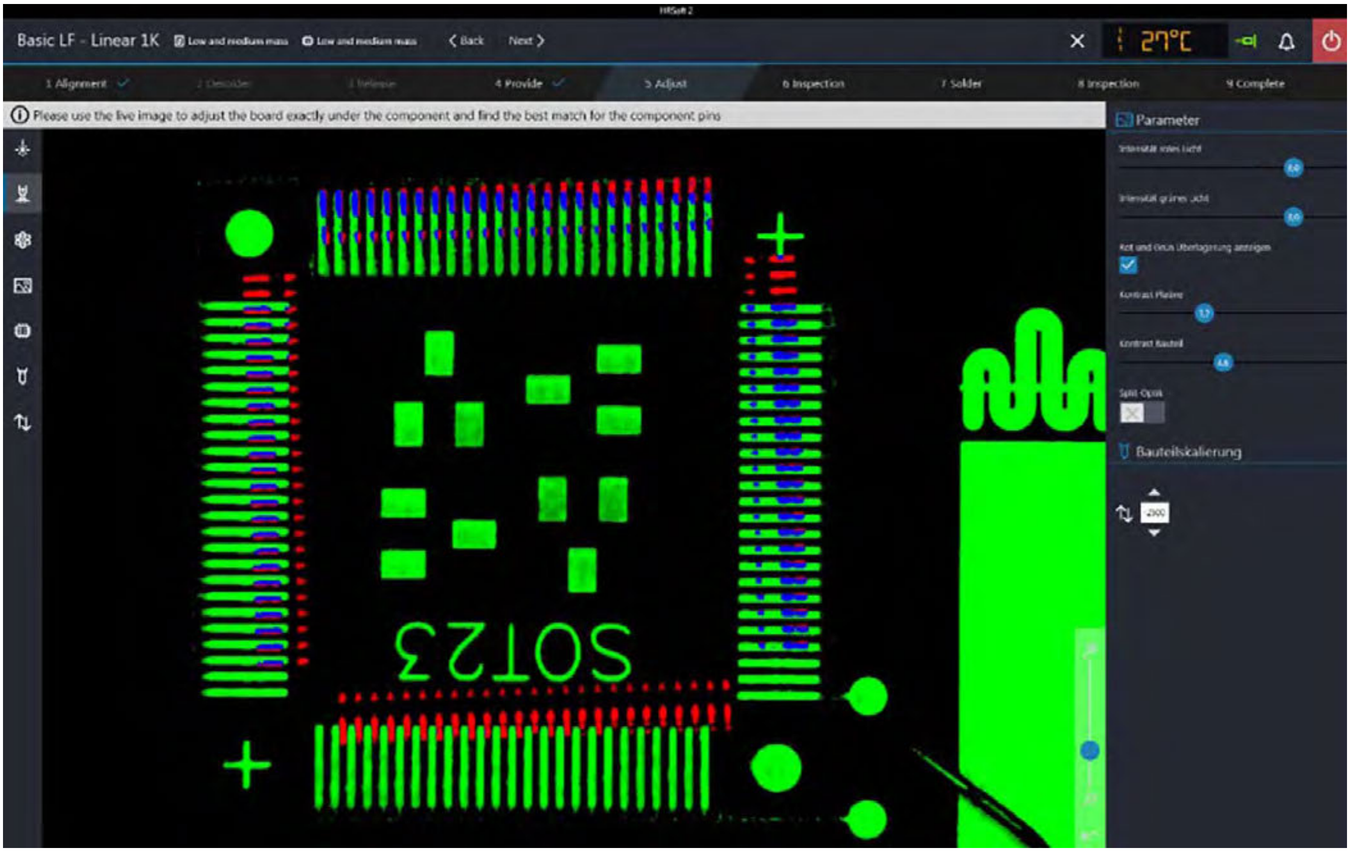


Figure 6: Computer aided placement with overlay of pins and pads in false colour depiction.

Figure 7: Flight radar image shows only relevant information in high contrast (as a reference).

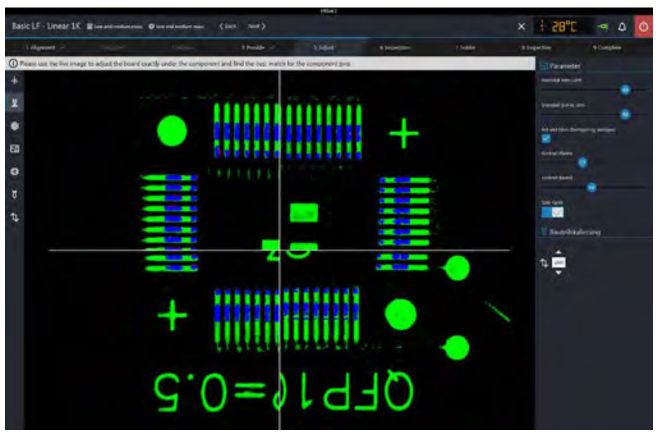


Figure 8: Digital split optic shows for corners of a component—here with ideal pin to pad matching.

the operator. Hereby, the concentration of the operator is focused on the alignment task and exhausting working conditions are minimized.

Another element of computer aided placement is the implementation of a digital split optic. It supplies images of (i.e., large QFP components) in high magnification for most accurate alignment (Figure 8). Instead of optical magnification with additional lenses, the high resolution camera image is split into

four segments. Each segment displays one component corner. Alignment is supported in large magnification. Matching of pins and pads becomes much easier for the operator's eyes.

Summary and Future Outlook

Even if production quality throughout the electronic industry is constantly rising, rework will remain a challenging topic for the next decades. Electronic assemblies are reaching higher integration and a generally increasing complexity. The rework system supplier's task will be to follow these market movements and offer solutions that provide the ability to rework boards successfully. At the same time the degree of automation will rise in the segment of rework equipment, and operator assistance will become more important. Besides technological challenges as many features as possible of the high end rework systems need to find their way down to the entry level rework units as a spin off. Commercial and environmental benefits due to less scrap and electronic waste will thus be achieved. **SMT**

References

1, 2. Wikipedia: "Void" in soldering defect and surface mount technology.

Editor's Note: This article was originally presented at the technical proceedings of IPC APEX EXPO 2017.

Joerg Nolte is the product manager for tools, rework and inspection systems at Ersa GmbH.

NIST Scientists Push Us Closer to Flash Memory Successor

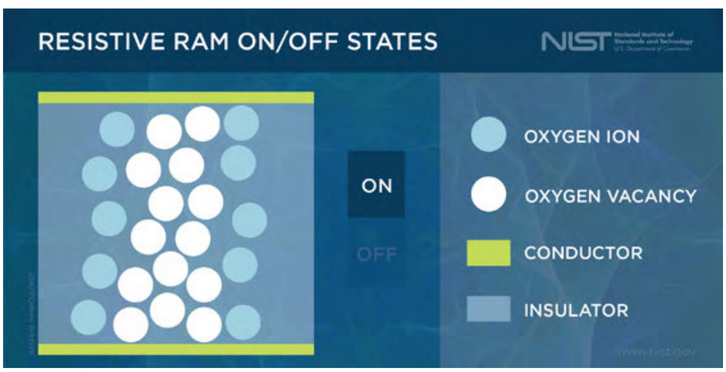
Research at the National Institute of Standards and Technology (NIST) may have found that subtlety solves some of the issues with a novel memory switch.

This technology, resistive random access memory (RRAM), could form the basis of a better kind of nonvolatile computer memory, where data is retained even when the power is off. RRAM could surpass flash in many key respects, it has yet to be broadly commercialized because of technical hurdles that need addressing.

One hurdle is its variability. A practical memory switch needs two distinct states, representing either a one or a zero, and component designers need a predictable way to make the switch flip. Conventional memory switches flip reliably when they receive a pulse of electricity, but we're not there yet with RRAM switches, which are still flighty.

In two recent papers, the research team has found a potential solution. The key lies in controlling the energy delivered to the switch by using multiple, short pulses instead of one long pulse.

"Shorter pulses reduce the variability," NIST guest researcher David Nminibapiel said. "The issue still exists, but if you tap the switch a few times with a lighter 'hammer,' you can move it gradually, while simultaneously giving you a way to check it each time to see if it flipped successfully."



Because the lighter touch does not push the switch significantly from its two target states, the overlapping issue can be significantly reduced. Nminibapiel added that the use of shorter pulses also proved instrumental to uncovering the next serious challenge for RRAM switches—their instability.

2017 Programs

August 9
Wisdom Wednesday — Webinar
Members Only

September 13
Wisdom Wednesday — Webinar
Members Only

September 16–21
IPC Fall Committee Meetings — Meeting
held in conjunction with SMTA International
Rosemont, IL, USA

October 3–4
IPC & WHMA Wire Harness Manufacturing Conference — Conference
Paris, France

October 3–4
IPC Technical Education — Workshop
Paris, France

October 9–10
IMPACT Europe — Meeting
Brussels, Belgium

October 11
Wisdom Wednesday — Webinar
Members Only

October 17–18
IPC Flexible Circuits-HDI Forum — Conference
Tutorials and Technical Conference
Minneapolis, MN, USA

November 8
IPC Technical Education — Workshop
held in conjunction with PCB Carolina
Raleigh, NC, USA

November 8
Wisdom Wednesday — Webinar
Members Only

November 14–17
IPC Committee Meetings — Meeting
held in conjunction with productronica
Munich, Germany

November 14–17
IPC Hand Soldering Championship — Competition
held in conjunction with productronica
Munich, Germany

December 6–8
HKPCA International Printed Circuit & APEX South China Fair — Conference and Exhibition
Shenzhen, China

December 13
Wisdom Wednesday — Webinar
Members Only

Contribute to the industry standards and guidelines that your company, customers, suppliers and competitors rely on by attending IPC standards development committee meetings.

IPC Standard Development Committees cover a range of topics, including:

- Assembly & Joining
- Assembly Equipment
- Base Materials
- Cleaning & Coating
- Environment, Health and Safety
- Fabrication Processes
- Flexible and Rigid-Flex Printed Boards
- High Speed/High Frequency
- Packaged Electronic Components
- Printed Board Design Technology
- Printed Electronics
- Process Control
- Product Assurance
- Product Reliability
- Rigid Printed Boards
- Testing

For more information, visit www.ipc.org/fall-meetings.

For more information, visit www.IPC.org/events

Supply Lines
Highlights

Pillarhouse International's Allan Jiang Discusses Selective Soldering Developments

At the recent NEPCON China event in Shanghai, Allan Jiang, sales manager at Pillarhouse International, discusses with I-Connect007 Managing Editor Stephen Las Marias some of the challenges in selective soldering, and technology developments to address these issues.

Rehm Receives Supplier of the Year Award from Continental Automotive Group

Rehm Thermal Systems has received a supplier of the year award in the category "Investment and Engineering (Soldering Machines)" from Continental Automotive Group.

Indium to Feature Ultra-Low Voiding Solder Paste at SMTAI 2017

Indium Corporation will feature its ultra-low voiding Indium10.1HF solder paste at the upcoming SMTA International Technical Conference, to be held September 17–21, 2017, in Rosemont, Illinois.

Optimal Electronics Adds Robotics Expert to Its Industry 4.0 Team

Optimal Electronics Corp. has expanded its Industry 4.0 team with the addition of Mile Ostojic as the company's new expert for robotic applications.

Cogiscan and Technica U.S.A. Launch Sales Partnership

Cogiscan Inc. has named Technica U.S.A. as its sales representative throughout Northern California, the Pacific Northwest and the Mountain States.

CCL Celebrates 20 Years of Serving the Electronics Manufacturing Industry

Adam Chinery, managing director at Computer Components Ltd (CCL), discusses the company's 20-year anniversary and how CCL plays an active role in supporting OEM and EMS customers.

CalcuQuote to Debut Purchasing Application for EMS at SMTAI 2017

CalcuQuote will launch a new procurement software for EMS companies at the SMTA International Expo 2017.

Koh Young Technology Receives Bosch Global Supplier Award

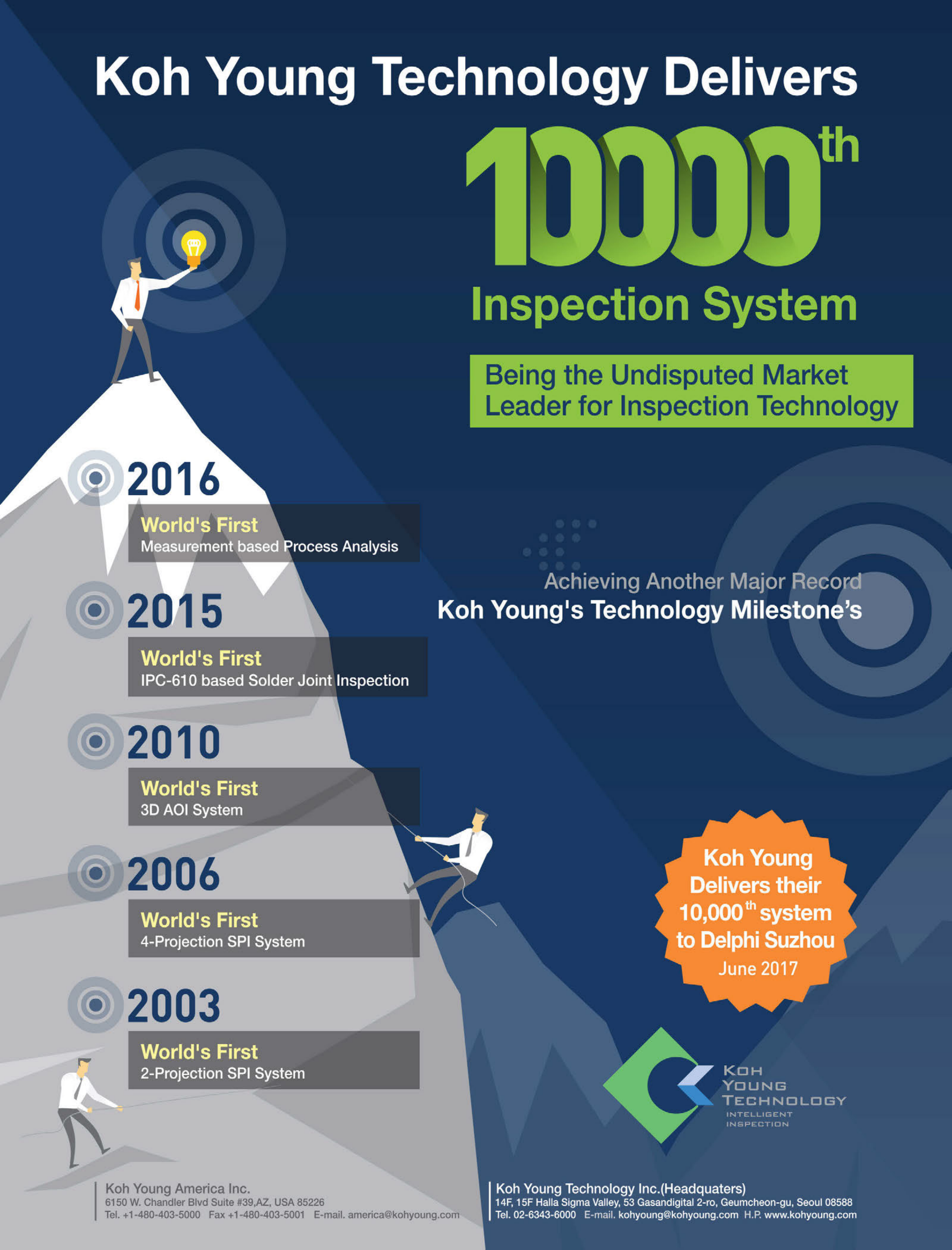
Koh Young Technology has received a supplier award in the 'purchasing of indirect material' category at Robert Bosch GmbH's recent Global Supplier Award 2017.

Carlos Espinoza Promoted to Operations Manager at KIC

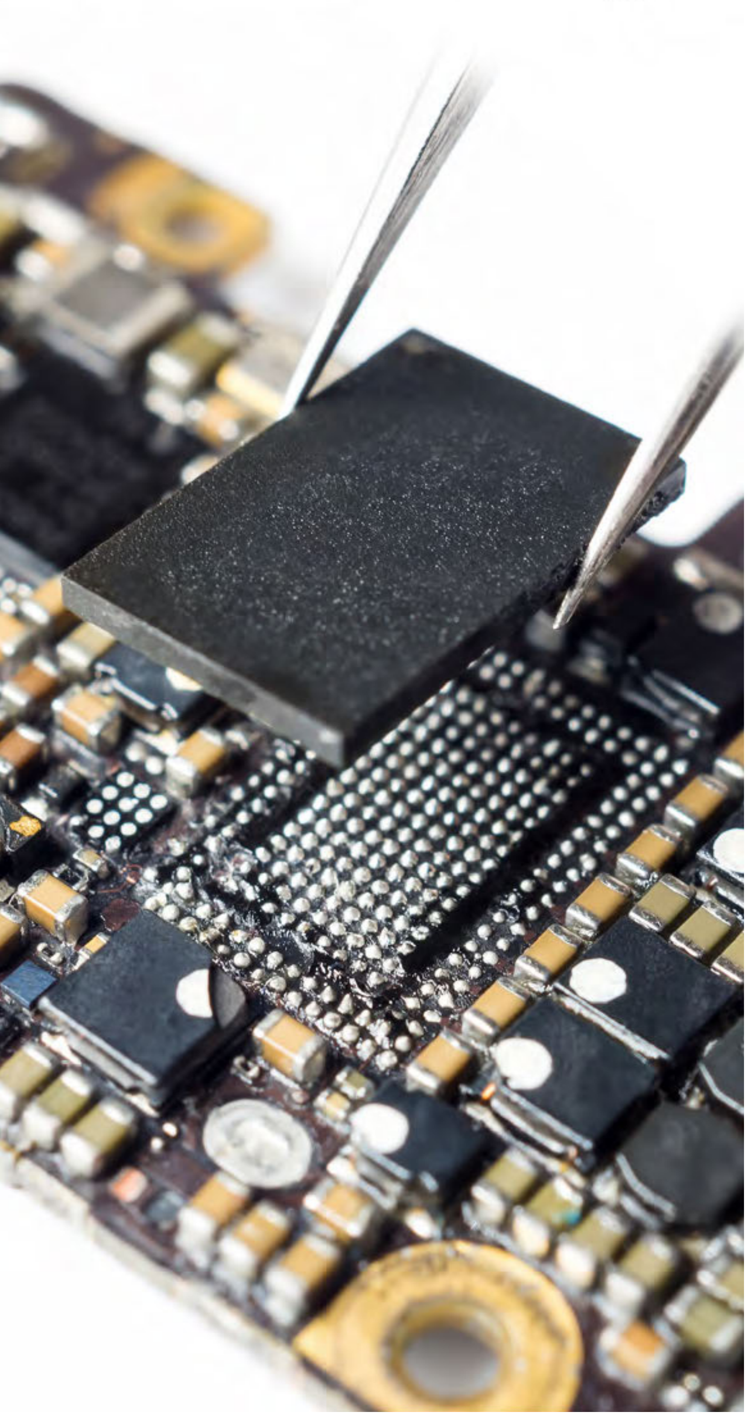
KIC has promoted Carlos Espinoza to the position Operations Manager. Espinoza has more than 20 years of planning, forecasting, purchasing, supply chain, and inventory management experience to drive efficiencies and reduce costs.

Magneti Marelli Selects Goepel X-ray Inspection System

Magneti Marelli has decided on two X-ray inspection systems from Goepel electronic for quality assurance of electronic assemblies.


Koh Young Technology Delivers
10000th
Inspection System
Being the Undisputed Market Leader for Inspection Technology
2016
World's First
Measurement based Process Analysis
2015
World's First
IPC-610 based Solder Joint Inspection
2010
World's First
3D AOI System
2006
World's First
4-Projection SPI System
2003
World's First
2-Projection SPI System
Achieving Another Major Record
Koh Young's Technology Milestone's
Koh Young Delivers their 10,000th system to Delphi Suzhou
June 2017
KOH YOUNG TECHNOLOGY
INTELLIGENT INSPECTION
Koh Young America Inc.
6150 W. Chandler Blvd Suite #39,AZ, USA 85226
Tel. +1-480-403-5000 Fax +1-480-403-5001 E-mail. america@kohyoung.com
Koh Young Technology Inc.(Headquaters)
14F, 15F Halla Sigma Valley, 53 Gasandigital 2-ro, Geumcheon-gu, Seoul 08588
Tel. 02-6343-6000 E-mail. kohyoung@kohyoung.com H.P. www.kohyoung.com

Rework and Reball Challenges for Wafer-Level Packages



by Lauren Cummings and Priyanka Dobriyal, Ph.D.
INTEL CORP.

Abstract

With increasing consumer demand for smartphones, wearable devices, and Internet of Things applications, there is a growing trend in package and printed circuit board miniaturization. In particular, wafer-level packages (WLPs) have garnered recent popularity for their affordable cost, small footprint, and thin profile. Component suppliers must be prepared to support failure analysis (FA) for PCB-assembled WLPs, including fault isolation (FI), nondestructive screening, as well as destructive analysis techniques. If a board- or package-level failure is subtle or cannot be detected non-destructively, the WLP requires rework and reball before proceeding with further component-level testing and destructive FA. Due to their fragility and small form factor, the rework and reball process steps pose considerable risks for WLPs. The component lacks a package substrate and is easily damaged using traditional rework tooling and handling. On high-density boards and modules, there is also a risk for adjacent board-side passives or packages to be bumped and damaged during package removal from the PCB. The present work addresses the rework and reball challenges of a specific WLP case study, and suggests improvements for maintaining the true failure signature. Rework and reball recipes were successfully developed for a WLP, and optical microscopy (OM) and C-mode scanning acoustic microscopy (CSAM) were used to inspect for thermally or mechanically-induced artifacts. By implementing enhanced WLP rework and reball methods, the industry will be better poised to improve the quality and reliability of small form factor devices.

Introduction

There is a growing consumer demand for smart wearable products, including watches, fitness bands, eyewear, and headphones. Barriers to the market still exist, as many consumers are concerned with style, battery life, functionality, and cost. The mature smartphone market faces similar challenges, with consumers

desiring thinner phones with longer battery life and increased sensor functionality. High-density and stacked PCB designs, system in package (SiP) assemblies, and small form factor packages have all emerged as solutions for sleeker styles and improved functionality. In particular, WLPs are gaining popularity for their low cost, small footprint, and thin profile. The newest smartphone models contain an average of 5-7 WLPs, with many WLPs used as RF transceivers, power management units, audio amplifiers, and BlueTooth and GPS modules[1].

Unlike traditional packages, WLPs are packaged and bumped first, then diced. Passivation and dielectric layers are added to the die frontside, followed by metallic redistribution layers. A second dielectric layer is deposited, then the underbump metallization and solder balls are attached. Lastly, the packages are singulated from the wafer. Figure 1 illustrates the two different categories of WLPs: the traditional a) fan-in WLP, and the newer b) fan-out WLP. The dielectric is exposed on the edges and frontside of fan-in WLPs, while the silicon backside is often covered with a protection tape. As the name suggests, fan-out WLPs "fan out" interconnects from the smaller silicon die to the larger package dimensions. The fan-out design allows for ball pitch customization, higher I/O density, and easy integration with SiPs and other multi-die packages. The board-level reliability is also improved by protecting the silicon die with an epoxy mold compound.

Though WLPs offer considerable advantages, they also pose challenges for failure analysis—particularly when reball and component-level testing are required. Figure 2 illustrates the typical FA process flow for a failing system, such as a mobile phone, tablet, or wearable device. Fault isolation is performed first to identify the failing component, then nondestructive FA is used to inspect for failures at both the board- and package-level. If the failure is subtle or cannot be found non-destructively, the package must be reworked and reballed before proceeding with socketed component-level testing

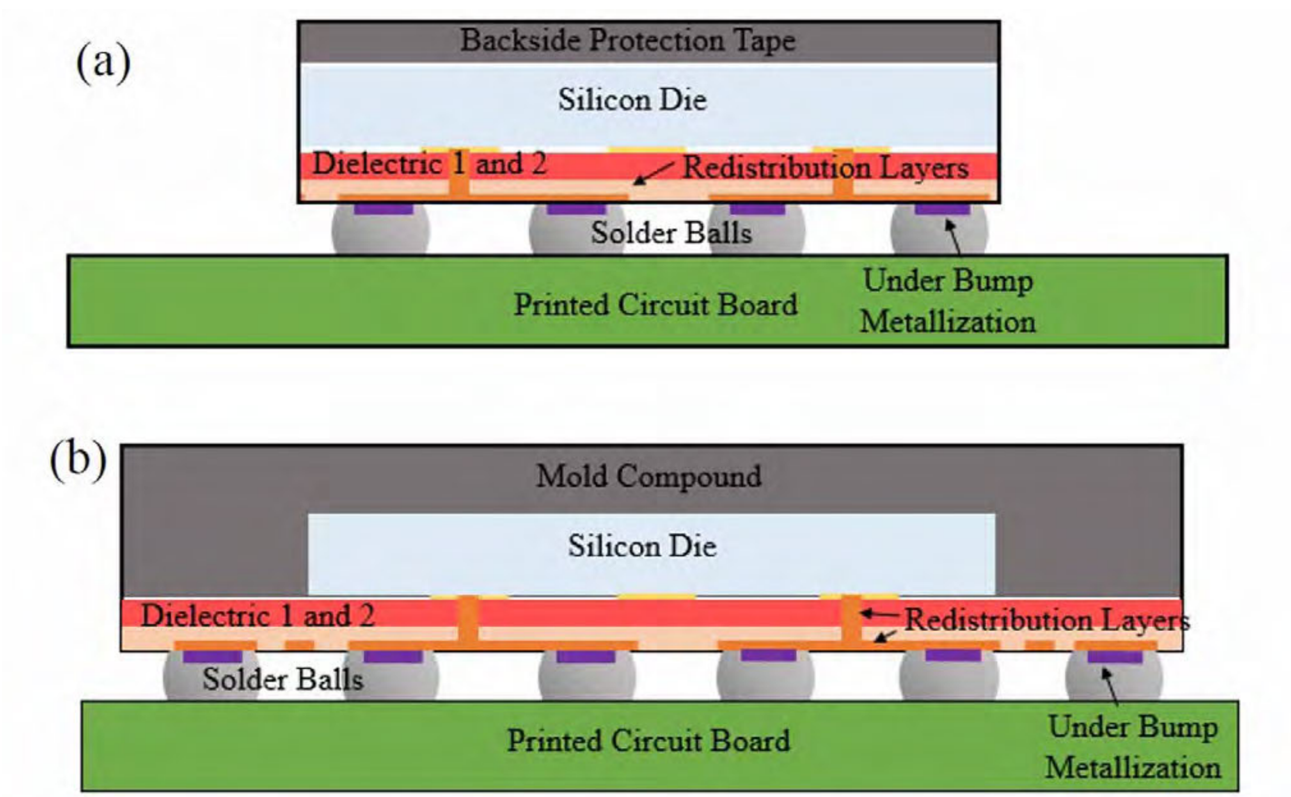


Figure 1: Cross-section schematics of (a) a traditional fan-in wafer level package, and (b) a newer fan-out wafer level package.

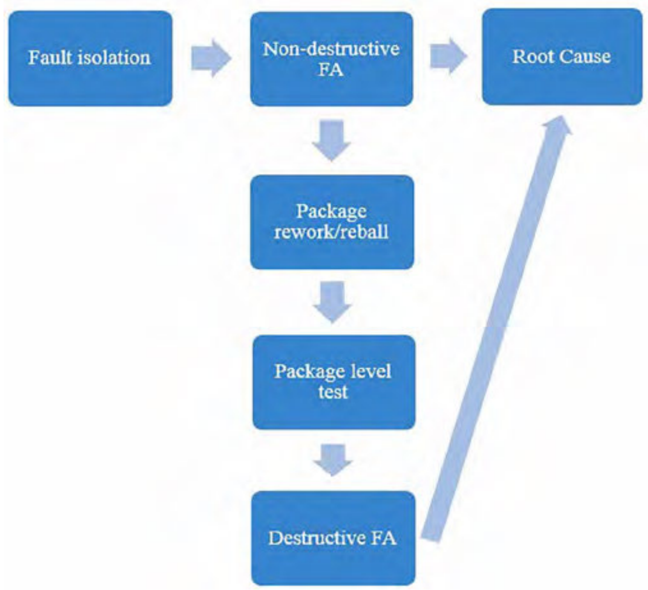


Figure 2: Diagram showing the typical process flow for system-level failure analysis.

and further FA. Due to their small form factor and fragility, WLPs can prove particularly difficult for the rework and reball process steps. The present work provides an overview of the FA process flow, emphasizing component rework and reball methodologies. The challenges of a specific WLP case study are discussed, and rework and reball improvements are implemented to minimize thermally- or mechanically-induced artifacts.

Fault isolation is an important first step in the system-level FA process. By isolating the failure to a specific package or interconnect, an optimal FA approach can be assessed and throughput time can be greatly reduced. Several fault isolation techniques can be used to measure for opens and shorts, including hand probing, time domain reflectometry and the newer electro optic terahertz pulse reflectometry [2]. High-resistance shorts can also be detected by powering the board and measuring the localized temperature increase using infrared thermal imaging techniques [3].

After the failing component has been isolated, nondestructive FA is performed to inspect for gross board- or package-level failures. OM can be used to inspect for external board or package defects, such as foreign materials or superficial die and overmold cracks. Since WLPs have exposed dielectric layers (and since fan-in WLPs have exposed bulk Si), it is especially important to perform a first pass inspection for external chips or cracks. It is recommended that optical inspection be performed again after rework and reball, to confirm that no artifacts were introduced.

CSAM, a popular non-destructive technique, can be utilized to detect internal defects or to evaluate the extent of external damage. CSAM uses an ultrasound transducer to raster-scan the package backside. At material interfaces, an acoustic pulse is reflected to the transducer and recorded as signal amplitude. Air-solid interfaces occur at the locations of cracks, voids, or delamination, and return high-intensity reflections. CSAM is thus a valuable metrology for identifying gross internal package defects that cannot be detected with simple optical inspection. CSAM can also be used to screen for rework and reball artifacts, particularly thermally-induced delamination.

2D X-ray is another common technique that provides an effective "quick pass" inspection for board-level solder defects, such as voids and bridging. By optimizing the sample tilt and rotation angles, subtler non-wet open and non-contact open defects can also be detected. However, 2D X-ray is not capable of detecting sub-micron defects, such as board-level solder or via cracks.

Recently, more advanced imaging metrologies have emerged as powerful non-destructive FA techniques. In particular, 3D X-ray computed tomography has proven effective at detecting both board-level and package-level sub-micron defects[2,4]. Multiple 2D X-ray images are collected as the sample is rotated at fixed angle increments. The 2D X-ray images are then superimposed to generate a three-dimensional volume. The superimposed image can be manipulated to display virtual "slices" of the sample, allowing for inspection of the solder joints, via barrels, and traces.

If board-level or gross package-level failures are not detected using non-destructive techniques, the package must be sent for socketed component-level testing and further FA. Standard test sockets use a spring-loaded floating base that is guided by the solder balls instead of the package edge. Reball is thus required to align the package and enable good electrical contact with each pin. It is very important to preserve the defect signature prior to testing; accordingly, precautions must be taken to improve the reball yield and reduce thermal and mechanical artifacts.

Rework and reball process yield is influenced by several different factors, and can be classified into four general categories, including: (1) personnel; (2) methods; (3) materials; and (4) machine/tooling[5]. Figure 3 summarizes the various categories and sub-categories for a typical PCB assembly.

The personnel category represents the "human factor," and includes handling, training, and quality control. The personnel factor is especially important for WLPs and other small form factor devices, as the components are much more fragile than standard flip-chip packages. Proper handling must be used to minimize mechanical artifacts and prevent damage to the bulk Si or dielectric layers.

The methods category encompasses the process steps for rework and reball, including sample preparation, package removal from the board, solder removal from the package-side pads, and reball of the package. Prior to demount, the sample must be prepared by removing any heat spreaders, thermal grease, corner glue, or underfill. The package is then demounted from the PCB using either mechanical or thermal methods. Next, solder is removed from the package-side pads using solder wicking with a braided wire and solder tip, or using a no-contact vacuum scavenging technique [6]. Lastly, the package is reballed using either a stencil, preform, or laser jetting method. Figure 4 shows the transformation of a WLP throughout the rework and reball process.

Materials—such as package type, PCB design, flux, underfill, and corner glue—also influence the rework and reball process yield. With higher board densities and package miniaturization, it becomes increasingly difficult to selectively heat and remove parts from a small footprint. Since WLPs do not possess a package substrate or solder mask, there is also an increased risk to damage the dielectric or even the metal redistribution layers.

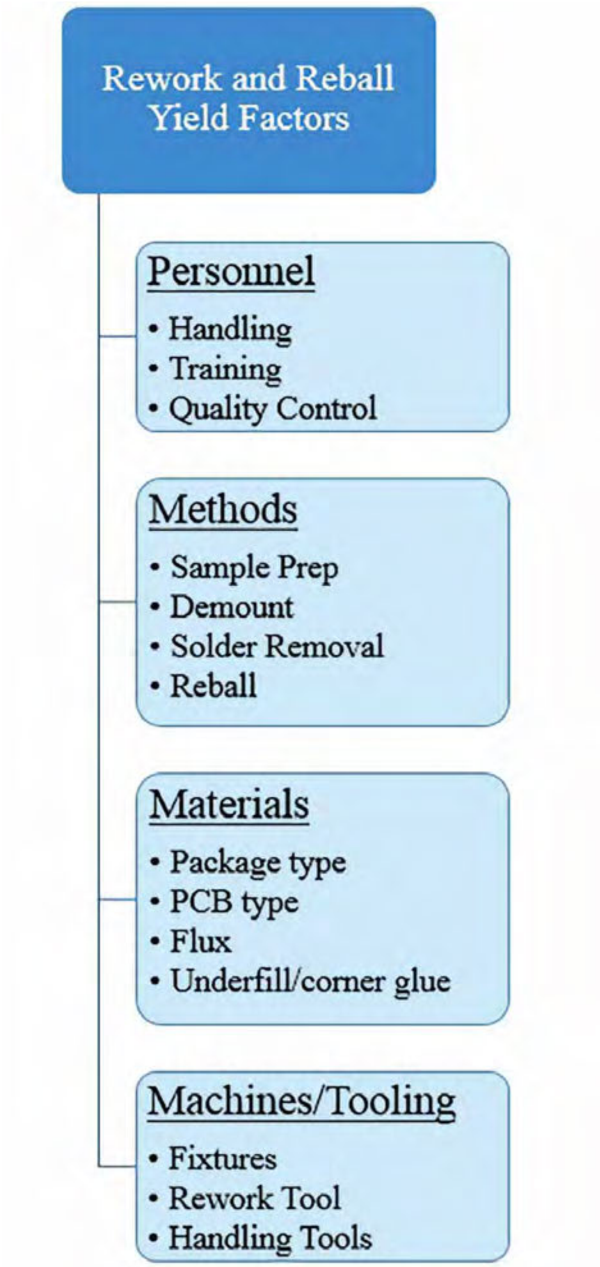


Figure 3: Diagram showing the factors that dictate the yield of rework and reball processes.

Lastly, rework yield is impacted by the machines and tooling used to handle and process the package. Rework machines can vary greatly in cost and complexity—ranging from a hot air pencil and tweezers, to a fully automated rework station. Semi-automated and fully automated rework tools are expensive, but can greatly minimize the risk for thermal and mechanical artifacts. The latter is especially impor-

BLACKFOX
Premier Training & Certification
Do you require IPC Training?
Blackfox is the Answer.
Blackfox is one of only a few that offer training in all 6 IPC certification programs.
We also provide training for instructors, operators, lead free, high temp solder and more!
CLICK FOR COURSE SCHEDULE
For more information contact us at 888.837.9959 or sharonm@blackfox.com
www.blackfox.com

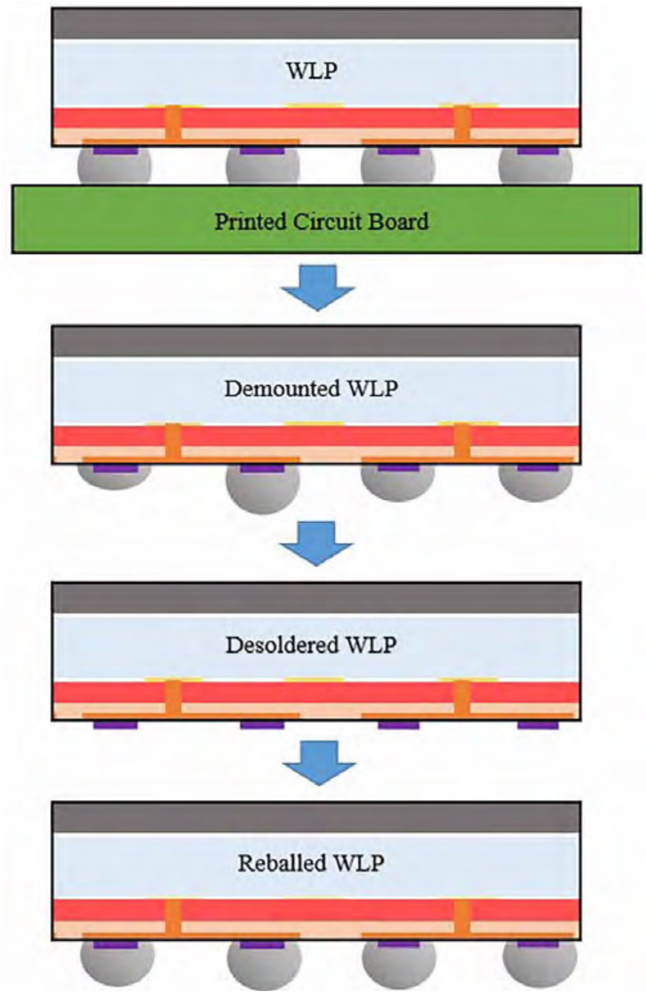


Figure 4: Schematic illustrating the WLP condition after demount, desolder, and reball.

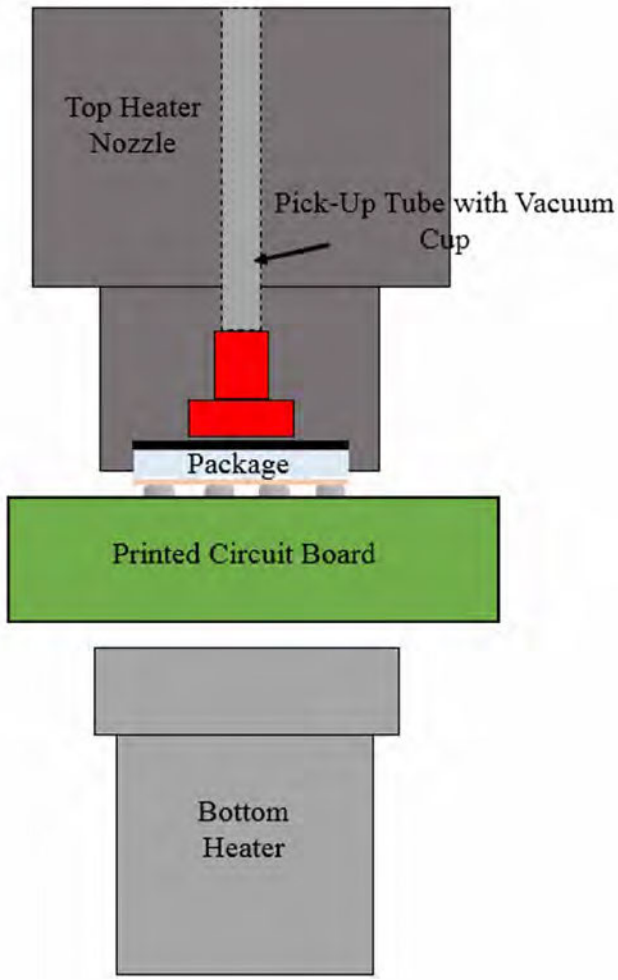


Figure 5: Schematic of set-up used to demount a WLP from a PCB.

tant for WLPs, as it is difficult to handle and secure the parts.

Experimental

A 3.5 x 3.5 fan-in wafer-level chip scale package was used for rework and reball evaluation. The package uses standard 0.5 mm pitch SAC405 solder balls. Demount, desolder, and reball steps were all performed using a semi-automated rework system. OM and CSAM inspection were performed before and after to assess for mechanically- or thermally induced rework artifacts.

Package Demount from Board:

Figure 5 shows the set-up for package demount using a semi-automated rework system. The PCB assembly was clamped on a motorized XY stage and a vision system was used to manually center the WLP between top and bottom heaters. Top heater convection was localized using a 10-mm nozzle attachment. The nozzle was lowered onto the board, and an automated recipe was used to heat the part to reflow temperatures. To prevent thermal artifacts and ensure complete solder liquidation, the WLP was heated between 217 and 250°C for 60-90 s. At peak reflow of 235–250°C, the WLP was lifted from the PCB using vacuum suction through a metal pick-up tube. Figure 6 shows a 3.5 mm vacuum cup that was used to minimize mechanical stress to the WLP silicon backside.

In order to accurately measure the WLP solder joint temperature, a board assembly was

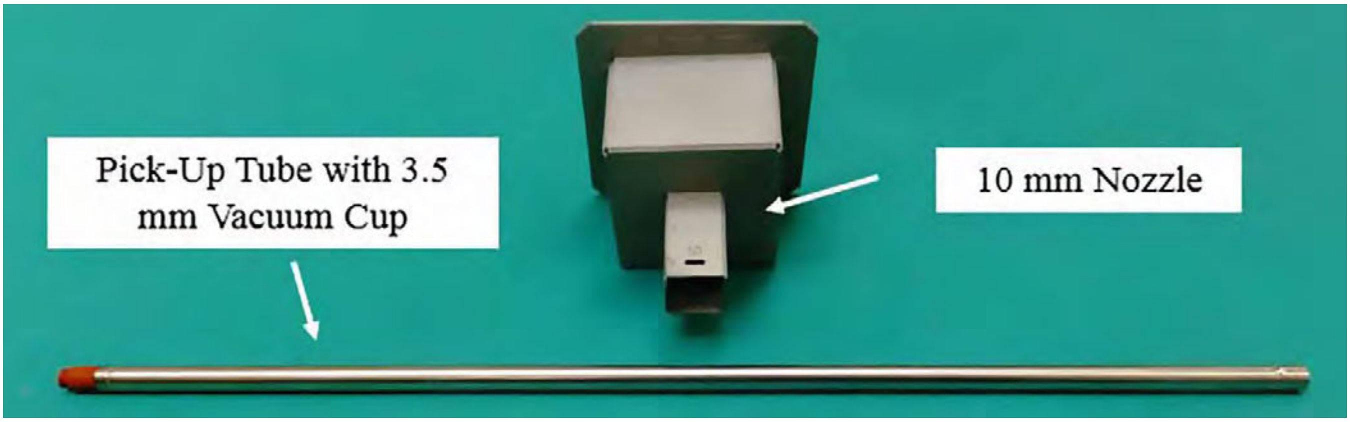


Figure 6: Photograph showing the 10 mm nozzle, metal pick-up tube, and 3.5 mm cup used during vacuum pick-up of the WLP.

sacrificed for temperature profiling. A WLP was demounted using a test recipe, and holes were drilled through the WLP board-side pads at the center, top right, and bottom left corners. Thermocouples were inserted through the backside of the PCB, until flush with the board-side pads. The thermocouples were then bonded and cured using a thermally-conductive epoxy. After the thermocouples were attached and tested, the PCB assembly was clamped to the X-Y stage of the rework system. A thin coating of flux was applied to the WLP board-side pads, and a vision system was used to pick, align, and place a fresh WLP on to the PCB. The package was reflowed to the board, and heater times and temperatures were iteratively adjusted until the critical reflow parameters were satisfied.

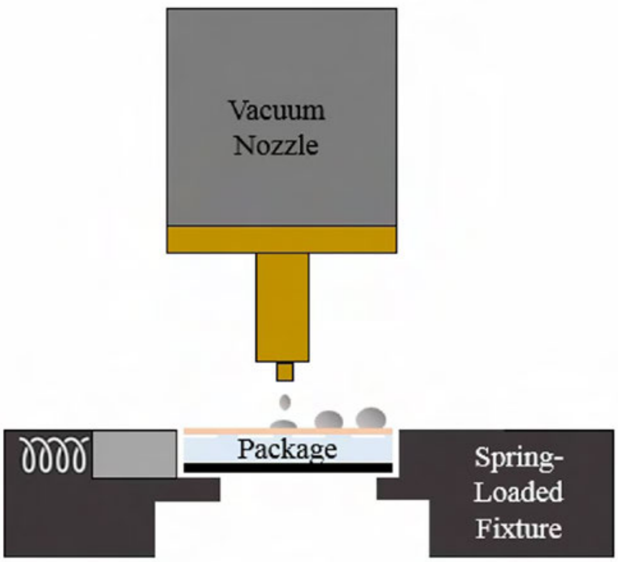


Figure 7: Schematic demonstrating the tool set-up for vacuum scavenging a WLP.

Package Desoldering

After package demount, residual solder debris must be removed to provide a smooth and even surface for reball. Conventional desoldering is performed using the solder wicking technique with a hot air pencil and braided wire. Alternatively, package desoldering was performed using a no-contact vacuum scavenging method that eliminates mechanical stresses and ensures repeatable temperature control. Figure 7 shows a schematic of the vacuum scavenge set-up, including the vacuum nozzle and custom fiberglass-resin fixture. The WLP was placed frontside up in a spring-loaded fixture and clamped to the rework stage. The top and bottom heaters were used to heat the component above solder liquidus temperatures while a vacuum nozzle descended 0.1-0.25 mm above the component. The molten solder debris and flux were then vacuum-suctioned in a pre-programmed XY raster pattern. Because the WLP is so small, only two passes were required to remove the residual solder from the package-side. The scavenging height and velocity, scavenge pattern, and top and bottom heater temperature were all controlled using a semi-automated recipe. To reduce artifacts and ensure liquidus temperatures, a test WLP was profiled by attaching a thermocouple to the component backside.

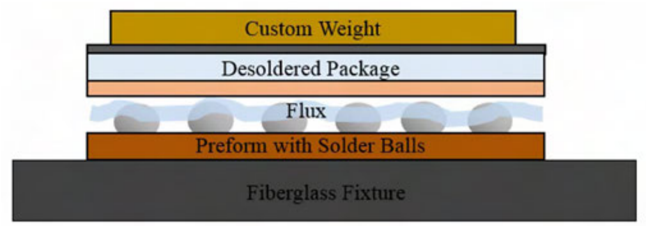


Figure 8: Schematic showing the reball stack-up.

Package Reball

Figure 8 shows a schematic of the preform process used to reball the WLPs. After desoldering the package-side, residual debris and flux were cleaned using a flux-off spray and a coarse-bristled brush. A custom solder preform was placed ball-side up on a fiberglass-resin fixture. A thin coat of flux was applied to the package-side, and the WLP was placed on top of the preform. To improve ball attach and prevent the part from blowing away, a metal weight was placed on top of the WLP and preform. The weight, WLP, and preform stack were reflowed using the rework system, then the weight and preform were carefully removed after the reballed package had cooled.

The entire stack-up was profiled by attaching a thermocouple between the preform and the fixture. The top and bottom heater temperatures and times were adjusted to meet the following critical process parameters: 60-90 s soak between 150°C and 217°C, and 60-90 s reflow between 217°C and 250°C.

Results and Discussion

Several board-assembled WLP units were used for rework and reball development activities. A demount recipe was created by profiling a PCB-mounted WLP and adjusting the top heater and bottom heater settings. Figure 9 shows the temperature profile obtained during demount. WLPs were successfully demounted using a peak temperature of ~235°C and a 70-s time above liquidus.

After demount, a recipe was developed to vacuum scavenge the solder from the package. A WLP was placed front-side up in a spring-loaded snugger inside a fiberglass-resin composite fixture. A thermocouple was attached to the silicon backside and used to measure the package

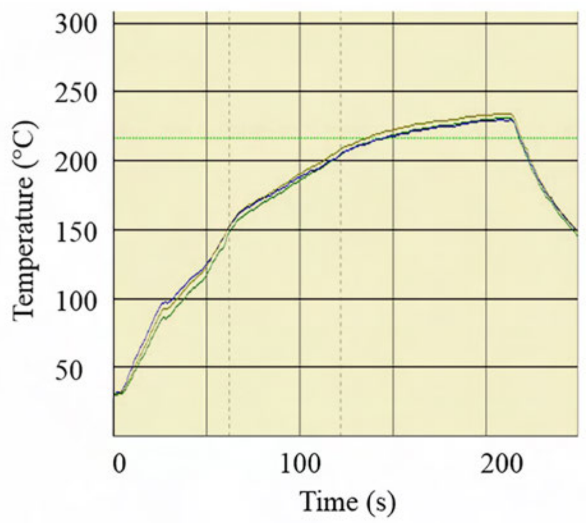


Figure 9: Graph showing the package temperature as a function of time during demount.

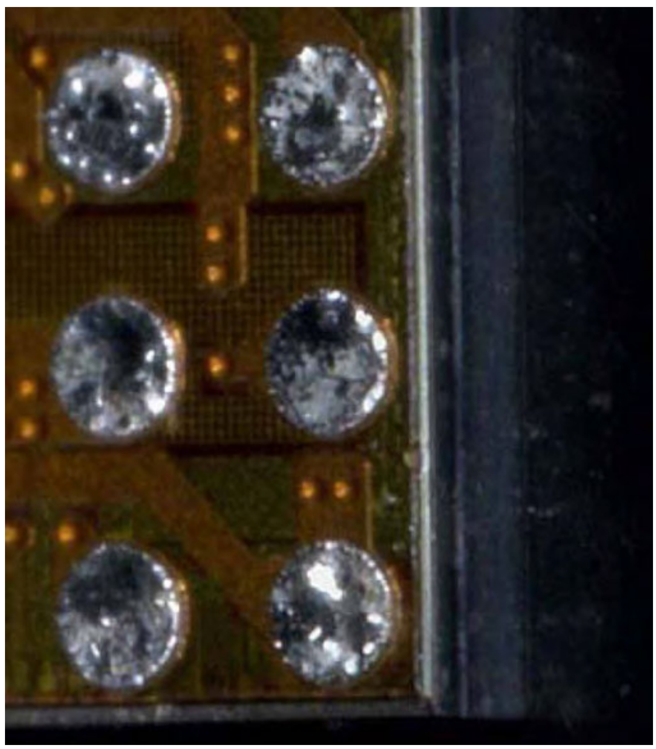


Figure 10: Representative microscope image showing WLP after successful vacuum scavenging. Only a thin layer of solder remains on the under-bump metallization.

temperature. Top and bottom heater set points were adjusted until the package temperature remained between liquidus and 240°C. Figure 10

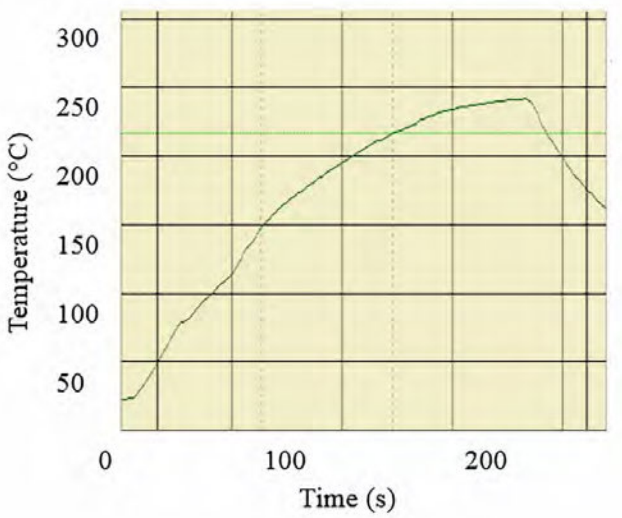


Figure 11: Graph showing the package temperature as a function of time during preform reball.

Figure 12: Representative microscope image showing WLP after successful reball.

shows a representative microscope image of one of the desoldered WLPs. Inspection showed the recipe provided adequate solder removal, with only a thin layer of solder remaining on the under-bump metallization.

Lastly, a reball recipe was created. The preform-package weight stack-up was placed on a fiberglass-resin fixture, and a thermocouple was mounted between the preform and the fixture. Top and bottom heater settings were adjusted until the package achieved the critical time and temperatures for soak and reflow. Figure 11 shows the WLP temperature profile during reball, with a ~240°C peak reflow temperature. Due to the low mass of the weight and WLP, the reball stack-up blew away during several reball attempts. Consequently, the air flow had to be reduced at the beginning and end of the recipe. Optical inspection showed the balls properly wetted to the under-bump metallization, as shown in Figure 12. No opens or shorts were visible on any of the inspected units.

CSAM and optical inspection were performed before and after the rework process. No thermal artifacts were found, but the following two mechanical artifacts were observed on multiple units: 1) peeling and chipping of the backside protective tape, and 2) chipping of the dielectric and top metal layers. Figure 13 a,b shows representative CSAM images of the package backside, captured before demount and after reball. Following reball, damage was detected at the interface between the backside protective tape and bulk silicon. Optical images confirmed that the backside protective tape chipped off and exposed the silicon, as shown in Figure 13c. Following a step-by-step investigation, it was determined that the backside protective tape was peeling and chipping after storing and removing the WLPs from adhesive packs. Though the tape chipping is cosmetic, care should always be taken to reduce artifacts and prevent masking of the true failure signature. Accordingly, the backside tape artifact was eliminated by storing subsequent samples in plastic trays instead of adhesive packs.

Frontside chipping was also detected during optical inspection. Figure 14 a and b reveals ~50 µm chips near the dielectric and top layer metallization. The chips were approximately the same diameter as the tips of fine point metal tweezers used during WLP handling. Chipped WLPs failed subsequent component-level test, suggesting that the artifacts affected the package integrity. Thus, the results show that front-

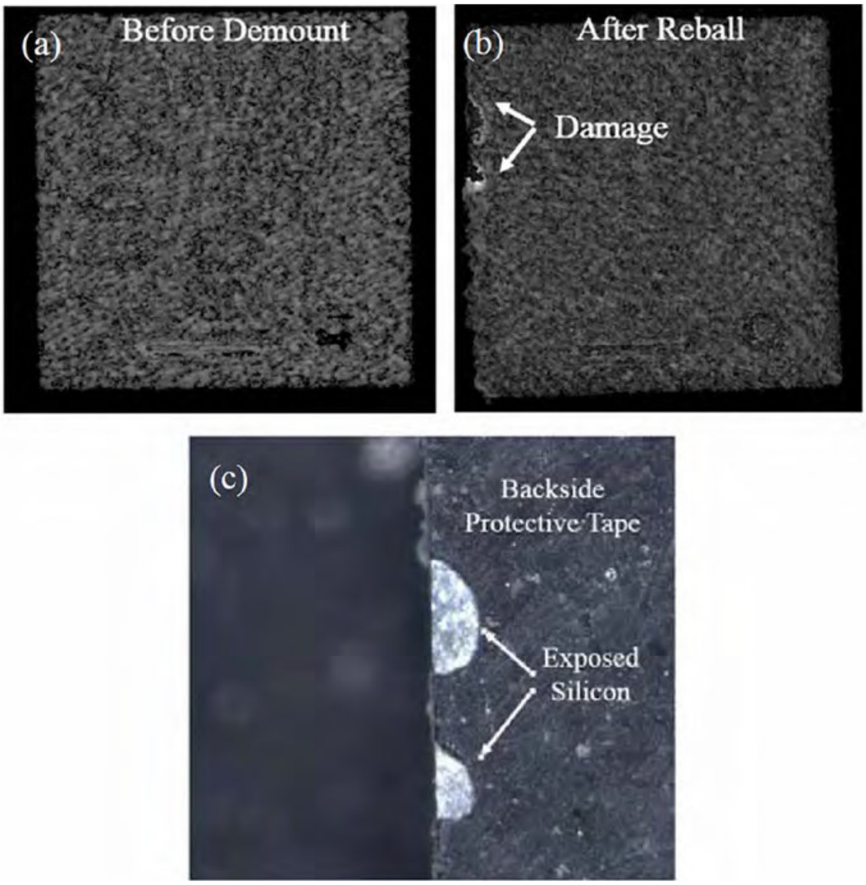


Figure 13: CSAM images showing (a) the package backside before demount, and (b) after reball. An optical image (c) shows chipping of the backside protective tape.

side chipping can not only mask the true failure signature but also induce failures during component-level testing. All further chipping was eliminated by handling WLPs with a vacuum pen and plastic tweezers. Table 1 summarizes all the rework-related challenges and risks discussed in this paper, and lists the implemented solutions.

Conclusion

Rework and reball recipes were successfully developed for board-assembled WLPs. OM and CSAM inspection were performed to evaluate the rework and reball process yield, and screen for thermally or mechanically-induced artifacts. The risk for mechanical damage was minimized by thermally demounting the WLPs with a vacuum pick-up tube and soft vacuum cup. Temperature was well-controlled using a no-contact vacuum scavenge technique to desolder the package. Lastly, the WLPs were reballed using a solder preform and a small metal weight. CSAM and OM did not reveal any thermal artifacts during the rework process, but chipping artifacts were found on the backside protection tape and near the dielectric and top layer metallization.

WLPs with frontside chips failed subsequent component-level testing, showing that small dielectric and metal defects can sacrifice electrical functionality. Both backside and frontside chipping artifacts were successfully eliminated by improving handling and storage techniques. By implementing similar rework and reball improvements, the industry will be prepared to support WLP FA while maintaining the true defect signature. SMT

References

1. TechSearch International Inc., “The Future of Packaging and Assembly Technology,” 2016.

Rework Step	WLP Challenge/Risk	Implemented Solution
Demount	Damage to the package backside or edges; risk of bumping adjacent components on high-density PCBs	Thermally demount package using pick-up tube with a small, soft vacuum cup
Desolder	Thermal artifacts from overheating the package	Use temperature-controlled vacuum scavenge method
Reball	Mechanical damage when part blows away; low ball attach yield due to insufficient force for ball adhesion	Use low airflow during reball; use metal preform weight to increase mass of preform stack-up
Handling/Storage	Mechanical artifacts from metal tweezers and tacky packs	Handle packages with plastic tweezers or a vacuum pen; use plastic tray or low-adhesive pack to store and transport packages

Table 1: Summary of challenges and risks associated with each rework step, along with the implemented solution.

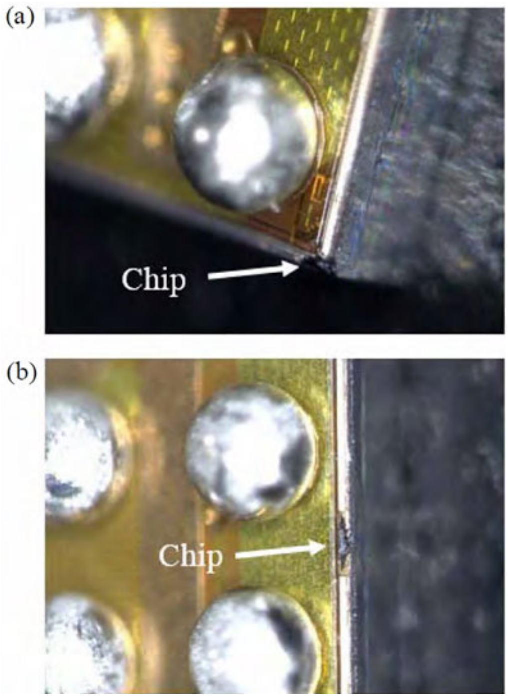


Figure 14: Representative optical images (a and b) showing chipping near the dielectric and top layer metallization.

2. Y. Li, P.K.M Srinath, D. Goyal, "A Review of Failure Analysis Methods for Advanced 3D Microelectronic Packages," Journal of Electronic Materials, January 2016, 116-124.

3. A. Wilson, "IR Cameras Tackle PCB Inspection Applications," 2007.

4. M. Pacheco, "Detection and Characterization of Defects in Microelectronic Packages and Boards by Means of High-Resolution X-ray Computed Tomography," IEEE Electronic Components and Technology Conference, June 2011, 1263-1268.

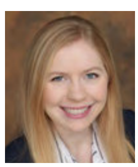
5. A.A. Primavera, "Process Issues for Fine-Pitch CSP Rework and Site Scavenging," EtroniX Conference Proceedings, 2001.

6. J. Wade, R. Aspandiar, D. Naugler, T. Leahy, "PCB Pad Site Dress Methods on BGA and Socket Pad Arrays," SMTAi Conference, 2010.

Acknowledgements

The authors would like to thank the teams from the Global Platform Analysis Center (GPAC) and Assembly and Test Technology Development (ATTD) FA Labs.

Editor's Note: This article was originally published in the proceedings of SMTA International.



Lauren Cummings is a failure analysis engineer at Intel Corp.

Priyanka Dobriyal, Ph.D., is a data center execution engineer at Intel Corp.

FEATURE

Top 5 BGA Challenges to Overcome

by Bob Wettermann
BEST INC.

BGA component package dimensions continue to get thinner as more are being used in handheld device applications. End-use device requirements include the need to maintain their interconnections, even when dropped, thus necessitating underfill. The increased demand for higher board densities requires neighboring or mirrored devices during the rework process to be more challenging. Higher reflow temperatures of lead-free rework increases the pressure for properly shielding the neighboring components. These developments are causing BGA rework challenges. This summary will discuss the most challenging aspects of BGA rework and options for solutions.

1 Warped BGAs

One of the challenges in reworking BGAs at this time is the warping of the packages as ever thinner packages lead to a variety of problems. A largely noted issue of a warped BGA is the 'Head in Pillow' (HiP) defect (Figure 1). This defect may or may not be detectable during the X-Ray inspection. In this solder joint defect, the solder paste deposit will wet the pad, but does not fully wet the ball. This is due to the ball of the package being 'pulled away' during the device warping. The result is a solder joint with enough of a connection to have electrical integrity, but not sufficient mechanical strength. Without the strength, these components may fail with a small amount of mechanical or thermal stress. This potentially costly defect is not

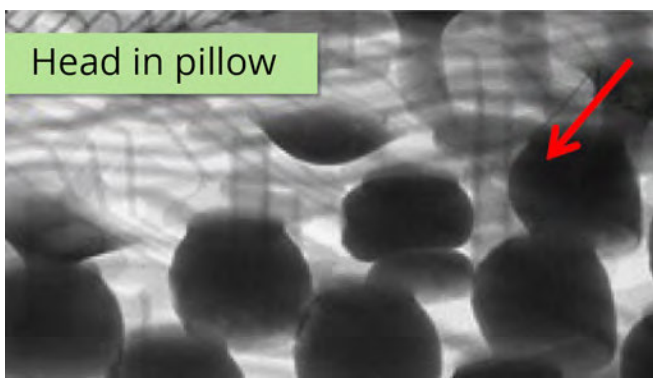


Figure 1: Head-in-pillow defect.

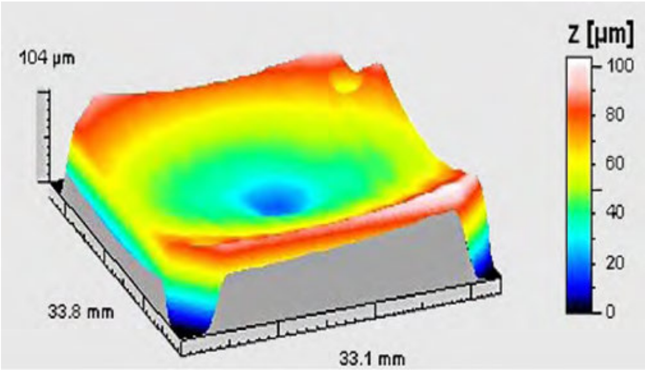


Figure 2: Warpage and Z-height deflection on BGA.

usually detected in functional testing but rather in the field after the assembly has been exposed to some physical or thermal stresses. Warping can also cause bridging and shorts, at either the outer corners or the center of the device during replacement (Figure 2). This warping phenomenon can cause the center of the BGA to bow upwards and the corners down, or vice versa. Sometimes, this is enough to cause the corners to move closer to the circuit board surface. This puts extra pressure on the corner solder joints. Later in the lifecycle of the device, this may cause shorts or cracks.

There are several fine tunings of the rework process which will mitigate the impact of warped packages. The main way to lessen the impact of warping includes the adjustment of the reflow profile and solder paste chemistry. The reflow profile will help determine which areas of the device may be subject to thermal stress as well as ensuring the flux activity level does not expire. The solder paste chemistry is an integral step in making sure there is plenty of flux activity if the warping occurs over a prolonged reflow cycle. These variables are important to control during the BGA rework process to minimize warping.

By aiming for a very small temperature differential across the entire BGA package—less than 10°C across the entire package is optimal—the impact of device warpage can be greatly reduced in the rework process. One of the methods for ensuring a consistent and small temperature gradient across the entire package is to use a programmable multi-zone bottom-side heating source (Figure 3). Ideally, a multi-zoned heating source will heat the underside of the board to 100–120°C (lead-free processing temperatures) with the device location elevated to 140°C if the board and components can withstand this. This slight temperature differential will ensure that there is not undo thermal stress, which may delaminate or warp the board. The heating nozzle (assuming hot gas is used as the reflow source) will bring the solder balls up to 20–30°C above liquidus for 60–120 seconds.

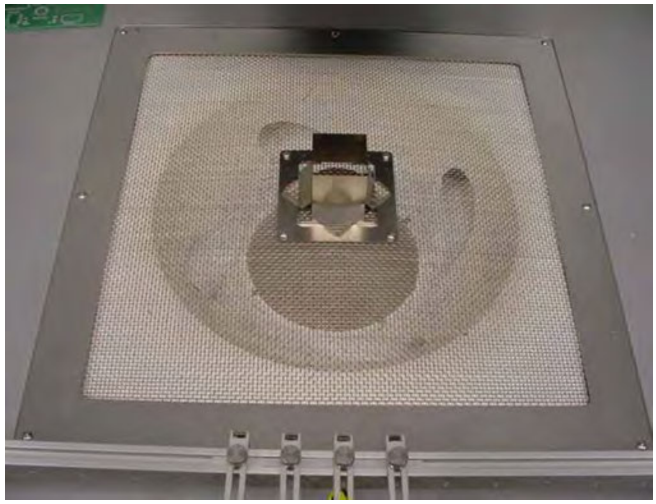


Figure 3: Multi-zone bottom heat of BGA rework system.

In addition to the proper removal and reflow profile, the PCB will need to be properly supported to mitigate any effects of deflections on the PCB during the removal or reflow profiles. Board supports should be such that they prevent undue board deflections. An example of such a board holder can be found in Figure 4. The lack of support further exacerbates warping which may occur.

Solder paste chemistry can impact the degree to which the device or PCB is warped during the rework process. Solder pastes, with an activation system that can provide sustainable high-temperature fluxing, can create a homogenous connection. This connection goes beyond the ball and the paste alloy interface, which is important for warped devices to form an intermetallic bond. Those that are not able to sustain high-temperature efficacy are more prone to HiP defects.

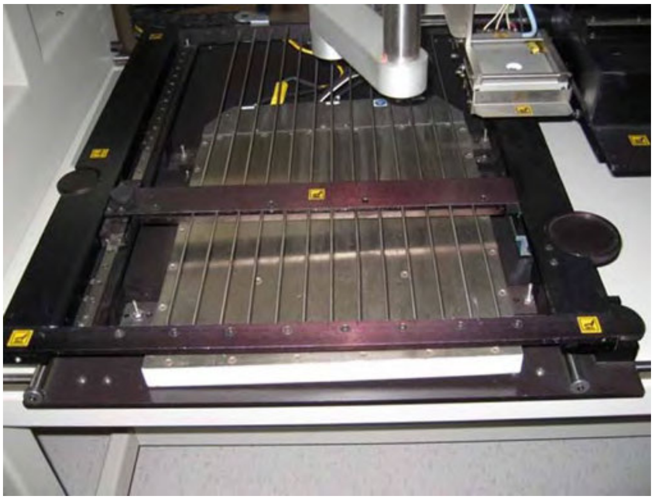


Figure 4: PCB support on BGA rework system.

2 Neighboring Device Damage

As the density of components on PCBs has increased, the need to protect neighboring temperature sensitive components near the BGA such as ceramic capacitors, crystals and plastic-bodied components such as connectors has increased. These devices must be protected from exposure to heat during the rework process. If they are not, they can become damaged showing either visible or 'hidden' damage. In addition, these components' long-term reliability may be impacted by this heat exposure, even if their appearance does not show it. While these components may be able to withstand the peak temperature of 260°C (as defined in J-STD-002), there may be medium and long-term impacts to its reliability if the IMC layer grows too thick. Neighboring underfilled parts may have the material 'ooze out' as the softening point temperature is below the liquidus temperature of lead-free solder.

There are a variety of shielding options in and around the BGA rework area. The increased liquidus temperature of lead-free solder has driven processing temperatures into areas where sensitive components have significant body temperature and time limitations (IPC J-STD-075 is the standard for maximum time/temperature exposure for all non-semiconductor devices). The intermetallic layer thickness, which to some degree represents the mechanical strength of the solder joint, can become too large with extended exposure to times above liquidus. If it becomes too large it can make the solder joint brittle. This in turn can impact the reliability of the solder joint.

To prevent these negative impacts on neighboring devices in the BGA rework area, proper thermal shielding is needed. A recent study (Wettermann, 2015) indicated that the shielding effectiveness of 'historical' materials, such as Kapton™ tape and stainless steel, are not as effective as more modern materials such as shielding clay gel (Figure 5) and ceramic non-woven ceramic materials. To fully protect a device from thermal damage, the study pointed out that the clay gel material is over two times as effective as Kapton tape as a thermal shield at a close distance, and three to four times as effective at further distances. The ceramic non-woven fiber material is nearly as effective as the gel in terms of its heat withstand properties, but does not need to be cleaned off after use.

Trending devices, such as smartphones and tablets, use underfill so that the BGA package can withstand drop testing requirements without damaging the solder joints. The challenge for a rework technician is the pliable nature of the underfill. This typically means the tack properties, even when above the softening point, make for a mess underneath the BGA. Even if the underfilled BGA can be pried off the PCB, the mechanical force exerted can potentially damage the device or board.

3 Underfill Rework

The softening point of the underfill is less than that of the reflow temperature

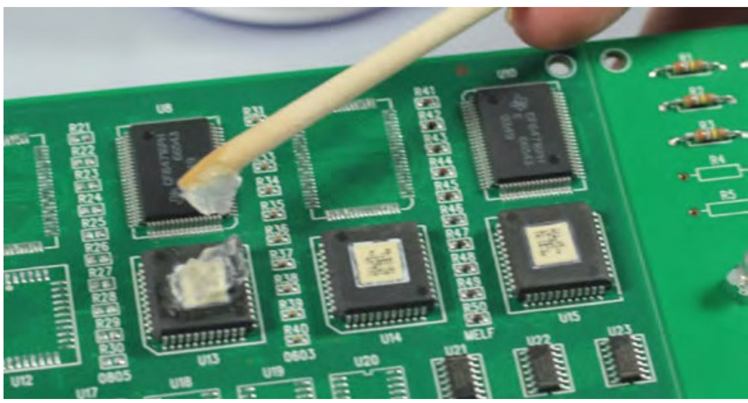


Figure 5: Clay gel protects and shields devices from thermal damage.

of the PCB device. This means that under the BGA, as well as any non-protected device, the underfill softens and expands prior to the solder reaching liquidus state. This along with the resulting tackiness presents challenges in the removal of the device. During removal, the underfill will squirt out as local pressure pushes out the solder when it reaches reflow temperature. The result is a mess in the underfilled device being reworked. Due to mechanical force, either through prying with a lever arm or a specialty nozzle in removing the underfilled device from the PCB, the board may end up with extensive damage. Due to the mechanical force, either through prying with a lever arm or a specialty rework nozzle in removing the underfilled device from the PCB, the board may end up with extensive damage (Figure 6).

In addition to this prying action causing damage to the PCB there may be damage around and underneath the area of the device in removing the underfill from the PCB. This damage may be caused by the solder wick or nozzle, which may scratch or damage the pads of the solder mask when removing remnant underfill. In addition, the tack adhesive strength of the underfill may be of such a high value that the pads are pulled off the board. This phenomenon may be most pronounced for pads that are no-connects underneath the BGA.

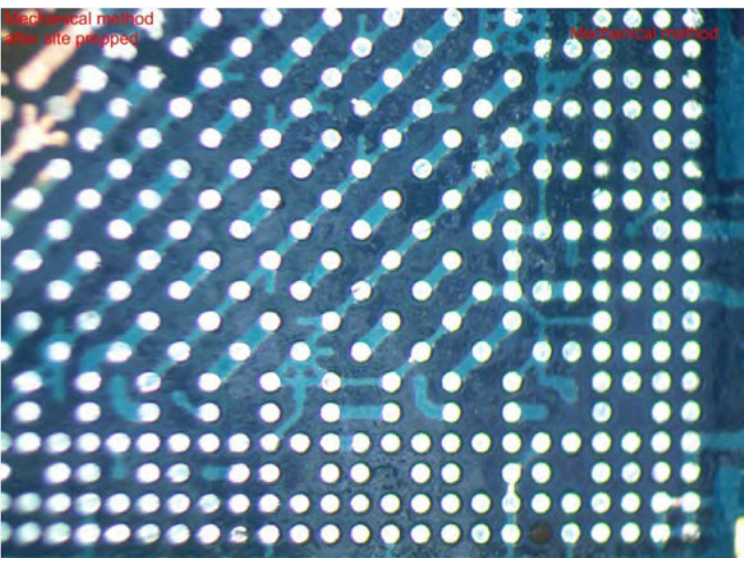


Figure 6: Mechanical grinding of underfilled BGA results.

One of the ways to overcome the extensive damage caused by preparing the BGA site location after device removal is using a high-speed milling system. In this approach, no direct heat is used to soften the underfill, but rather a high-speed milling operation will grind off the cured underfill material as well as the remnant solder balls. This requires precision in this mechanical operation (Figure 6).

By not grinding far enough, it will leave too much of the underfill at the BGA device location making the pads non-solderable. Care must be taken during this rework method to ensure the mechanical vibration, and stress of rework, does not cause a decrease in the reliability of the PCB.

4 Extensive Solder Mask Damage

Solder mask damage underneath a BGA location occurs due to several reasons. This damage is in the form of missing mask or a breakdown in the mask adhesion to the PCB. This can be caused by using solder braid during the site prep process, an uncontrolled heat source to remove the BGA, an abnormally high number of heat cycles applied to the PCB or by poor initial solder mask adhesion. The resulting problems upon component replacement is solder flowing down the dog bone pattern and ‘starving’ the solder joint/flow underneath. The poorly adhered solder mask will cause solder shorts or other soldering anomalies.

Solder mask can be repaired via a variety of techniques, each with its own advantages and disadvantages. A simple technique for spot solder mask repair is using a repair pen (IPC 7721 2.4.1), which is typically cured by air drying or a bake-out cycle. Another method, as outlined in IPC 77212.4.1, is via the use of liquid solder mask. This can be spread onto the areas that need repair. It is then either heat or UV-cured. Another technique, which repairs the mask underneath the BGA, is a stay-in-place stencil. This serves as a reliable way to place the BGA while simultaneously repairing the mask. Lastly, there is the mask repair stenciling technique. This method saves repair time as an ultra-thin stencil defines the area where the mask is repaired. Replacement mask material is then squeegeed into the apertures and then cured. Post curing,

the stencil is peeled away, leaving hardened replacement mask in its path.

Solder mask repair pens are labeled as simple-to-use PCB repair tools which can replace solder mask. The pens can be simply drawn across the areas requiring solder mask. The liquid oozes out of the soft-tipped pen and then can be air or heat-cured. The pen tips themselves are large with respect to modern BGA pads site pitch, making it a challenge to precisely dispense the mask material. Due to the porous nature of the dispensing tip, it tends to pick up debris from the board (including flux residue, remnant mask and cleaning agents). The soaked up debris then can re-contaminate other areas of the board. The skill level for someone making solder mask repairs using this technique will be at the advanced level; however, the repair quality will tend to be low.

The most common method used for IPC Class 2 and 3, if allowed, solder mask repairs is via the use of liquid replacement solder mask. In this method, a skilled technician selectively brushes/dabs a small amount of solder mask onto the damaged areas underneath a BGA (first removing the BGA) being careful to not get the material onto the component or solderable areas. Depending on the type of mask used, this mask can then either be heat or UV-cured. On the fine-pitched devices of today the exacting placement of the replacement mask requires a great deal of dexterity, requiring the use of a microscope.

As a time-saving enhancement to the above technique, a stencil can be designed and fabricated using the GERBER files of the board. This will help selectively cover solder mask underneath a specific location underneath the BGA. The stencil is peeled off its carrier backing, aligned, then placed on to the PCB surface. Replacement mask is squeegeed with a micro squeegee across the surface of the stencil and then cured. After curing, it is removed in an ionizing environment as not to cause any latent static charge damage to the components in the area. This method, while time saving for multiple boards requiring the exact same area of repair or for a very complex large area of repair, requires a repair technician with an advanced skill level.

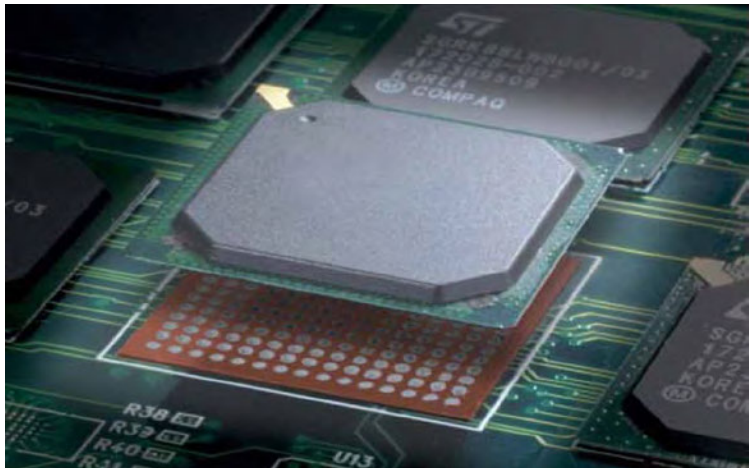


Figure 7: Stay-in-place stencil for solder mask repair.

The last approach to repairing solder mask is using a semi-permanent stay-in-place BGA stencil. This stencil, while having the benefit of being a simple way to place a BGA, also provides isolation between pads and prevents shorting between the IO. This will fix the standoff height between the base of the BGA and the PCB to control collapse height, while serving as a mask band-aid. Once in place the stencil acts like a solder mask repair stencil (Figure 7). This allows even the beginning repair technicians to repair damaged solder mask underneath the BGA.

5 Pad Damage

Another common trouble spot is the potential for pad damage while the BGA is being reworked. Pad damage is usually the result of improper site preparation which can be a result of numerous processing problems. Items on this list are contaminants on the solder wick, improper tip temperature, too much pressure of the soldering iron on the solder wick material, improper solder tip selection or expired flux material. Improper temperature profiles found in the BGA removal process would also be a contributing factor to pad lifting. Finally, there may be cases where the original adherence of the pad to the laminate was insufficient due to problems in fabricating the PCB.

The proper procedure for the preparation of BGA pad sites after a BGA has been removed is outlined in IPC 7711 procedure 4.1.3 and re-leveling of the pads is found in 4.2.1. The improper method for pad leveling involves 'scrubbing the deck.' This occurs when the wick is pushed back and forth along the underside area of the BGA pad site. This can result in the mask being scratched and pads being bent up or lifted off. The proper technique (Figure 8) calls for the solder braid to be moved in an up and down fashion onto the pads thereby not scratching the surface or prying the pads up.

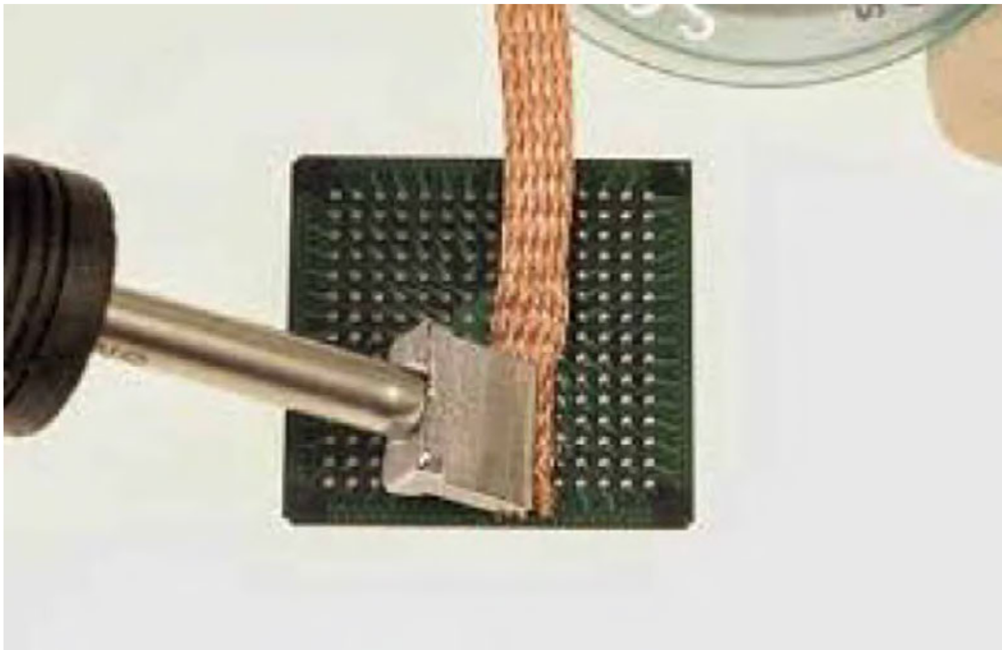


Figure 8: Proper site preparation technique eliminates mask and pad damage.

One way to overcome the problems associated with these contact types of pad prepping processes which rely on operator skill is to use a non-contact method for site preparation. Several higher end rework systems are now equipped with programmable non-contact scavenging systems. In these systems, a heated nozzle comes in to proximity of the PCB to reflow the solder, while at the same time following the contour of the PCB surface and vacuuming up the molten solder from the board. This way results in no damage to the pads or board surface. In addition, the skill level of the rework technician is removed as a variable. The downside of this approach is lessened throughput as both the programming time of the scavenging system and the extended cycle time of the scavenging operation makes this somewhat cumbersome for most rework.

The proper BGA removal profile needs to be developed to make sure the removal of the BGA will not unnecessarily cause pad lifting for removal of the BGA. The process for developing such a profile is like that of profiling a PCB for assembly, only done in reverse and on a smaller scale. First, a solder sample board is analyzed to determine the proper location of the various thermocouples. Typically, one is embedded in the die of the BGA, one each in two corner balls, one or more on the neighboring parts and one or more scattered throughout the BGA ball pattern depending in the idiosyncrasies of the PCB's thermal characteristics. Attachment of the thermocouples includes drilling and gluing them into the board, the solder balls, and the actual die itself. After this the technician dials in a reflow profile based on experience. Solder profiles are developed and the temperatures at these locations are measured. From there, adjustments to the profile, removal of neighboring parts, or proper heat shielding will fully optimize the profile for minimized reflow time and damage to the neighboring components, while gaining the most consistent collapse of the solder balls. Bottom-side heat is especially necessary with thermally massive boards or for those processed using lead-free solder. This will prevent thermal damage to the PCB if the rework process is being done in higher liquidus temperature solders such as lead free. Multi-zone bottom-side heaters are sometimes necessary for higher layer count boards and to maintain a smaller temperature differential over the entire component area. Finally, the proper board support will help prevent warping of the board.

If the pads have been turned up by more than one pad thickness or have been partially or completely ripped off the board there are two basic methods of repair as outlined in the IPC-7721 board level repair guidelines. In one method a two-part epoxy is used, while in the other a pre-adhered dry film adhesive is used.

The two-part epoxy (IPC 7721 2.6-epoxy mixing) method for pad repair is outlined in the IPC-7721 Procedure 4.7.1 Surface Mount Pad Repair, Epoxy Method. It is the most reliable method for pad repair. This requires a higher degree of skill and patience by the technician. In this method, the site is prepped for the new pad by removing the existing pad or pad/trace combination with a sharp knife. After cleaning the area, the proper replacement pad or pad/trace is soldered to the existing board using a lap solder joint. The two-part epoxy is mixed per the manufacturer's recommendations on a flat plate where the mixture can be seen (a glass plate is easiest). Using a wooden orange-wood stick, a thin layer of this two-part mixture is then placed underneath the replacement pad or pad/trace area and clamped using a non-stick surface clamp to hold the replacement pad or pad/trace to the PCB during the curing process. Curing per the epoxy manufacturer's direction, which is usually accelerated to some extent by elevated temperature conditions, will then complete the process. Prior to implementing the final step of overcoating with solder mask over the trace area and/or up around the periphery of the pads to gain some adhesive strength, the continuity between the various conductors involved in the repair process should be confirmed.

The dry film method for pad repair is outlined in IPC-7721 Procedure 4.7.2 Surface Mount Pad Repair, Dry Film Method. It is the cleanest of the two approaches and requires a high degree of dexterity to perform. The pad and trace preparation process as described previously is used in this method. However, when cutting out the replacement trace and film, great care needs to be taken in making sure that the replacement cut out dry film is adhered everywhere on the bottom-side of the foil. If a trace section needs to be lap soldered to that section on the board, the technician needs to make sure that the overlapped section has the dry film on the board. Once it is affixed in position, the replacement materials will have the heated tip of a curing iron sized over the bonding area. While being adhered, the curing temperature needs to be confirmed, as both the correct temperature and pressure needs to be applied to get the cure right. Cleaning, testing, and inspection are the same as in the case of the epoxy repair described above.

Conclusion

The above discussion is a snapshot in time with respect to the top BGA rework challenges. These challenges, in no order, were that of: excessive BGA warping due to thinning packages, shielding of neighboring devices in an era of increasing component density, underfilled BGA device removal and replacement, as well as the repair of solder mask. In addition to these current challenges, others including reworking ever-finer devices pitches and integrating lower reflow temperature solders are rework trials that will be added to this list soon. SMT

References

1. Gregory L. Tonkay, Robert H. Storer, Ronald M. Sallade, and David J. Leandri, "Critical Variables of Solder Paste Stencil Printing for Micro-BGA and Fine-Pitch QFP," IEEE Transactions on Electronics Packaging Manufacturing, Volume 27, No. 2, April 2004.

2. Garcia, Omar, et al, "Selective Reflow Rework Process," IPC APEX EXPO Proceedings, 2015.

3. Wettermann, Robert and Gaynor, Adam, "Effectiveness of Different Materials as Heat Shields during Reflow/Rework," IPC APEX EXPO Proceedings, 2015.

4. Luetzlow, Norbert and Jahal, Kiuldip, "Quantifying Performance of Mechanical and Chemical Processes for Pre-treatment Prior to Solder Mask Application," IPC APEX EXPO Proceedings, 2013.

Editor's Note: This article was originally published in the proceedings of SMTA International.

Bob Wettermann is the principal of BEST Inc., a contract rework and repair facility in Chicago.


LED A.R.T. Symposium
ASSEMBLY | RELIABILITY | TESTING
November 28 - 30, 2017
Archie K. Davis Conference Center
Research Triangle Park, NC
LEADING TOPICS
LED Applications
LED Packaging
Failures & Failure Mechanisms
LED Solder Joint Reliability
LED Processing
REGISTER NOW!
www.SMTA.org/LED
SMTA
Jenny Ng
952-920-7682
Jenny@SMTA.org
calce

Electronics Industry News
Market Highlights

Average Contract Price of PC DRAM Modules Posts Sequential Monthly Gain in July

The average contract price of PC DRAM modules rose by nearly 40% sequentially in the first quarter to $24 and then by more than 10% sequentially in the second quarter to $27, according to TrendForce.

3D Printing Market Worth $23.8B by 2025

The global 3D printing market is estimated to reach $23.79 billion by 2025, according to the new report conducted by Grand View Research Inc.

e-mobility: The New Eldorado for Li-ion batteries

e-mobility overtakes the consumer electronics market segment to represent 72% of the total rechargeable Li-ion battery cell market's value in 2022, according to Yole Développement.

Global Market for Smart Manufacturing Solutions to Top $320 Billion by 2020

TrendForce forecasts that the size of the global market for smart manufacturing solutions will surpass $320 billion by 2020 as manufacturing companies in various industries, following the Industry 4.0 conceptual framework, embark on a mission to transform their operations by deploying smart technologies.

Enterprise 3D Printing Strengthens Position in Aerospace

The market for 3D printers is set to change over the next 10 years as the Federal Aviation Administration (FAA) and the European Aviation Safety Agency (EASA) approve more 3D-printed parts for use in commercial jet engines.

Smart Speaker Market Forecast to Grow at 50% CAGR from 2017 to 2024

From a valuation of $400 million in 2016, the smart speaker market in the next seven years is forecast to outpace all records by collecting a revenue of $13 billion by 2024, according to Global Market Insights.

Semiconductor Manufacturing: What Is Driving the Growth of the Glass Material Market?

The 8-inch equivalent glass wafer market is expected to increase at a 23% CAGR through 2022, reaching around 14M 8-inch eq wafer, as glass materials make serious inroads in the semiconductor market according to Yole Développement.

Wearable Devices' Expansion to Industrial Sector Thrives with Addition of Advanced Sensors and Software

The emergence of the Internet of Things (IoT) and workers' need for real-time data, monitoring and tracking are boosting the development of wearable technologies for the industrial sector.

Local Smartphone Brands Facing Increased Competition in Indonesia

The smartphone market in Indonesia has changed with the China-based vendors becoming more aggressive with their aggressive strategies, not just with their product line-up but also their overall marketing plans and activities.

Global Defense Exports Expected to Decline for First Time Ever

Weakening defense export order backlog points to a contraction in the market by 2018, according to the annual Global Defense Trade Report released by IHS Markit.

ARTICLE

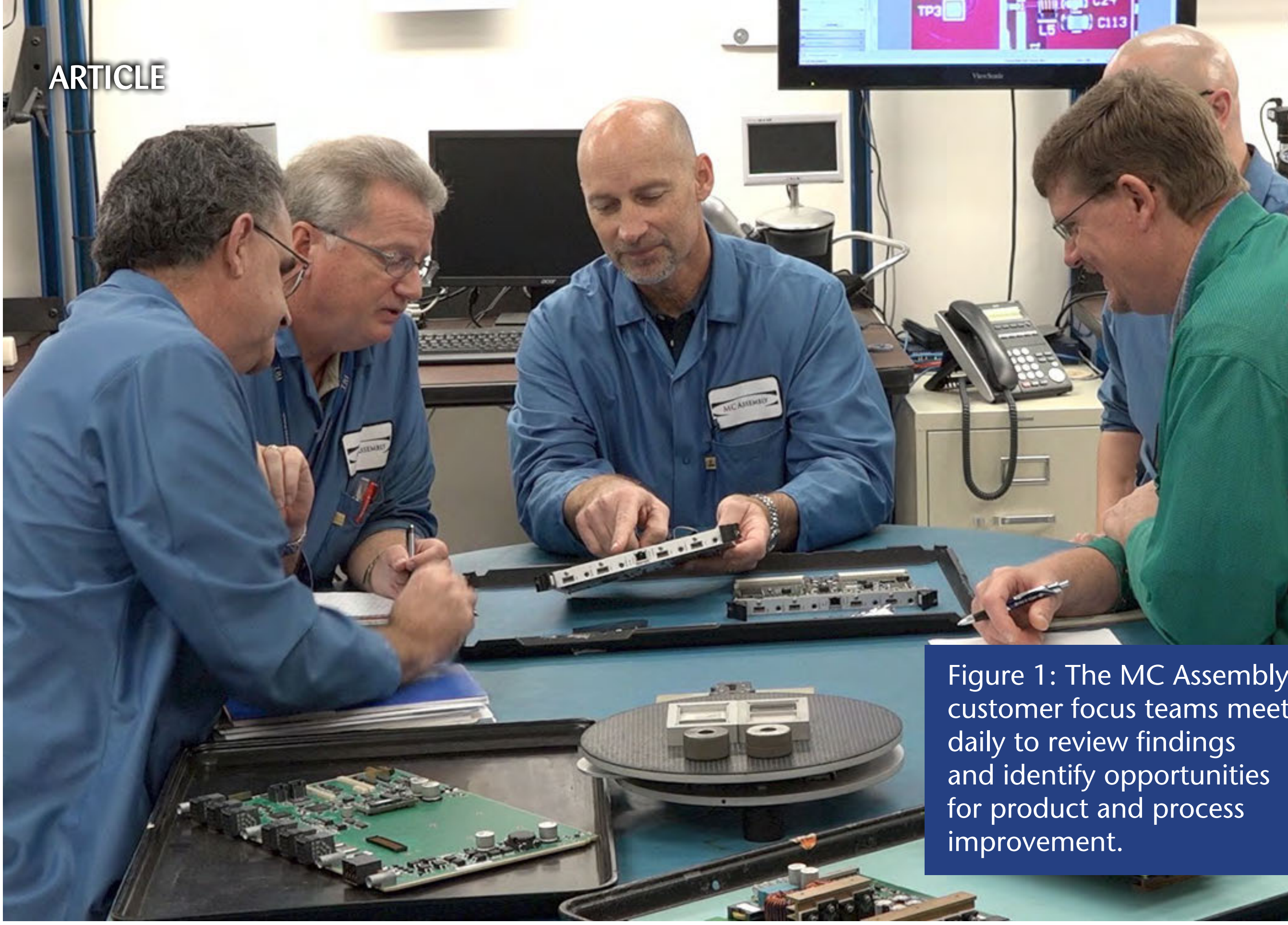


Figure 1: The MC Assembly customer focus teams meet daily to review findings and identify opportunities for product and process improvement.

IMPLEMENTING A CAPACITY PLANNING TOOL

by David Prunier
MC ASSEMBLY

So, you have a wedding coming up. Among the struggles of deciding what colors the bridesmaids are going to be wearing and who gets to sit next to eccentric old Uncle Russ, you may have had to stop and ask yourself how many people can fit into the church? Then how many people can fit into each pew, (comfortably) and especially, who can endure Uncle Russ for an hour. This little exercise of determining how many relatives, friends and strangers can fit in the church is in its simplest form and example of capacity planning. For the benefit of our readers, this discussion will focus on the use of capacity planning (CP) in the context related to contract manufacturing. Uncle Russ symbolizes the unknown constraints that may influence your ability to meet customer's demand, which a good CP tool should take into consideration.

In our first example of determining how many people would fit in the church, we were doing a rough-cut capacity plan. Finite capacity planning (FCP) was determining how many people could fit into each pew, seat or bench. Unfortunately, not all CP is that simple.

For those who grew up in manufacturing during the 1980s, you probably remember the term MRP II. Manufacturing Resource Planning or MRP II is not to be confused with Material Requirements Planning (MRP). One is the software used to manage the inventory, materials purchasing activities and production plans to meet the customer delivery dates (MRP) versus the methods used for efficiently managing the manufacturing resources of the company (MRP II). We are not going to bore you with the details behind each terminology but rather we want to focus in one of the important elements of MRP II where we see most EMS companies struggling. We will focus our discussion in the Capacity Planning process under the MRP II method. If you would like to learn more about MRP II, we suggest you read the book "The Oliver Wight Class A Standard for Business Excellence".

Figure 2: Scanning points at each step in the operation allow tracking of product flow and cycle times and provide traceability of each unit as it moves through the operation.

One of the more common challenges we see in the EMS world is that through the outsourcing of their manufacturing, many OEMs have forgotten the fundamentals of supply chain management and expect quick turnaround on orders without taking into consideration the whole supply chain constraints or the impact of not providing accurate forecasts to the EMS partner. Old Uncle Russ can, too easily, disrupt a great capacity plan if we ignore the possibility of his visit! In this paper, we will talk about some of the fundamentals but also about possible solutions in the reality of a not so perfect world.

CP is important to us in the contract manufacturing or EMS world for several reasons. It helps in level loading our factory, it helps us balance demand with available capacity, it helps to identify bottlenecks-those obstacles that might otherwise impede the flow of product and most importantly it helps us to improve our on-time delivery performance; something both near and dear to our customers and ourselves in the EMS world. If you've read anything regarding the "Theory of Constraints," you know how important it is to identify all potential and existing bottlenecks associated with the flow of product. This may also include all the process steps concerned with external operations within your supply chain as well.

CP can concern itself with labor, design and machine capacity. There are several key assumptions that must be made for CP to work properly. These serve as an excellent starting place for those interested in developing a good CP model. These are the following core assumptions:

1. All material is available when needed.
2. All machines are up and running effectively.
3. All labor standards have been reviewed and validated.
4. All part numbers/model numbers are accurate.
5. There are sufficient available resources to operate equipment, run planning tools, complete tasks.
6. All appropriate work centers have been identified.
7. All available resources are identified in each work center.
8. Queue times are identified. All wait periods, set-up, transfer times, transaction times and transport.
9. Management support for implementing the tool is given and there is a champion for the project.

You may find that you have your own site-specific gates to making sure that the plan can work effectively, and this should be included in your overall assessment and timeline when undertaking this project. The nine assumptions listed above should get you most, if not all the way there.

How many of us in the EMS and OEM worlds have found ourselves wrestling with a master scheduler or planner to have their product put in the queue only to have it bumped or find out that something else prevented it from being run in the time slot allotted? Uncle Russ always shows up at the most inopportune time! This problem is a very common one, almost as common as finding out that most EMS providers using an MRP system also have a CP module available to them but chose to either selectively use its outputs or to ignore its existence completely.

We have found many of our OEM customers do not have a good integrated capacity planning process. Forecast information may be unreliable or nonexistent because of many companies migrating to a "just in time" philosophy—without buffering capacity to accommodate unplanned demand fluctuations (Uncle Russ making an unannounced visit!). As such, we as EMS providers need to adjust and adapt to this new trend or will suffer the consequences including loss of business.

Master scheduling is a considerable task all by itself, not using a CP model in conjunction with the MRP tool can be a considerable waste of time and can be very detrimental to those concerned with meeting production schedules. The master scheduler or planner needs to know at the time an order is taken or being proposed what the next available slot or opening in manufacturing can be and what priority the order may have relative to existing orders already confirmed. How else can an accurate delivery date be predicted let alone be committed to? To not do so assumes that you have infinite capacity available to you, and we all know that capacity is always finite. Capacity equates to cost and cost must always be covered by price so understanding one's capacity and scheduling within the confines of capacity is as much of a prudent cost consideration as it is a customer service requirement. The large, Tier-1 EMS providers have the luxury of dedicating specific production capacity to specific customers. Their sloppiness in production planning is masked by the repetitive nature of large manufacturing runs while the costs are inevitably passed back to the customer who is basically "renting" the production capacity. In the high-mix/low-volume environment of the mid-tiered EMS world, capacity must be constantly planned and flexed over a broader customer base. The ability to do so offers a competitive advantage to the better mid-tier EMS partners.

Now having made up your mind to commit to a CP model, determine what platform you will run it on. This can be something as simple as a manual system, spreadsheet or database. More sophisticated models will employ the use of a classical MRP system or a custom or "canned" software tool. There are several that exist today. A word of caution, before investing heavily into an off the shelf software tool: it would be a good idea to determine how easily the data you will load can be transferred into a more permanent system later. Look for a system that will work well out of the box without having to manipulate it or customize it greatly. This will save time and numerous man-hours on the front end of your implementation plan. In our case, (and most likely in your case despite the ERP platform your company has) we historically used spreadsheets to fill the gaps in our CP process. We recognized the flexibility obtained by using spreadsheets. As an enhancement to infuse efficiency into the capacity planning process, we have invested in VENA, where we can control and share spreadsheets for many of our business functions. This makes the user interface easier to adopt and offers the ability to better integrate the capacity planning into our broader business applications.

Once the determination of the platform is accomplished, return to the nine assumptions given earlier in this article as the framework for a possible implementation plan. Let's take one at a time and discuss the intent or plan behind each one.

1. Ensure that all material is available (input).

Nothing can stop a 2,000-lb car from moving better than a missing five-cent piece of hardware. This is the theory here as well. To plan appropriately, all production work going into the plan cannot be plagued with constant starts and stops. Material shortages effecting a work order or kit will have a serious "trickle down"

Figure 3: Workers using precision equipment to assemble medical devices.

effect to everything lined up behind it. This creates the instant need to reschedule everything else and changes our available outlook on capacity. It may also add unnecessary overtime or temporary labor to accommodate the change. A robust clean-to-build tool is essential to ensure your material readiness.

A model within your material portion of this plan should address how material is kitted or staged for production in such a manner as to not impede the production plan. If people must stop to hunt down material or look for missing parts when the available time slot has arrived, then the time spent looking for the material is now eating into your available capacity and effecting your standards as well. At MC, we have invested in Rapid Response from Kinaxis. This is an advanced planning tool bolted to our MRP system where you can do multiple simulations without changing your live MRP data. We run material "what ifs" simulations to determine the projected date for all material availability at the site. With this information, we can then make a high-level prediction on when we most likely will complete the order based on our existing capacity state.

Obviously, what tools you use to develop these material strategies to reduce shortages can vary. This article is not intended to address the particulars surrounding the corrective action, only to point out the area of concern and highlight it as an area of concern when implementing a CP tool.

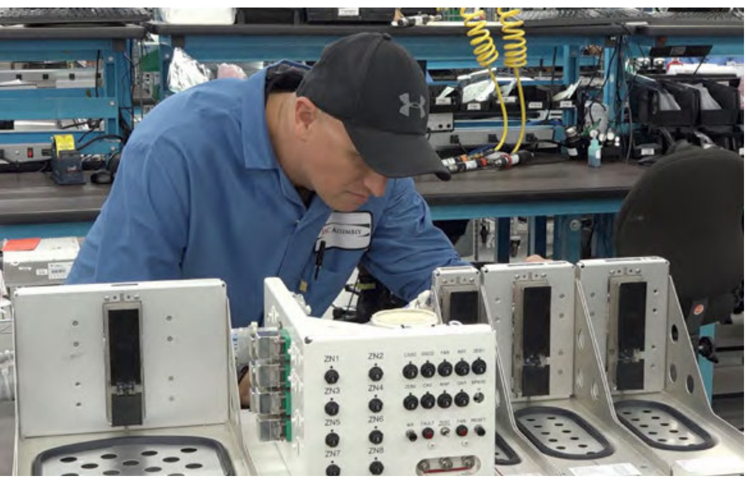


Figure 4: A worker assembles an aerospace electronics component.

2. All Machines are up and running effectively (output).

A typical CP plan will usually assume that all equipment is up and running and available to the operators who use it. Some models do allow for the input of additional queue times to allow for set-up which may include programming time and tooling adjustments. Unfortunately, this only masks legitimate process activities. Queue times are caused by either insufficient capacity to process one-piece flow or batching logic created by minimum order quantities. Queue times may be inevitable but should always be predictable and should not contain miscellaneous activities that should be more visible to the scheduling tool.

All equipment used in the manufacturing of a device or processing of a product should be identified early on and noted in the specifications of your internal process. Ownership should be identified as to the responsible parties that will ensure that the identified equipment has been reviewed, calibrated, cleaned, maintained and certified as "ready for use". Of course, there will always be unplanned, unexplained and occasional catastrophic types of failures that will cause a "line down" situation but these should be the exception and not the rule.

3. All labor standards have been reviewed and validated (input).

This process step should begin with the review or creation of labor standards for each assembly type or model that will be run through the shop floor environment. Who reviews the data isn't as important as the act of the review itself. Improper labor standards can skew the working model greatly and conceal available capacity or result in overcommitting existing hours.

Once the standards have been reviewed they need to be documented and stored in some manner that is either tied to a specific review date or revision for each appropriate assembly. With constant engineering change activity, it is easy to have a standard become obsolete quickly through the addition or deletion of certain process steps. For this reason, there should be an owner or panel of owners tasked with the ownership of those standards and their systematic review. This will help keep your CP model working correctly.

Where possible it may be a good idea to link the noted standard directly to the screen on your MRP model or imbedded into your work instructions. The intent being that it is accessible to the operator(s) who will be working with this product who can see what the standard is prior to performing the actual work. Keep in mind however that if you imbed the standard into the work instructions and you are using a paper system of work instructions you will have to purge and update that documentation every time you change the labor standard.

If your organization does not use standard cost accounting and lacks the labor routings, there are different approaches to validating the standards. At MC Assembly, we utilized an advance shop floor system called Fusion from Aegis where we use their traceability function to determine the exact time between operations or work centers and then compare those with the quoted assumptions. We then create a database with our quoted standards which allows us to measure our actual performance vs those standards.

4. All part numbers/model numbers are accurate.

The next step involved with creating your CP model is to ensure that the current part numbers and model numbers for the products for which you are creating standards are accurate. This review is best performed when doing the standard creation or review.

The reason that this step is so important becomes apparent when you are producing multiple models or variations of the same product. Most people discover that they have the same assembly being referred to as many different names in their system or by different operators. Customers will also bring their own variation to this process as well by creating part numbers for their products that may be similar to ones you have already chosen for other products.

Imagine how your CP model would work if the standard you had in your system was calling for twenty minutes for an assembly that took three hours. This is not as uncommon a discovery as you would imagine. There can often be a very large discrepancy between the estimated times created during a quote process and the actual time it takes to perform a task in reality once all the nuances of the process are known. It is critical that this feedback be collected so that your standards can be updated and reflected in your CP model accurately.

5. There are sufficient available resources to run equipment and planning tools, and complete tasks.

Once all the standards for your products have been identified and reviewed, machines are running smoothly and all material is available, you will want to check for some additional basics. These include the verification of adequate resources to staff equipment, complete all the identified tasks and to run all your planning tools.

Basically, this introduces a realistic finite constraint algorithm into the CP itself. Just like physical resources, time is never finite.

One commonly overlooked gap in planning for appropriate resources is tracking when your employees will be out on vacation, leave or are out sick. If you have two employees out sick for one day you've just lost sixteen available man hours that you were otherwise planning on. Therefore, it may be advisable to review your average employee time off and work some small buffer or percentage into your equation to ac-

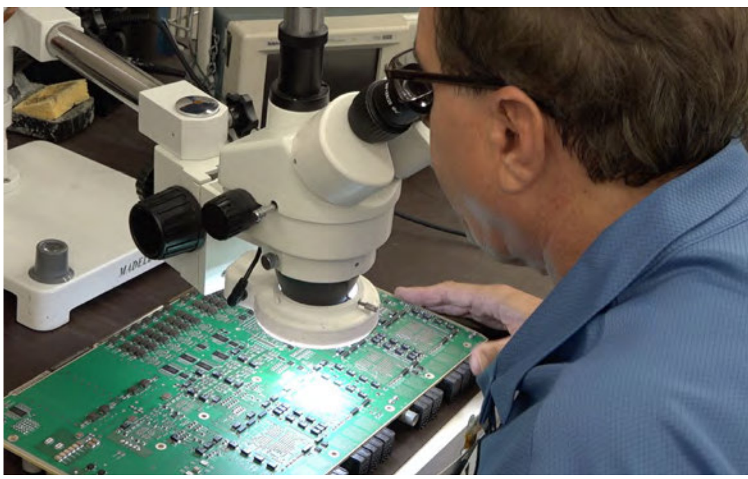


Figure 5: A test technician examines a printed circuit board under a microscope to ensure quality.

Figure 6: The inspection team auditing the standard work process to ensure SMT equipment is running to capacity.

count for anticipated or unanticipated time out by any of your staff. This is called the Load Factor used to recognize the loss due to utilization, efficiency, absenteeism, etc.

6. All appropriate work centers have been identified.

For any good CP tool to work properly you need to capture as many touch labor points as possible. The more finite the tool the more accurate it can be. In the EMS environment, most standard PCB process steps average approx. 12-15 work centers and with a standard Box Build or system integration area somewhat less at 8-10 work centers. For more complex high-level assembly (HLA) such as fluid, pneumatics, hydraulics, gears, motors and other moving parts then the average work centers may climb to 18-20.

Work centers should not be confused with process steps. Process steps may range in the hundreds if not higher. These would be the actual steps involved in putting the product together. Work Centers are the stops along the way that the product will go through to be processed. In a typical PCB assembly, these may include process steps like, Audit, Prep, SMT, Post-wave (Secondary Ops), Wave Solder, Test, QC, Package, etc. These steps will vary a little depending on the EMS provider. Each of the assemblies you are creating labor standards for should have a standard for each of those defined steps that it passes through (see Table 1).

In Table 1, we have an assembly that has 1.1 hours or 66 minutes' worth of applied labor estimated for each product. If we know our lot size was 100 units then it would be easy to esti-

Assembly P/N	Audit	Prep	Kitting	SMT	Reflow	Clean	Post-wave	Touch-Up	Wave	Clean	QC	Pack	Total
ABC123	0.02	0.09	0.45	0.04	0.02	0.02	0.33	0.01	0.02	0.02	0.1	0.03	1.1

Table 1.

mate that the total required labor would be 110 hours. Set-up, programming, etc., and balancing against available capacity is discussed in the next section.

In our example above it is not important whether you use actual minutes or tenths of an hour. It is important that whatever method you decide to go with that it is consistent and applied equally across all assemblies before the data goes into the system. All the operators using the system should also understand the "rules" as well before misinterpreting 1.1 for minutes vs. hours.

It is easy to see in the example above how much time can also be accumulating in what may be considered "non-key" process steps. If you were to only count the SMT time and post-wave time in the example and were only tracking this in your labor estimates, you would be missing 19 minutes' worth of labor required for every one of those 100 units. This would amount to 32 hours' worth of labor or roughly one man-week. That is also why it is important to identify and capture any work center that the product is likely to pass through.

Consideration should be given to the fact that many work centers have significantly lower cycle times than others, particularly the machine-driven work centers. Careful consideration needs to be given to the buildup of inventory queues around constraint operations and its working capital impact related to the lot sizes quoted. The notion to run a work center as much as and fast as you can create serious inventory issues. The goal is for product to flow and avoid the buildup of excess inventory queues in front of constraint work centers as much as you can. Focus your efforts in scheduling the constraint work center and base your production releases on the ability of these constraints to process parts further down the production flow. Products will not move any faster than the constraint work center therefore it does not matter how fast you run previous work centers, product will just sit waiting for the pacemaker.

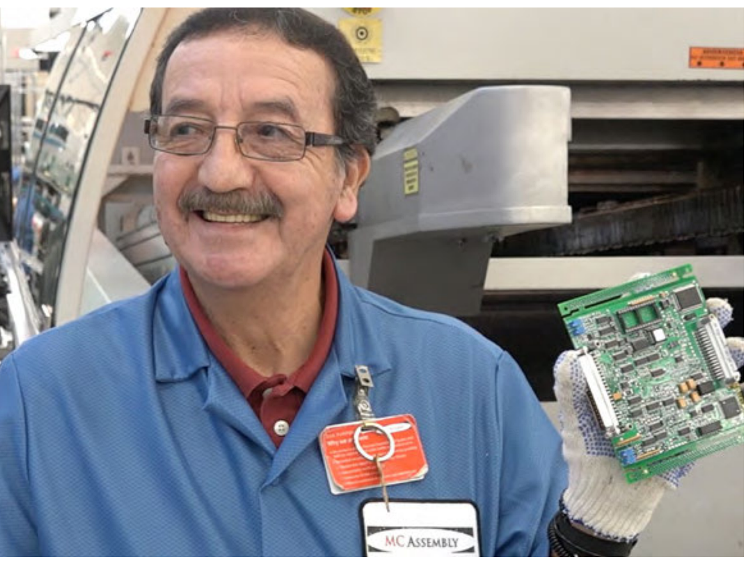


Figure 7: Here, we see an MC Assembly worker proudly displaying a freshly completed PCB board off mass solder operation.

7. All available resources are identified in each work center.

To complete the other half of your CP model, you will now need to identify the "available" resources in each work center. Depending on the type of model you are running, these will either be labor hours, machine hours or computer hours. (Other variables may apply.)

If you are estimating the available labor hours simply begin by taking a head count in each work center. First, note the "fixed" labor—the labor that does not float in and out of that work cell to work on other assignments. These should also be the resources that are available to apply labor to the product not supervisory headcount unless they are a "working" supervisor.

Once you have identified all the fixed or stable labor, estimate the net "heads" for those resources that move in an out of that work center. For instance, if you have two people that spend half of their day in that work center then you would add an incremental "1" for your available headcount. Total the two amounts, the fixed and variable resources. You will then need to discount this amount somewhere between 10-20% depending on your estimated time spent on set-up, programming, material transit time, tooling set-up, operator fatigue, break times, unplanned stoppage, sick time, vacation time, meeting times, clean up times, line set-up, etc.

This discount will vary depending on how you can overlap or utilize your time wisely.

Lines can be pre-set up prior to the operators arriving for their shift, 5S programs can be implemented to reduce hunting time looking for tools or breaking down materials prior to starting work. Break times can be overlapping, etc.

Now that you have your available labor hours identified for each work center and they have been properly discounted, then enter this time into your CP model. Whoever is in charge of updating this available labor will have to be conscious of the changing labor by week. Vacation and sick time for instance will fluctuate. Holidays will occur during certain weeks and there may be planned or unplanned shutdowns that will affect the stated available capacity. You may also be adding resources to a work cell or experiencing attrition. For these and many other numerous reasons the review of these available resources will have to be continually updated.

Machine hours are somewhat easier to estimate. You obviously do not have to concern yourself with sick time or vacation time. Machines (ideally) don't have fatigue throughout the day so long as maintenance has been kept up to date and they are manned properly you can anticipate the same available output from the machine throughout the day. All things being equal, if the machine is placing 10,000 parts per hour at 9:00 a.m., then it should be capable of placing 10,000 parts per hour at 2:00 p.m. as well. What you do have to consider is planned or unplanned preventative maintenance (PM) time, operator clean up and set-up.

Programming time and machine warm up periods after sitting idle. For the data in your model to be realistic you must note all the minutes or hours that the machines are available. If they are sitting in your factory at night and on the weekends and you choose not to run them or man those machines that is your choice. It doesn't reduce the available machine hours. Your model will simply reflect some incremental hours that are available and could be producing product.

This is opportunity cost and should be discussed in another article. When planning machine hours for your CP model also keep in mind that whether standing three operators in front of your machine or ten, the machine typically will not run any faster. Most machines

Figure 8: In the fast-paced EMS industry, MC Assembly workers strive to stay ahead of the curve.

have a fixed placement rate that may be augmented somewhat but not significantly through the addition of incremental operators. You may improve efficiency by reducing some stop and start times but that is all.

It should be noted in the high-mix, low-volume (HMLV) market, the ability to have a flexible work force is essential in meeting customer demands while controlling the labor costs. As such, we train our associates in multiple disciplines so they can be utilized at various points in our process as opposed to being single skilled. This means that in developing the CP model, you must incorporate the understanding that you have a certain amount of resource "float" that can be applied up and down the process line to meet the specific constraint. Although an over-simplified object of a CP model is to line balance, in the HMLV world, this is simply not economically possible. The human "resource" is probably the most difficult to apply in a CP model since a successful HMLV organization must have the flexibility to take into consideration specific skill sets over a broader resource range.

8. Queue times are identified. All wait periods, set-up, transfer times and transport times.

The one variable that is often overlooked when creating or working with a CP model are the queue times or "wait" periods. These include the times it takes to transfer product from one area to another, set-up times, non-automated data collection time, waiting for external sign-offs, essentially any time spent by direct labor that is not spent working directly applying value added activity to an open sales or work order.

At first glance, you may consider this to be insignificant but the accumulative effect of all this time can be substantial. By tracking this time or shedding light on all this kind of activity it also assists internal efforts to reduce these times and return more productive labor time to the shop floor to work on product. Set-up reduction activities, staging material and automating data collection and continuous flow models can all improve these situations.

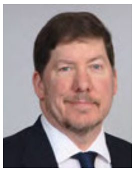
My suggestions for improving queue times would of course be to start by collecting all the time associated with these functions. Consider this as a baseline measurement that can be used as a jumping off or starting point. Track improvements in each of these areas over periodic intervals to highlight reductions. The inverse of this time saved should directly correlate to increased capacity.

9. Management support for implementing the tool is given and there is a champion for the project.

Most projects that have any hope of lasting and being implemented properly are those that have a specific champion or project manager as well as the support from senior management. With the proper support, the appropriate number of resources may get applied and the appropriate time allocated to the project to see it through to completion and full implementation.

A successful CP model should be part of the organization's sales and operations planning (S&OP) system. In this process, the executive leadership continuously review, plan and allocate the resources of all functions to meet a revenue and financial goal. Without a cohesive planning approach across all functional leaders of the organization, any isolated CP process will have only limited impact. The S&OP process is a topic by itself so we recommend you further investigate the topic and benchmark from companies successfully running an S&OP process. We will expand about S&OP in a later article. **SMT**

This article was written in collaboration with Richard Kelly, vice president of supply chain, and Luis Ramirez, COO, of MC Assembly.



David Prunier is the vice president of new business development at MC Assembly.

Red, Green, Yellow, Blue

The color of the light emitted by an LED can be tuned by altering the size of their semiconductor crystals. LMU researchers have found a clever and economical way of doing just that, which lends itself to industrial-scale production.

LMU researchers, in collaboration with colleagues at the University of Linz (Austria), have developed a method for the production of semi-conducting nanocrystals based on perovskite. These crystals are extremely stable, which ensures that the LEDs exhibit high color fidelity. Moreover, the resulting semiconductors can be printed on suitable surfaces, and are thus predestined for the manufacture of LEDs for use in displays.

The crucial element in the new method is a thin wafer, only a few nanometers thick, which is patterned like a waffle. The depressions serve as tiny reaction vessels, whose shape and volume ultimately determine the final size of the nanocrystals. Moreover, the wafers are produced by means of an economical electrochemical process, and can be fashioned directly into LEDs.

IPC's DAVID BERGMAN on Industry Training and Education

by Stephen Las Marias
I-CONNECT007

In a recent interview with *SMT Magazine,* David Bergman, vice president of standards and technology at IPC, explains how the organization helps elevate the industry through its training, continuous education, and standards development.

Stephen Las Marias: What are the big challenges you are looking at that really need to be tackled for overall industry growth?

David Bergman: The most critical issue we are facing is the recruitment and retention of employees. This stems from several other issues, specifically, a growing skill gap between the knowledge and skill that our current workforce possesses, and the knowledge and skills needed to compete in a global marketplace; rapidly evolving technology and the currently inefficient means of disseminating and swiftly training our workforce; lack of educational structures that support work and learn opportunities, stackable credentialing and education, and rapid retraining; and lack of transfer of retiring professional's knowledge base to young engineers.

Las Marias: What are the causes of these challenges?

Bergman: These challenges are created by a myriad of core issues in our industry. The single largest problem, however, is the lack of clearly defined career pathways, mechanisms for growth, and a structured training framework for the industry. Without clearly defined career paths, the industry will have trouble recruiting young talent that can easily decide on industries with "better" opportunities.

Without mechanisms for individuals to grow, the industry has trouble maintaining the talent they currently employ. No one wants to be working in the same job 10 years from now. This also ties back to the first point of a lack of career pathways. Finally, the lack of training and apprentice frameworks in the industry make it difficult to recruit and retain talent. This also impacts other parts of the industry also. The lack of this training infrastructure makes it difficult for companies to rapidly retrain employees for changing needs or the emergence of new technology.

Las Marias: Why is there a need for continuous training and education of the current workforce in the electronics assembly industry?

Bergman: Simply put, components are getting smaller, printed circuit board size is shrinking, electronic products are continually changing, manufacturing equipment is becoming more automated and requires technical repair skills, and worldwide manufacturing requires communication skills. Technologies change; needs change. Success in the electronics industry is largely determined by a company's ability to meet industry needs, but these needs are not static. The ability to rapidly and effectively retrain workers on new processes and methods, or new technologies, is a key factor in competition.

Las Marias: How would you describe the skills gap right now in the electronics manufacturing industry?

Bergman: The skills gap is a chronic problem in the electronics manufacturing sector. Most manufacturing companies have a hard time aligning the talent needed to run their businesses with the talent that is available to work locally. And as new innovations emerge, new skill requirements emerge as well.

As an association that represents thousands of member facilities across the global electronics industry supply chain, we decided to survey our U.S. members to gain insight into how the skills gap affects them. The results indicate that most of our member companies have trouble finding applicants with the necessary experience and technical skills.

Among production jobs, general assembler and hand solder experts are the most difficult to fill. On the professional side, quality control, process and entry-level electrical engineers have been hardest to find. Insufficient experience is the most common reason that applicants do not qualify for most positions. However, for many technical professional positions, the leading reason jobs went unfilled was that there were no applicants at all.

Respondents cite many essential skills that are in short supply, but the most common ones are soldering for production jobs, and engineers with industry experience, especially in process, test, and quality control. Two-thirds of our member companies reported they would expand their operations if they knew that finding qualified workers would be no problem. Thus, finding solutions to the skills gap is a high priority if America wants to expand its manufacturing sector.

In response to mounting concern about the shortage of U.S. workers with skills needed by electronics manufacturers, IPC conducted a fast-facts study this April to learn more about the skills gap as it affects U.S. electronics assembly manufacturers.

Las Marias: How is IPC helping the industry address this issue?

Bergman: Smart decisions, quality products, reliable performance are all critical to success in the highly-competitive, always evolving global electronics industry. To support these ever-changing demands, IPC delivers various methods of education, training, and certification. IPC training and certification programs are based on some of the most popular and critical IPC standards. IPC also develops media products for use in training employees in specific subject matter topics.

Launched last July, IPC EDGE delivers educational opportunities via online video training across the industry. IPC EDGE provides a 24/7 online training environment. The goal is to maximize training efficiency with minimal time away from the job or time spent in a traditional classroom.

The system is mobile friendly with on-demand courses ranging from IPC Essentials, an introductory course to the electronics industry, to a new electrostatic discharge (ESD) certification program launched in September 2016. More than 40 courses are currently available with more planned for release in 2017.

IPC EDGE curriculum will continue to evolve to meet the industry's growing demands. To further accomplish this, IPC has engaged member companies and training centers to develop new course topics. The result of this is a strengthened education portfolio to deliver the most efficient and effective training possible.

Through these educational programs, IPC aims to keep the electronics industry workforce on top of their game.

Las Marias: Please give a list of some of the programs of IPC that help elevate the skills of the operators, engineers, supervisors, etc., in the electronics assembly line.

Bergman: IPC training and certification plays a key role in bringing value to the electronics industry. These training and certification programs, built around IPC standards, developed and approved by industry, are delivered in a classroom setting by IPC certified trainers. Upon successful completion of the training and testing, the student is issued an industry traceable certification in one of the following IPC standards: J-STD-001, A-610, A-620, A-600, 7711/21, and 6012. Even though the training is conducted in the classroom, the certification testing is delivered through the online IPC certification portal. IPC also provides formal classroom training and certification programs for Certified IPC Designers.

For more than 30 years, IPC has been producing industry-approved, commercial-free training videos, covering electronics assembly acceptance standards, hand soldering, lead free, repair and rework, ESD control, component ID, counterfeit components, cable/wire harness assemblies and printed board fabrication. Now available in IPC EDGE, IPC's comprehensive collection provides companies with another method of training and education to enhance the skills of employees.

Las Marias: What are the advantages of these programs?

Bergman: The benefits are clear. Investing in IPC training and certification programs can help participants demonstrate to current and potential customers that their company considers rigorous quality control practices very important; meet the requirements of OEMs and electronics manufacturing companies that expect their suppliers to have these important credentials; gain valuable industry recognition for their company and themselves; and facilitate quality assurance initiatives that have become important in international trading.

And with IPC EDGE, from entry level personnel to executives, users are provided with knowledge that support learning goals that can be applied directly to their work. This includes preparation for CIS (Certified IPC Specialist) certification, the most recognized certification from IPC in the electronics industry. Users receive up-to-date information on compliance and regulatory issues, as well as highlights on the latest revisions and updates to IPC's most popular standards.

From skills development, operator training, and technical knowledge to certification and professional development, IPC EDGE covers all the pertinent areas needed to excel in the electronics industry. Topics covered include electrostatic discharge (ESD), control for electronics assembly, introduction to hand soldering, FOD prevention in electronics assembly, surface mount solder joint quality standards, counterfeit components, and component identification, among many others.

Each year, IPC hosts and participates in industry related events. Ranging from small to large, IPC hosts more than 100 events across the globe each year, drawing in thousands of participants. These events included technical education both online and in the classroom, government relations conferences, webinars, workshops, and regional hand soldering competitions.

Las Marias: Are you seeing increasing demand for these activities from the industry?

Bergman: Yes, we are continuing to see increases in global demand for training and certification. Some of our focus has been on operator-level courses with the ability to deliver online training in various languages. We are also looking at how to support engineers, managers, and designers beyond our existing education events by adding more online courses and working with our members to identify specific areas IPC can support the industry.

Las Marias: What activities is IPC doing to ensure that the new workforce entering the industry have the proper skill sets?

Bergman: As part of its government relations program, IPC advocates for ambitious public policies to address the skills gap. For example, IPC supports the bipartisan Strengthening Career and Technical Education for the 21st Century Act, H.R. 2353, which is making its way through Congress and would provide federal support for career education programs. We are also engaged in an ongoing dialogue with the Trump administration to explore how we can support their apprenticeship and workforce development initiatives.

The annual observance of Manufacturing Day (MFG DAY), which takes place this year on October 6, offers a special opportunity to engage your local community on attracting the next generation of workers to the industry. Supported by a group of industry sponsors including IPC, MFG DAY encourages companies to open their doors to show the public what manufacturing really is. Last year, more than 400,000 people attended 1,700 events across the country, and we are looking to make a bigger impact this year.

In addition, IPC supports the EU Skills Agenda which seeks to improve the quality of European labor market. IPC stands ready to work with the European Commission, the member states and stakeholders to tackle our common challenges including the lack of relevant skills to match labor market needs, insufficient comparability of skills and qualifications, and the difficulty to anticipate skills that would be needed in the future. Addressing the current skills gaps will have a multiplying effect—translating into more innovation, more growth, more competitiveness and more high-quality jobs in the EU.

Attracting and retaining a skilled workforce has become an increasingly important factor of competitiveness in a globalized market place. Recruiting the necessary talent is a fundamental concern for the advanced manufacturing industry in Europe, which consists of more than 700,000 enterprises and employs more than 13 million people. With 35 training centers across Europe that improve the skills of approximately 14,000 employees per year in the EU, as well as online training possibilities, IPC is a credible and reliable source for electronics education for the electronics industry.

Las Marias: Do you have any final comments?

Bergman: IPC is dedicated to addressing the core issues of recruiting, retention, and retraining. Through IPC EDGE, and some of the new initiatives we have in the pipeline, we are hoping to provide the electronics industry with mechanisms and infrastructure needed to address some of the critical issues. IPC will be at the forefront of the evolving needs of the electronics industry, and lead the effort to address the growing skills gap and a lack of career pathways and education frameworks. While this road is not short or easily traversed, we are dedicated to driving forward.

Las Marias: Thank you very much.

Bergman: Thank you. **SMT**

MEIKO

Leading PCB Manufacturer Seeks Account Manager

Meiko Electronics, a global leader in PCB interconnect solutions for Tier I and II electronics companies, has expanded its global manufacturing footprint to include two campuses in China and two in Vietnam.

We are looking for a full-time account manager to introduce the company and our outstanding capabilities to new customers, primarily in the automotive space.

Key Responsibilities:

- Work directly with PCB sourcing teams to generate interest in our company
- Manage all customer relations, including scheduling onsite customer meetings with sourcing team decision makers, factory audit and qualification visits resulting in AVL status attainment
- Manage quality/engineering/logistics issues pertaining to key accounts

Qualifications:

- 3 years' professional experience in PCB sales or similar electrical component experience
- Excellent communication and relationship building skills
- Organizational skills, with a strong attention to detail
- Knowledge of Japanese or Mandarin languages a plus

Location:

The ideal candidate will have some initial prospective customers located nearby in the Midwest region and the ability to travel as needed to our Asia-based manufacturing locations.

Competitive compensation and benefits package, including competitive base salary, generous bonus/commission plan, medical/dental/vision and life insurance, matching 401k, PTO.

apply now

American Standard Circuits

Creative Innovations In Flex, Digital & Microwave Circuits

CAM Operator

American Standard Circuits is seeking a candidate to join its team in the position of CAM operator. Applicants will need experience in using Valor/Genesis (GenFlex) CAD/CAM software with printed circuit board process knowledge to edit electronic data in support of customer and production needs. Other requirements include:

- 5+ years of experience in PCB manufacturing
- Process DRC/DFMs and distinguish valid design and manufacturing concerns
- Modify customer supplied data files and interface with customers and engineers
- Release manufacturing tooling to the production floor
- Prepare NC tooling for machine drilling, routing, imaging, soldermask, silkscreen
- Netlist test, optical inspection
- Work with production on needed changes
- Suggest continual improvements for engineering and processing
- Read, write and communicate in English
- Understand prints' specifications
- Must be U.S. citizen or permanent resident (ITAR)
- High school graduate or equivalent

apply now

Altium

Application Engineer

The application engineer is the first contact for our customers who have technical questions or issues with our product. We value our customers and wish to provide them with highest quality of technical support.

Key Responsibilities:

- Support customer base through a variety of mediums
- Log, troubleshoot, and provide overall escalation management and technical solutions
- Create various types of topic based content, such as online help, online user guides, video tutorials, knowledge base articles, quick start guides and more
- Distill complex technical information into actionable knowledge that users can understand and apply
- Continually develop and maintain product knowledge

Requirements:

- Understanding of EDA electronic design software, schematic capture and PCB layout software
- Bachelor's degree in electronics engineering or equivalent experience
- Sales engineering and/or support engineering experience
- Circuit simulation and/or signal integrity experience
- Understanding of ECAD/ MCAD market segments
- Understanding of micro controllers, SoC architecture and embedded systems market
- Database experience preferred (i.e., MySQL, PostgreSQL, Microsoft Access, SQL, Server, FileMaker, Oracle, Sybase, dBASE, Clipper, FoxPro) etc.
- Experience with PLM/PDM/MRP/ERP software (Program Lifecycle Management) preferred
- Salesforce experience a plus

Salary based upon experience. Comprehensive benefits package and 401k plan. Openings in USA, UK, and Germany.

For more information, contact Altium.

apply now

esi®

Designed for Brilliance. Engineered for Production.

Embedded Engineer—

Portland Oregon

ESI, a pioneer and leading supplier of world-class production laser systems that help microtechnology customers achieve compelling yield and productivity gains, is looking for an embedded engineer.

As a software engineer, you are designing and delivering the embedded software that drives ESI's leading-edge manufacturing systems. The successful candidate will join a multi-disciplinary team focused on developing cutting edge technology in a fast-paced and technically challenging environment. Primary responsibilities will include embedded real-time system development, low-level machine control, system-level troubleshooting, and some supporting application level development.

Desired experience includes:

- Highly proficient in C/C++ programming
- Proficient in working with and programming DSPs or microcontrollers
- Experience designing software for embedded systems with constrained resources
- Knowledge of different embedded runtime environments (Linux, bare metal, RTOS)
- International travel to support ESI system installations (<10%)
- Engineering degree with to 5–7 years of related experience, or equivalent combination of education and experience
- Fundamental engineering knowledge (basic physics, calculus, problem solving)

Interested? Please apply below.

apply now

MacDermid
PERFORMANCE SOLUTIONS

Do you have what it takes?

MacDermid Performance Solutions, a Platform Specialty Products Company, and daughter companies manufacture a broad range of specialty chemicals and materials which are used in multi-step technological processes that enhance the products people use every day. Our innovative materials and processes are creating more opportunities and efficiencies for companies across key industries – including electronics, graphic arts, metal & plastic plating, and offshore oil production. Driving sustainable success for companies around the world, and at every step of the supply chain, takes talent. Strategic thinking. Collaboration. Execution.

The people of MacDermid Performance Solutions stand united by a guiding principle: That if it doesn't add value, don't do it. This belief inspires a unique culture where each team member has opportunities to imagine, create, hone and optimize. Do you have what it takes? Join our growing team of over 4,000 professionals across more than 50 countries with openings in research, finance, customer service, production and more.

MacDermid Performance Solutions and its affiliates are Equal Opportunity/Affirmative Action Employers.

apply now

eptac
TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

We are growing! EPTAC, a leading provider in the electronics training industry is looking for some great people to join our team. If you love teaching, choosing the classes and times you want to work, and being your own boss, this may be the career for you. We are looking for instructors who have a passion for working with people to develop skills and knowledge. If you have a background in electronics manufacturing and an enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Opportunities available across U.S. and Canada, especially in our growing markets of California, Florida and New England. Some travel involved. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

apply now

MivaTek Global

Application/Sales Engineers

Positions available in the Eastern, Midwest and Western United States. Positions will focus on supporting sales and applications development for Miva Technologies' DLP direct imaging system within the PCB and micro-electronics markets. Experience with photoresist and imaging preferred, but not required.

Service Technicians

Positions available for Eastern and Western United States. Service technicians will support our rapidly expanding installed base of Miva Technologie's DLP imaging systems and other systems sold by the company.

Send resume and contact information for both jobs to Brendan Hogan.

apply now

Outside Sales/ Key Account Managers

NCAB Group USA is adding to our existing outside sales team in various U.S. locations:

- Ontario, California
- Itasca, Illinois
- Irving, Texas
- Vancouver, Washington

This is a sales position that requires the ability to convert those cold calls into high-value customer meetings. What we are looking for:

- A "hunter" mentality
- The ability to create solid customer relationships
- A desire to excel and not settle for mediocrity
- 5+ years of experience in the PCB or semiconductor industry
- An excellent ability to present a product and do the "deep dive" during customer visits by asking open ended questions and identifying customer pain points
- The energy to move from prospecting to cold calls to getting the win
- Knowledge of "SPIN" selling
- A college degree
- Willingness to travel, domestically and globally
- U.S. citizens with a valid U.S. passport

Interested? Send your resume.

apply now

Visit us at www.NCABGroup.com

PCB Process Planner

Accurate Circuit Engineering (ACE) is an ISO 9001:2000 certified manufacturer of high-quality PCB prototypes and low-volume production for companies who demand the highest quality in the shortest time possible. ACE is seeking a skilled individual to join our team as a PCB process planner.

Responsibilities will include:

- Planning job travelers based on job release, customer purchasing order, drawings and data files and file upon completion
- Contacting customer for any discrepancies found in data during planning and CAM stage
- Consulting with director of engineering regarding technical difficulties raised by particular jobs
- Informing production manager of special material requirements and quick-turn scheduling
- Generating job material requirement slip and verify with shear clerk materials availability
- Maintaining and updating customer revisions of specifications, drawings, etc.
- Acting as point of contact for customer technical inquiries

Candidate should have knowledge of PCB specifications and fabrication techniques. They should also possess good communication and interpersonal skills for interfacing with customers. Math and technical skills are a must as well as the ability to use office equipment including computers, printers, scanners, etc.

This position requires 3 years of experience in PCB planning and a high school level or higher education.

apply now

TECHNICA, U.S.A.
Fulfilling Manufacturing Needs
Throughout the Electronics Industry

Southern California Territory Sales Engineer

Technica, USA, a Western regional manufacturer's representative/distributor, has an open sales position for our Southern California territory. The position will be responsible for selling and servicing our entire product line within the specified territory to the PCB manufacturing industry.

This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Required Skills:

- BA/BS degree-desired, in a technical area is preferred
- Two years of outside/inside sales or manufacturing experience in the PCB manufacturing environment is desired
- Self-motivated self-starter with the ability to initiate and drive business with little supervision
- Independent worker with a strong commitment to customer satisfaction
- Understanding of consumable sales process
- Ability to organize activities and handle multiple projects simultaneously with effective and timely follow-up
- Ability to solve problems and make decisions for which there are no precedents or guidelines and be resourceful in nature
- Positive attitude while operating under pressure and be an independent problem-solver
- Computer skills in Windows, Outlook, Excel, Word and PowerPoint
- Must have a valid driver's license with good driving record

Please send resume.

apply now

TECHNICA, U.S.A.
Fulfilling Manufacturing Needs
Throughout the Electronics Industry

Western Regional Equipment Service Technician

Technica, USA, a Western regional manufacturer's representative/distributor has an opening for an equipment service technician covering the Western USA, including but not limited to, California, Oregon, Washington, Utah, Colorado, and Arizona. The position will be responsible for servicing our PCB fabrication equipment product line, including installation, troubleshooting, repair service, rebuild service, etc. This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Key responsibilities are to install and service equipment, conduct equipment audit, and provide technical service when appropriate to solve problems.

Required Skills:

- 2+ years of experience in a PCB manufacturing environment or similar
- Willing to travel
- Positive "whatever it takes" attitude while operating under pressure
- Self-motivated self-starter with the ability to initiate action plans
- Ability to work independently with a strong commitment to customer satisfaction
- Excellent communication and interpersonal skills
- Strong ability to use all resources available to find solutions
- Computer skills with ability to write detailed service and equipment reports in Word
- Understanding of electrical schematics
- Able to work in and around equipment, chemical, and environmental conditions within a PCB manufacturing facility

Please send resume.

apply now

BLACKFOX

Premier Training & Certification

IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

apply now

CHEMCUT

BOUNDLESS INNOVATION | UNBEATABLE PRECISION

Field Service Technician

Chemcut is looking for a field service technician who is willing to travel worldwide. Previous experience with industrial machine controls (including PLC systems), mechanical components such as conveyors and pumps, plastic piping and fabrication are desirable.

To learn more about Chemcut and apply for this position, please apply to Mike Burke below, or call 814-272-2800.

apply now

Prototron Circuits

Experienced PCB Sales Professional

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. Prototron of Redmond, Washington, and Tucson, Arizona are looking for an experienced sales professional to handle their upper Midwest Region. This is a direct position replacing the current salesperson who is retiring after spending ten years with the company establishing this territory.

The right person will be responsible for all sales efforts in this territory including prospecting, lead generation, acquiring new customers, retention, and growth of current customers.

This is an excellent opportunity for the right candidate. Very competitive compensation and benefits package available.

For more information, please contact Russ Adams at 425-823-7000, or email your resume .

apply now

Process Engineer (Redmond, Washington)

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. We are looking for an experienced PCB process engineer to join the team in our Redmond, Washington facility. Our current customer base is made up of forward-thinking companies that are making products that will change the world, and we need the right person to help us make a difference and bring these products to life. If you are passionate about technology and the future and believe you have the skills to fulfill this position, please contact Kirk Williams at 425-823-7000 or email your resume.

apply now

ARLON

Arlon EMD, located in Rancho Cucamonga, California is currently interviewing candidates for **manufacturing** and **management positions.** All interested candidates should contact Arlon's HR department at 909-987-9533 or fax resumes to 866-812-5847.

Arlon is a major manufacturer of specialty high performance laminate and prepreg materials for use in a wide variety of PCB (printed circuit board) applications. Arlon specializes in thermoset resin technology including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, high density interconnect (HDI) and microvia PCBs (i.e., in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2008 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customer's requirements.

more details

LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®
311 Turquoise Street Milpitas, CA 95035 (Phone) 408-945-8787

SALES ACCOUNT MANAGER

This is a direct sales position responsible for creating and growing a base of customers. The account manager is in charge of finding and qualifying customers while promoting Lenthor's capabilities to the customer through telephone calls, customer visits and use of electronic communications. Experience with military and medical PWB/PWA a definite plus. Each account manager is responsible for meeting a dollar level of sales per month and is compensated with salary and a sales commission plan.

Duties include:

- Marketing research to identify target customers
- Initial customer contact (cold calling)
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Quantity and delivery requirements
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Bonding
- Submitting quotes and sales orders
- Providing ongoing service to the customer
- Problem solving
- Developing customer information profiles
- Developing long-term customer strategies to increase business
- Participate in quality/production meetings
- Assist in customer quality surveys
- Knowledgeably respond to non-routine or critical conditions and situations

Competitive salaries based on experience, comprehensive health benefits package and 401(k) Plan.

apply now

Recent Highlights from SMT007

1 IPC Committee Selects Communication Transport Protocol for Connected Factory Initiative

The IPC 2-17 Subcommittee has voted to use the Advanced Message Queuing Protocol (AMQP) as the transport protocol for machine to machine communication as part of the Connected Factory Initiative (CFX).

2 How Much of My Electronics Manufacturing Should I Outsource?

Once you have decided to outsource to an EMS partner, you need to think about how much of your existing operation you plan to relinquish.

3 IPC Invites Members to Join European Standards Steering Committee

As the development of IPC standards in Europe continues to grow, IPC is reaching out to the European electronics industry and IPC members to join the IPC European Standards Steering Committee.

4 4 Ways Your EMS Partner Can Respond to Supply Chain Disruption

Electronic component supply chain disruptions are painful. Lead-times can extend overnight, prices can treble, and in some cases, parts are placed on allocation or discontinued altogether.

5 Foxconn and Rockwell Automation Collaborating on Smart Manufacturing

Foxconn and Rockwell Automation are collaborating to implement Connected Enterprise and Industrial Internet of Things (IIoT) concepts for smart manufacturing in Foxconn's new U.S. facilities.

6 Valtronic Welcomes New R&D Engineering Director

Valtronic Technologies (USA) has hired Mike Labbe to the newly created position of Director R&D Engineering.

7 Celestica Releases 2016 Sustainability Report

Celestica Inc.'s 2016 Sustainability Report highlights the company's sustainability strategy and key activities and milestones for each of its focus areas including employee sustainability, environmental sustainability, material stewardship, sustainable solutions and sustainable communities.

8 STI Acquires Fischerscope X-ray XDAL 237

STI Electronics Inc. has acquired a new Fischerscope X-ray XDAL 237 energy dispersive X-ray fluorescence (EDXRF) system.

9 iNEMI's Bill Bader to Keynote Technical Innovations Symposium at SMTA International

Bill Bader, CEO of iNEMI, will keynote the Technical Innovations Symposium at SMTA International 2017.

10 Saline Lectronics Promotes Jeff Riedel to Executive Vice President

Saline Lectronics Inc. has promoted Jeff Riedel to the position of Executive Vice President of Manufacturing and Continuous Improvements.

Events

For IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing, check out SMT Magazine's full events calendar here.

24th FED Conference
September 15–16, 2017
Bonn, Germany

SMTA International 2017 Conference and Exhibition
September 17–21, 2017
Rosemont, Illinois, USA

electronicAsia
October 13–16, 2017
Hong Kong

TPCA Show 2017
October 25–27, 2017
Taipei, Taiwan

productronica 2017
November 14–17, 2017
Munich, Germany

HKPCA/IPC International Printed Circuit & South China Fair
December 6–8, 2017
Shenzhen, China

47th NEPCON JAPAN
January 17–19, 2018
Tokyo Big Sight, Japan

DesignCon 2017
January 30–February 1, 2018
Santa Clara, California, USA

IPC APEX EXPO 2018 Conference and Exhibition
February 27–March 1, 2018
San Diego, California, USA

Medical Electronics Symposium 2018
May 16–18, 2018
Dallas, Texas, USA

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:
MANAGING EDITOR: **STEPHEN LAS MARIAS**
+63 906 479 5392; stephen@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:
PRODUCTION MANAGER: **SHELLY STEIN** shelly@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA , TOBEY MARSICOVETERE**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER: **SHELLY STEIN**

COVER IMAGE: **© VITEC40, ADOBE STOCK**

SMT® (Surface Mount Technology) is published by BR Publishing, Inc., PO Box 50, Seaside, OR 97138

September 2017, Volume 32, Number 9 • SMT© (Surface Mount Technology©) is published monthly, by BR Publishing, Inc.

ADVERTISER INDEX

Coming Soon to *SMT Magazine:*

OCTOBER:
Solder Joints
Critical factors, parameters, and strategies for achieving the perfect solder joint.

NOVEMBER:
HDI
Challenges and strategies in dealing with HDI boards.