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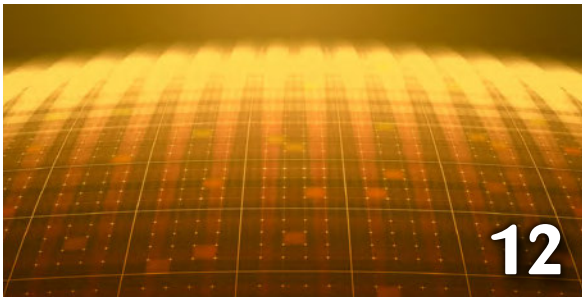

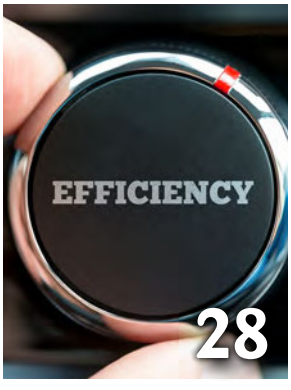

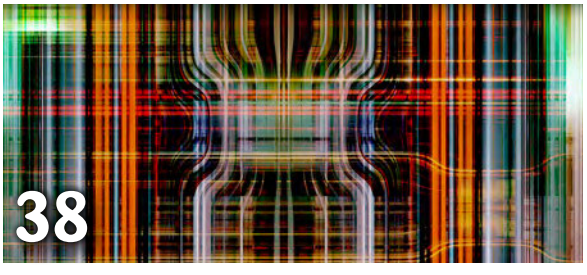

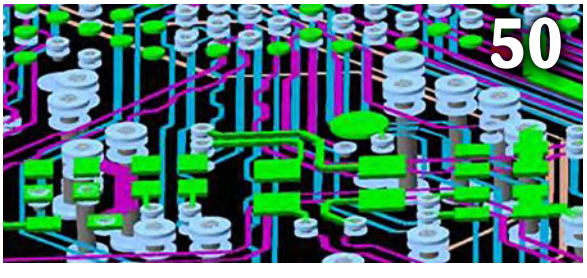

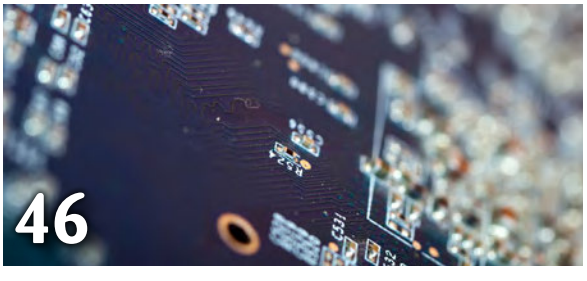

High-Density Design

Each year, more and more PCB designers are designing boards that feature HDI technology. And no wonder: HDI can lead to substantial reductions in cost by lowering the board's layer count. But as OEMs continue to squeeze more functionality into tiny handheld devices, there are still a lot of questions swirling around HDI design.

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Is HDI Making a Comeback in the U.S.?

by Andy Shaughnessy
I-CONNECT007

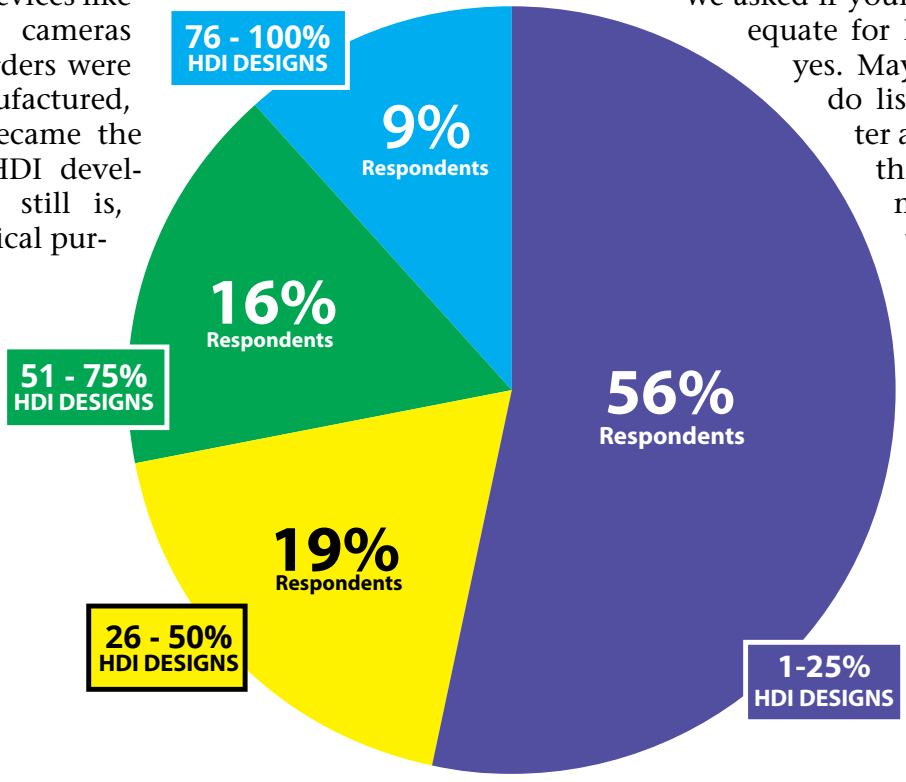
When I first started covering this industry 19 years ago, I kept hearing about this thing called HDI that was about to take off. I'd go to trade shows and hear, "You watch…next year, or maybe the year after, most PCBs are going to be HDI. It's inevitable. You watch."

There were roadmaps, white papers, and articles advocating HDI. Happy Holden and Mike Fitts taught a class on HDI design, and the room was usually packed with designers hungry for information about this new technology.

Everyone was hot for HDI, and soon it really did take off…in Asia. Like a few other technologies, HDI was born here, but mastered by companies in Asia. That's where the handheld devices like cellphones, cameras and camcorders were being manufactured, and Asia became the center of HDI development. It still is, for all practical purposes.

But HDI has come full circle, as we found when we surveyed readers for this issue. A lot of you are spending at least some of your time designing HDI boards. As you can see in Question 1, less than 3% of respondents said they never deal with HDI boards. Over half of respondents said HDI makes up only 1-25% of their work, and for almost 10%, HDI is a regular part of their job.

Designers used to tell me, "HDI design won't really be possible until the EDA companies get on board and give us more functionality so we can stop doing workarounds." Well, the survey results in Question 2 indicate that the EDA companies have heard your pleas. When we asked if your EDA tools were adequate for HDI, over 77% said yes. Maybe EDA companies do listen to designers after all, or they just knew they could charge more for software that can do HDI. Either way, it's a good



Q1: What percent of your designs are HDI?

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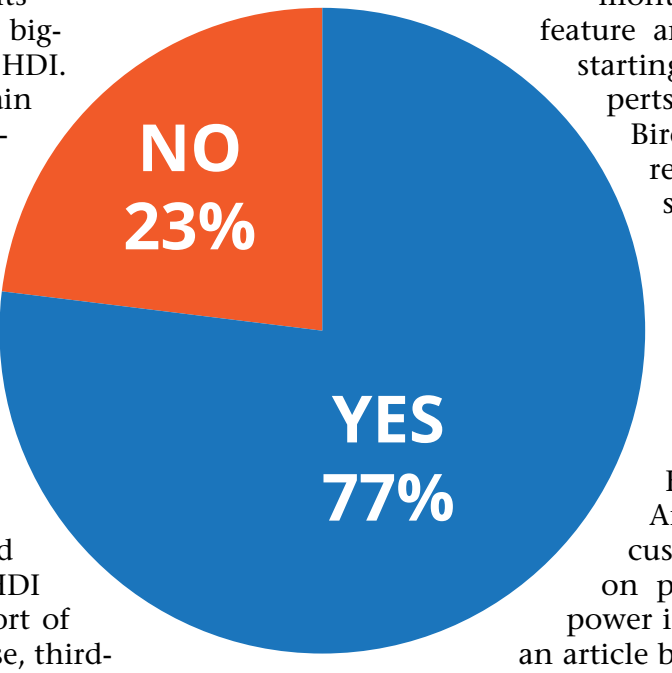
thing that you all have the right tools for the job.

Quite a few respondents listed cost as one of their biggest challenges regarding HDI. Since one of HDI's main benefits is lower overall cost, there may be a disconnect somewhere along the line. I've heard horror stories of companies using HDI when it's not necessary, and that's a recipe for disaster.

Almost every respondent said they use FR-4 or a variation of FR-4 for HDI build-up. And almost everyone doing HDI said they receive some sort of training, whether in-house, third-party events, or conferences. Many have also read books such as Happy's HDI Handbook, and a few said they relied on their fabricators' knowledge of HDI processes.

HDI is making a comeback in the States, with more and more fabricators here offering HDI services. Can the U.S. ever become the HDI center of the world?

Q2: Are today's EDA tools adequate for HDI?



If so, we'd like to help make that happen! This month, we have a raft of feature articles on HDI design, starting with a rousing experts' discussion with Steve Bird of Finisar, Tony Torres of APCT, and MC Assembly's Steve Jervey, Mike Smyth and Paul Petty. Then, San Diego PCB founder Mike Creeden shares his views on what it takes to design and manufacture a cutting-edge HDI board today. Craig Armenti of Mentor discusses the impact of HDI on power distribution and power integrity. Then we have an article by NCAB COO Jim Nuttall, who explains the state of HDI as he sees it, and the smart decisions that have to be made, from the design stage through volume production.

We also have an article by Bruce Wu of EDADOC, the largest design bureau in China, on the HDI trends he's seeing in the domestic China market, as well as around the globe. We round things out with Vern Solberg, who has a great column on design strategies specifically for HDI boards. As usual, we also have columns by our regular contributors Barry Olney, Tim Haag, and Jade Bridges.

I'm getting ready to head off to productronica, in Munich. I hope to see some of you there, but if you can't make it across the pond, don't worry. We'll have plenty of coverage of this giant show on our sites and in our newsletters in the coming days and weeks.

See you next month! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine*. He has been covering PCB design for 18 years. He can be reached by clicking here.

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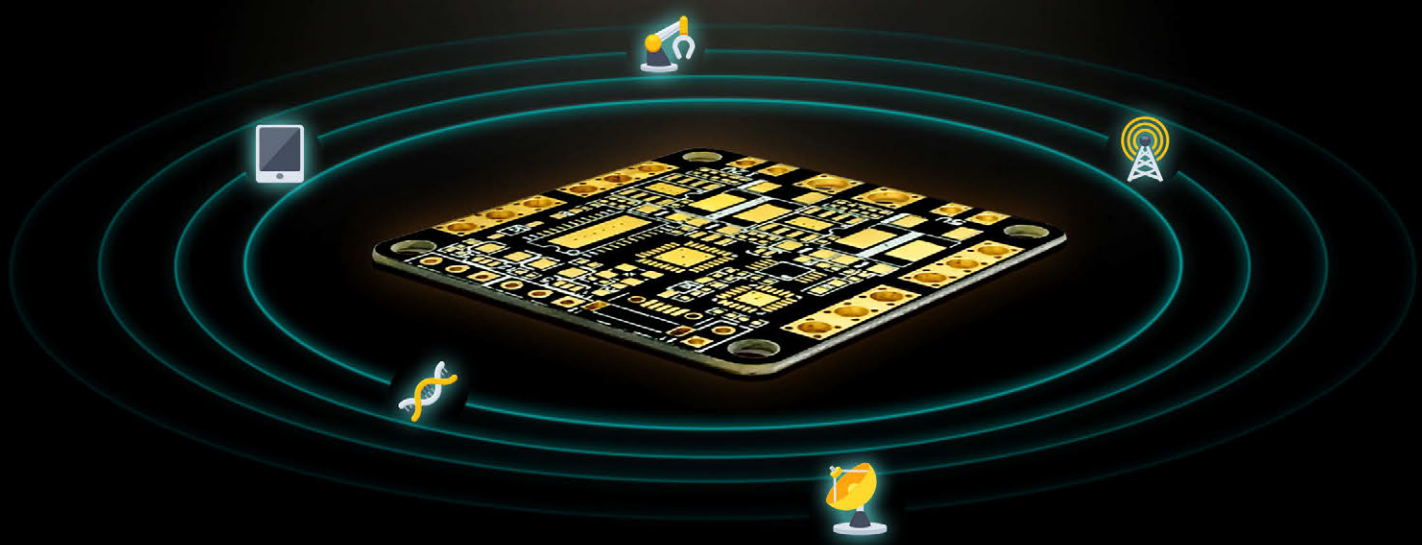

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by the I-Connect007 Team

For this month's issue, our editorial team interviewed some of the top HDI experts in the PCB supply chain. Joining us on the conference call were Steve Bird, PCB/flex technology manager at Finisar, and Tony Torres of APCT. Also on the call were several technologists from MC Assembly: Vince Burns, quality engineer; Steve Jervey, director of Test Engineering; Mike Smyth, SMT engineer; and Paul Petty, product engineer. This wide-ranging conversation covered the latest technology developments, manufacturing challenges, and HDI strategies, from the design, fabrication, and assembly perspectives.

Andy Shaughnessy: Why don't we start with design? Steve, you're an HDI technology manager, so you're driving this whole thing. Why don't you tell us where you guys are with HDI?

Steve Bird: Sure. I'm wearing two hats. One is technical lead for the EEs and the CAD designers here at Finisar, and the second one is organic substrate roadmapping and development. Maybe 18 months or two years ago, we were working with a fabricator. We started cheating on the FR-4 design rules, and to their credit they built over 1,500 of these over a period of a year or so and finally gave it up and said, "No bid." So of course, the upper management team came to my group saying, "You're violating the design rules." And I said, "Yes, but not without an engineer sitting next to the CAD designer. And yeah, we did, but what we have here really is not a design rule violation, but a technology limitation."

That spun off an effort to find a substrate that could support the design rules that we're cheating to. Our PCB technology team was tasked with the effort. We got one new substrate developed and released, but now those new design rules are being violated; we have to continue development. For that previous generation, once we got off FR-4 and onto alternate materials, we were still in the subtractive process. Now we're looking very heavily at the semi-additive process. Our trace with normal FR-4 is going from 4 mil trace and space down to say, 3.5 mil,

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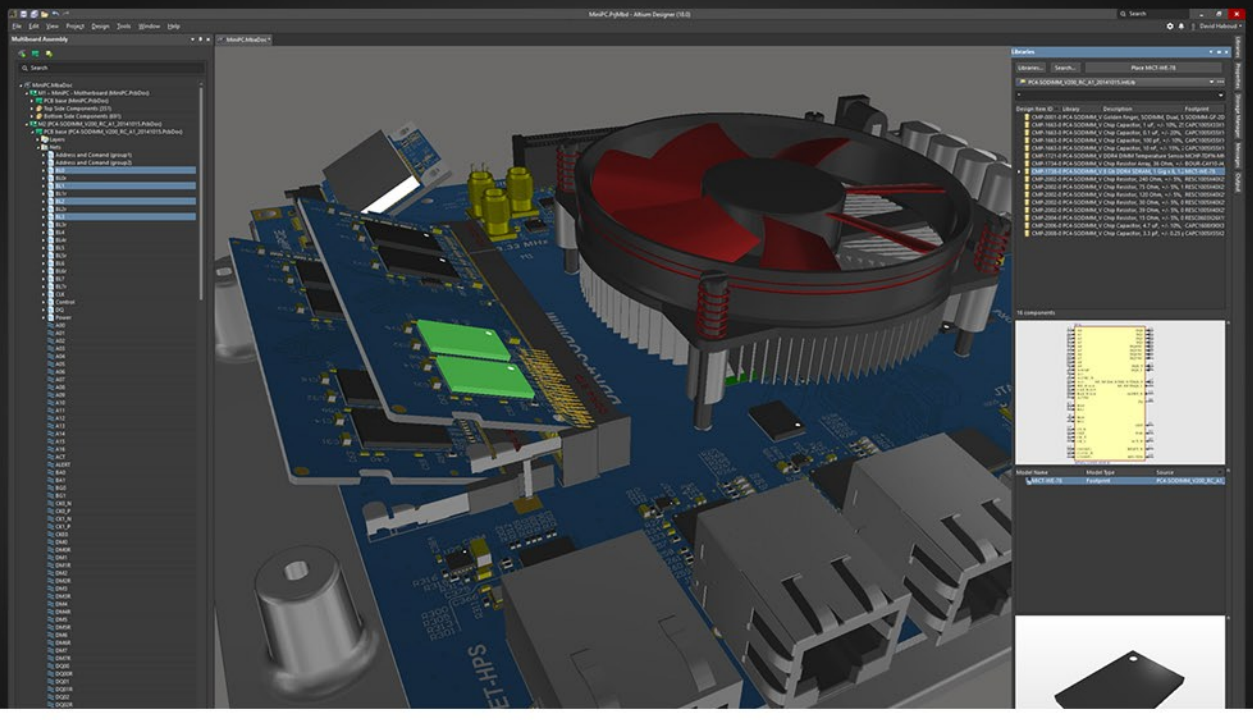

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roughly, and that's what earned us the no-bid. Now we're at two mil trace and three mil space, and that's still not good enough.

So, we're continuing to increase the density, and for us, our whole game is no vias, no stubs, and no parasitics. Everything's predictable: no glass weave, etc. So what we're looking at is thinner and thinner laminate, and hybrid stack-ups. We can certainly do all our power delivery and control signal distribution on FR-4 layers, but what lies on that surface is important to us. We can do small modules, system-type modules for our ICs and such, our chip-on-board and so on, but really what we need is a full system-level surface layer that can support those types of densities and mount chips.

Steve Bird

That's really what we are working towards right now. We're now looking at 20–25-micron traces and 25–40-micron gaps, and seeing if we can't do that. If we can, then we can support all our chip mounting technologies. We can support our system-level traces that get from the origin to the destination and so on. When we do that, then of course these traces get very lossy, and that becomes a huge concern. So our antidote to that is keep them short. Get them shorter. And so that's kind of our roadmap in a nutshell. We're starting with surface density, because the propagation is the fastest, keeping it stubless, and then making the net as short as possible. We run everything that's important differentially for noise immunity. So, you can imagine the types of stackups we're looking at in terms of hybrid stack-ups and so on.

Shaughnessy: What sort of materials are working out best for you?

Bird: When we first started this effort, my boss asked me, "What would you use? What's the first step that you would do?" My response was, "Thin, glass-free laminates. Something that's just as thin as you can make it." Let me put it this way: There is a slide that shows FR-4 with traces and spaces in the 4 mil range. With the help of HDI, we then took the through-hole off the surface and stacked the blind and buried vias. We call this technology level modified FR-4. This got us to 3.5 mil trace/space. There is another slide called the constant impedance funnel for differential pairs. You can imagine this funnel that starts out in the FR-4 at 4 mil trace/space and goes all the way down to be something like chip-on-glass or ceramic at 0.6 mil trace/space. One can place a large bracket in the gap with a label saying "This gap is too large. This gap is responsible for chewing up real estate because things are not scalable." The things that you do on an IC or on glass, you have a lot of overhead in terms of the splay angle, trying to get the signals out (escaped) and getting them routable.

We are trying to solve that. Because once you solve the trace to be similar to the pin or pad pitch, then your channels become much more scalable on the surface. By the way, as we're going up in frequency, we're also going up in channel count. We're getting whacked from both sides. We need to step back and look at what design rules we need. If we're at 25-micron trace and 40-micron gap, things such as channel count and speed become much more manageable. Now the trace has become much shorter. From a signal integrity standpoint, the first thing to do is get rid of all your parasitics, get rid of all your stubs, trace, tie-bars, etc., as well as your parallelism and propagation delay; get rid of everything that will kill a signal, and then go for improved material. That's where we're at right now. We're searching the world for the best material with the best copper with the best adhesion, which means the best processes in terms of subtractive, additive or semi-additive.

Then of course the vias stick out like a sore thumb, and even 25-micron vias stick out like a sore thumb to us. So it's very important that we go vialess for all our high-speed traces. If we do that, then we can get to where we want in organic material. My whole point is, let's be organic if we can, and I don't think we're done being creative here.

Happy Holden: Sounds like RF in the digital environment.

Bird: That's exactly what it is. It's a mix of RF- and IC-level packaging. We've become a packaging company. If you really think about what we're doing, we're reinventing our schematic into smaller and smaller packages with each generation, because we know that's the only way that the speed is going to scale. So, yes, exactly that. We're at the point with a coplanar waveguide that you either use all of it, from end to end, or you use none of it. Because if you terminate a coplanar waveguide early, it will show up in the sims and in the EMI behavior, it will also show up in the bit error rate tests. So, we can discern a 50-micron movement in a via, in terms of the return path. We're revising our boards just based on pad shaving, artwork shaving. No net list changes; we're just shaving the artwork.

Barry Matties: You mentioned that you're on a material search. Have there been any surprises in that search?

Bird: Yes, we've had a couple of surprises. First, the first generation was well at hand. If we don't do a lot of chip mount on PCB, then a lot of the polyimides would work for as long as we keep them on the top or bottom layers. But in the semi-additive process and the additive process, there are a couple of materials that are starting to show up as promising, which is probably the best way to say it. We're working out a deal where one of the suppliers is actually looking at pre-drilling the blind vias and pre-seeding the FCCL, so that we can use a fab house that would normally do just the subtractive process and get them into semi-additive without a lot of work.

Holden: Sounds like shades of via ply, where the polyimide was prebuilt with 1 mil holes and then vacuum-metalized and then plated up to 5 microns thick.

Bird: That's exactly the region we're in.

Holden: You didn't have to drill or metallize any holes because the via holes were already in the substrate. You just ended up with a lot of holes in the board because you didn't use those vias and they got etched away.

Bird: Got it. Now, what we're doing is we're sending our blind via drill chart to the FCCL (flex copper clad laminate) provider so they're customized. By the time they get over to the fab shop, our blind vias are pre-drilled and pre-seeded, including the via barrels. So, it's not the only path that we're taking. We're scouring the Earth for inorganic solutions as well. We're looking everywhere we can to stay competitive and our mantra here is that we have to explore every path, because if we don't our competitors will.

We're just now starting to explore the pre-drilled and pre-seeded layer idea. We're actually right in the middle of looking at particular fab shops saying, "Is there a traveler that you could put together that would yield these types of trace, space and via features?"

Stephen Las Marias: Tony, what HDI challenges is APCT facing right now?

Tony Torres: My title is director of marketing, so I'm not going to pretend that I'm an engineer. But what I can tell you is that, when this design goes to our DFM team, besides looking at lines and spaces, annular ring and hole to copper, one important issue that we review is the materials to be used. I was very interested in listening to the discussion on what's coming. The first thing that we must do to satisfy customer needs is to come through with quality and high-reliability product. We give a lot of feedback about what materials to use. We would be very, very open in that conversation.

"The first thing that we must do to satisfy customer needs is to come through with quality and high-reliability product."

If a customer has the design already in hand and wants us to use a certain type of material, if we think that the design will be better and go through easier with a different type of material, we'll certainly suggest that. We have partnered with different material suppliers and we often go out with our sales force, with our supply partner at our shoulder, and start the design discussion of HDI work with material. It's very important that the materials work for both the OEM and the printed circuit board manufacturer. That's critical.

Secondly, we want to try to help them and guide them in design, so getting us involved early is just a tremendous help. Then we can confirm the design, confirm the manufacturability, and we're off and running. But everything is becoming thinner, smaller and tighter. Back in the day, the question was, "Can you get the hole smaller and smaller and through this board?" Now with laser drills, the issue is not about drilling the hole and getting perfect registration. Now the issue is how to get solution through the darn thing. I think more importantly, from a printed circuit board standpoint, the large departments are now in upfront engineering, being a teammate to all the customers who call in. I think the niche in the marketplace is not to simply take the Gerber files and build it, but to really be a partner to the end-customer. Be a help to them and talk out the design and get something that is not only reliable, but manufacturable.

Matties: Tony, what percentage of your customers are doing true HDI?

Vince Burns

Torres: It's unbelievable. Just two short years ago, in 2015, we were doing 20% HDI work. Our facility in Santa Clara now does 85–90% HDI work. We're a company whose mantra is to say yes to the customer's needs, in technology and in delivery. We were forced to really learn how to build HDI work because that was their very first question: Can you build this product? Then they want to know how fast we can get it to them.

Matties: Was that market demand or was that a capability that you carried out to your customers and swayed them to go in that direction?

Torres: It was market demand. The demand came from, as Happy knows, all those IPC meetings that we would attend monthly. Now the numbers in North America said that single-sided, double-sided and multilayer boards were all flat at best; HDI technology was the only growth model. Over the last three-year period, flex circuits and rigid-flex had a little bit of growth, but as far as percentage of the business, it was very, very low. The bulk of the business was HDI and so the writing on the wall was clear. That's why we made the shift in equipment and in upfront engineering, and it's paid off.

Matties: One of the advantages for HDI is that ultimately your customers wind up with a lower cost for their boards. Is that the result that your customers are reporting?

Torres: It is a mixed bag. Moving to HDI technology and keeping layer count down will ultimately wind up with a lower cost for our customer. However, there are times that, with standard through-hole technology and lower layer counts, simply adding two more layers may be more cost-effective than moving to an HDI design.

Las Marias: Thank you, Tony. Let's go to the assembly side. Vince, from your perspective at MC Assembly, what are the challenges when dealing with HDI boards?

Vince Burns: We're listening to the designer and the fabricator talk about getting layers thinner and smaller. But one of the things that we're all discussing here is the temperature cycles. Just starting out, everything that we build here must go through a reflow oven. It has to go through a reflow profile. We have to melt the solder so that we can get the parts to stick to the board, so the thinner the layers and material get, the more we're

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concerned about the adhesion of the layers, of the copper to the substrate, and the internal adhesion of the substrate layers. What I've seen in the past with boards that aren't HDI is that you'll get issues with moisture in the boards and then you'll get issues with delamination as we run through the reflow process at the surface metal level, and at the wave solder and through-hole level. And that's not even mentioning the rework.


Mike Smyth

Unfortunately, the way that the systems work is that they go through the reflow or the SMT process, and parts don't always go where you want them to go, and so you end up with rework. When we rework these things, now we're applying a 700°F soldering iron to a pad and you're more likely to have that glue that's holding the boards together come apart on you, so a big concern that we have are our thermal profiles and how these things are going to stick together. Another concern is that the smaller these parts get, the more difficult it gets for us to put solder paste on the board and have things that we can see, like the bottom side underneath the BGA. When things flow in there, we must look at it with X-ray. If we're talking about micro BGAs, we don't have a whole lot of clearance for the solder to reflow and hopefully not bridge.

Matties: How are you facing those challenges?

Burns: We're starting to use a lot more nanocoating on our stencils; we're focused in on different designs. Instead of typical round BGA pads, we're doing the square with the rounded corners, and we have to have carriers. A lot of the times, we're running boards through the reflow oven or an exterior that gives it more rigidity. It goes through reflow so you don't have any warping of the board, which can also damage it.

Matties: This of course adds cost and cycle time.

Mike Smyth: Right, and we also have an inline SPI which we are definitely checking.

Matties: For the solder paste, is jetting the solution for the solder paste in this application?

Paul Petty: It's something that we can look at. We do not have that capability at this time. We have looked at different equipment that could do that, but right now what we do is we rely on our SPI a lot. That monitors our height, volume, size. It keeps all the pads in check so that we can ensure that everything is meeting spec. I was also going to say we're sometimes constrained by our customers on which solders we can use. We have a variety of tin-lead solders and we have the RoHS-compliant solders, so we'll have a variety of the SAC solders and some others. For one customer, we use a low-temperature solder that has a high bismuth content, so we've got a huge variety of solders. Some of our customers don't allow high- or even medium-activity fluxes. We have to use ROL0 fluxes, which again creates other additional issues.

Matties: How often do designers come to you prior to designing the boards to discuss the best layout for assembly?

Burns: In about 12 1/2 years that I've been in this industry, I've had one company come to us and talk to us actively about the design of the board prior to them bringing it to us for manufacturing, and that was an interesting journey. It ended up working really well. They went through a lot of iterations of the board design before we finally got one that would work, but the vast majority come to us with a product and say, "Here, we're ready for you to start building this."

Matties: Obviously having the designer come talk to you first would be your preference, I would think. How do we get more designers to do that?

Burns: We have to convince them that there's value to be added. It's not just designing the

perfect circuit, but it has to be manufacturable, and that's where our input comes in.

Matties: One of the things that Happy mentioned in a more recent conversation is design for automation. Happy, why don't you talk a little bit about that.

Holden: Well, with design for automation, when you start investing in very expensive automated equipment, you can't afford to replace that equipment over time because designers keep trying to innovate and doing anything they want. Instead, if you've got to get payback and have a cost-effective product, this is the capability of the automated equipment. You somehow have to design within the constraint of that; otherwise you can't run it down this really great automated line. We're back to handcrafting it which is not going to be inexpensive. Automation is great, but it's not like humans. You can't reprogram it with a training course or a set of instructions. You're now constrained by the boundary condition of that automated equipment.

Matties: Do you all overhear designers talking about design for automation at all?

Torres: If I could put in my two cents from a fab standpoint, I would have the same comments as everyone else: Suppliers very rarely get involved early. If I can be so bold, I see it as a comment on business in general that everybody is just concerned with their own responsibility, their own expertise. You've got to start acting like partners, not only with suppliers, but with your internal customers as well. If that designer understood the cost problems of the purchasing department, one phone call to the fab manufacturer before the design is completed could save a lot of time and money. If you design something for manufacturability, it's going to be more cost-effective for their company, and obviously if you go one step further and design for automation, that's even better.

Paul Petty

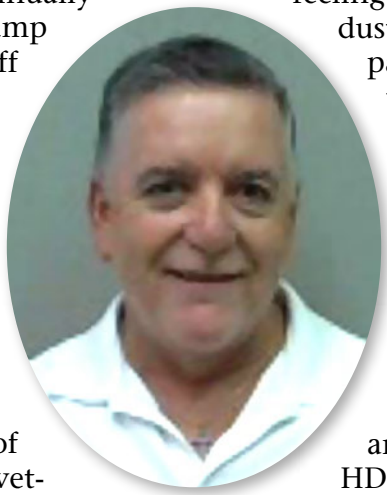
I think the companies that embrace teamwork in all facets are going to win. When you start talking about the designers, do they know that the prototype is going to go into big production? In some cases, they do, but if they had a system to always call the fab house to have that relationship, why not call the assembly house and get all the feedback before the design is completely made? Then you have a winner in all facets and you're not chasing your tail after the fact. You're saving time and money upfront. The goal is to work together as a team and share our expertise with one another.

Matties: That's a great vision. One of the things that we started talking about some years ago was DFP, design for profitability. If it's a smart design, everybody makes money. What do we do to solve that?

Bird: I've been in this industry since '79 when Happy and I worked together at HP, and the things that we care about now are so different from the things we cared about then. For instance, who cared about the height of a trace or a trapezoidal shape back then? Now we're trying to squeeze gaps down, and all a sudden, we get this metallic bathtub where we are hitting the spacing limits because we can't etch out the gaps cleanly. We use ENEPIG a lot. But now we're getting to a point where nickel, the thickest metal in the stack, is too lossy. It just goes against our density and performance goals. Therefore, we are going to be evaluating EPIG, actually more accurately EPAG (electroless palladium/autocatalytic gold). We're looking at metal thicknesses and trace features that I never thought we would see during my career.

Also, as PCB technologists, we have to be willing to go out and scour the globe, not just within our approved vendor database, for what's up to date and then next year do it again and then do it again, because things are changing so quickly. The best thing we can deliver to the engineering community? Put together a package that is properly

vetted, that you know is stable, all the delamination and via micro-cracking, etc., address all the reasons that people say why we shouldn't do it (challenge all paradigms). This means that we have to have DOEs going continually to make sure that we didn't just jump off the cliff. I'm always jumping off the cliff; Happy knows that. You really need to own it, and owning it is doing the look-aheads that you talked about—talk to your assembler, talk to your fabricator, and talk to the guy on the plating line. Talk to the guy who's running the laser drill. So this position two years ago did not exist and it does now, and the reason was because we were failing some of our substrates. Now, with proper vetting in place, we can explore just about anything that makes sense to us, as long as we qualify it before production. At this advanced level, PCB and flex technology roadmapping, PCB reliability, and the DFM process cannot be separated.


Steve Jervey

Matties: Tony, from your point of view and your role in marketing, just give us a quick overview of what you see in the marketplace. What's the feeling out there right now?

Torres: From a marketing standpoint, the goal is to keep your company "top of mind" to your customer or prospect. Because the industry had been close to flat over the past few years, I've noticed companies pulling back on their marketing efforts, when in fact I believe you should increase those efforts during challenging times. However, now in 2017, the industry is showing slow growth and more companies are coming back into the marketing arena.

What's interesting from my perspective is that the message being sent to the industry is what I see as the "standard" message: "These are my capabilities, these are my capacities, these are my cycle times, this is my equipment list and I have the lowest price!" Few, if any, talk about their people. And that's where APCT is different. Yes, you have to have the tools and equipment and the technology to be successful; however, it's the people that make the difference and I believe APCT is among the very best in that category.

From a marketing perspective, I think the feeling is wait and see. If the overall industry is showing growth, more companies will invest in marketing; if there's a downturn, companies will cut back. I strongly disagree with that perspective. The job of the marketing manager is to keep their company top of mind. Always invest in that philosophy to stay strong through upturns and downturns.

Holden: I have a question for Vince and his team. One of the problems HDI brings is limited access for in-circuit tests. Have you worked out solutions to help people who use HDI in terms of being able to use it for assemblies?

Steve Jervey: That's a big concern of ours. As a contract manufacturer, our in-circuit test traditionally has been a big part of our test solution. Over the last couple of years, I see that dying out very quickly. Our response to that in the immediate mode was to transition a lot of our work into flying probe with very small-pitch flying probe leads down to three mils on the point of the probe. We're doing a lot of flying probe work. The obvious extension to a physical test is to utilize boundary scans where we're capable of using vectorless type tests or physical access isn't there to test things. It's going to be a challenge. As things get smaller and smaller, ultimately you have to touch it somewhere to test it in some fashion and it's a challenge every day.

Holden: Technologies would help that where instead of looking for a via hole, you make an opening in the solder mask to touch any particular trace that may be available.

Jervey: Right, so that technology was pioneered by HP, I think, in the HP3070 (tester) days. They used to call it beads, where they would just eliminate the mask and put a little solder

paste on the trace itself. Of course, as speeds get higher you probably don't want to put the paste on there. Probing just the trace is certainly an option, although sometimes probing the trace will deform the trace, so now you're introducing another aspect of altering the circuit.

Las Marias: Vince, from an EMS provider standpoint, what do you think our readers should consider when it comes to HDI assembly?

Burns: Honestly, I think one of the best comments I've heard today was just more communication and better communication up front. So for the design and the fab end of it, the readers should consider contacting not just the OEMs but some EMS manufacturing facilities and ask them up front what their capabilities are. If we go smaller and smaller, what do we need to do as an industry to be able to manufacture things at that level? This also goes to the component manufacturers because now we're also looking at components that have to be mounted on these boards.

We need the designers and the fab guys to understand the conditions that these boards are going to go through when they get to our end and a lot of it is heat. We're concerned about the number of heat cycles we can run a board through, and how we can keep from damaging things as we go through the heat cycles. From the material aspect, we need to make sure that the materials are robust enough to withstand the things that we're going to put them through at our end.

Matties: All right then. Thank you, everybody. This was great.

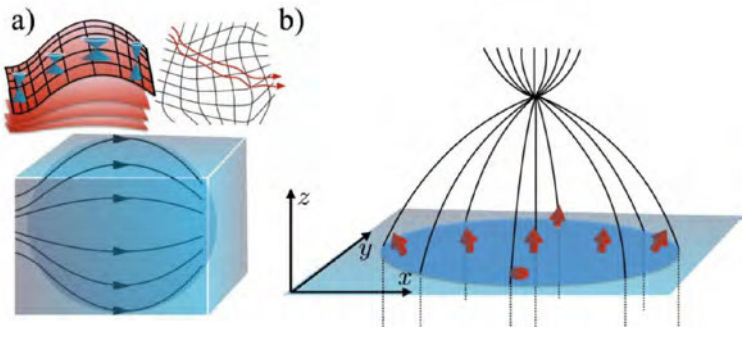
Burns: Yeah, that was good.

Bird: Thanks.

Torres: Thanks, I appreciate it. **PCBDESIGN**

New Quantum Materials Offer Novel Route to 3D Electronic Devices

In a new study funded by the Academy of Finland, Aalto University researchers Alex Weststrom and Teemu Ojanen propose a method to go beyond special relativity and simulate Einstein's theory of general relativity in inhomogeneous Weyl semimetals. The theory of Weyl metamaterials combines ideas from solid-state physics, particle physics and cosmology and points a way to fabricate metallic designer materials where charge carriers move like particles in curved space-time.



"The systems we introduced offer a route to make the charge carriers move as if they were living in a curved geometry, providing a tabletop laboratory for simulating curved-space quantum physics and certain cosmological phenomena," Alex Weststrom explains.

Weyl semimetals are an example of recently discovered quantum materials that have received a lot of attention. Charge carriers in these materials behave as if they were massless particles moving at the speed of light.

"We discovered that Weyl metamaterials may serve as a platform for exotic electronic devices such as the 3D electron lens, where the trajectories of charge carriers are focused much like beams of light in an optical lens," Teemu Ojanen says.

The theory of Weyl metamaterials also paves the way for fundamentally new electronics applications, for instance, the development of electronic invisibility devices.

Three Perspectives on HDI Design and Manufacturing Success


Mike Creeden

by Andy Shaughnessy, Happy Holden, and Stephen Las Marias
I-CONNECT007

Mike Creeden, CID+, has been in the PCB design industry for more than 40 years. In June 2003, he founded San Diego PCB Inc., a design bureau serving a variety of industries, including industrial, automotive electronics, medical diagnostics, defense, aerospace, and communications markets. The company was acquired by EMS firm Milwaukee Electronics in November of 2016. Currently, Creeden is the vice president of layout services for San Diego PCB Design LLC, which has about 18 designers and supports four CAD platforms. He is also a master instructor at EPTAC, where he teaches CID+ certification classes across the country.

San Diego PCB has designed a variety of HDI circuit boards over the years. So, for this month's issue of our magazines, we interviewed Creeden to get his insights on the challenges when it comes to HDI and how designers and manufacturers can address those issues.

Typically, HDI can improve the performance for dense, high-speed signals. HDI may have little or no effect on design cycle time. However, HDI is usually a cost adder to the fabrication cycle, with some exceptions, such as layer reduction. Most HDI issues are negligible to the PCB assembly process.

"HDI, along with almost any aspect of PCB design layout, in my opinion, should consider three perspectives for success: layout solvability, whereby oftentimes there's a complex packaging challenge involving dense BGAs or fine-pitched BGAs that need pin-escapes; electrical integrity—including all signal and power integrity considerations; and DFX manufacturability," explains Creeden. "A designer must approach HDI and any portion of PCB design layout with all three of those perspectives in mind.

"The solvability is a skillset that a designer would have to essentially understand and be competent to truly satisfy the placement and connectivity of the board with their CAD tool. HDI exists in many different forms. For example, via-in-pad. It would require half the geometry to pin-escape a board if you can put the via right in the pad. Therefore, you must consider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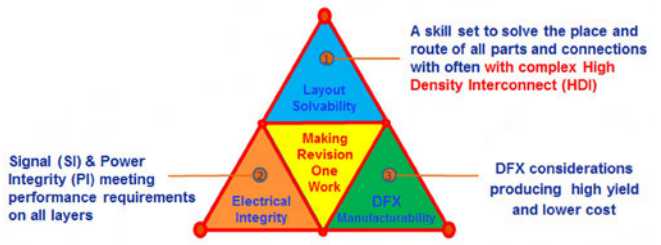


Figure 1: Per IPC-2200 series: three perspectives for PCB design layout success.

the manufacturability of that because now, you have potentially a via filling and a planarization and a plating aspect. From an electrical integrity standpoint, when doing via-in-pad, you essentially are reducing some of the parasitics, by having an extra piece of metal there to perhaps impede or affect the circuitry. Via-in-pad is a form of HDI. We're seeing BGA pin counts routinely now in the 1,500 to 2,000 range; there are some BGAs that are way beyond that, but many are in that neighborhood. With the dense pin-count of the BGA, it presents a challenge to supply power, pin-escape and completing all the routes while maintaining electrical performance. It really becomes a geometric solve whereby you may seek to utilize—even if the pin pitch is 1.0 mm—an HDI solution to pin-escape in the dense board without adding extra layers. Sometimes, you cannot add so many layers in a standard board thickness, therefore HDI is a solution to increasing layer count. However, designers must be careful because they must always respect high-speed issues, such as the return path, whereby the electromagnetic (EM) field is resident in the dielectric material between a signal and GND and a voltage and GND. You must be observant that it's not just the physical pin-escape; you must consider the electrical integrity. And again, if you are using

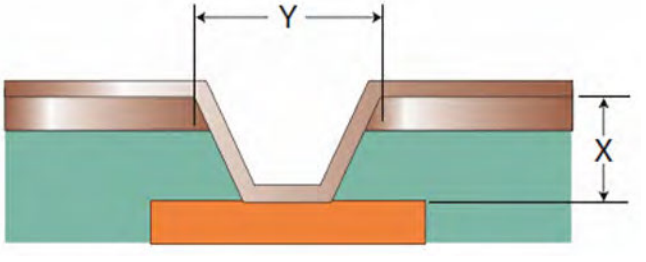


Figure 2: IPC 2221, microvia aspect ratio.

HDI, you've brought many extra process steps to the fabricator, such as considerations of FR-4 material and plating issues, to name a few."

Microvias

According to IPC 2221, a microvia has an aspect ratio of 1:1 or less. For example, with a 4-mil dielectric, you would have a 4-mil drill diameter. Creeden points out, "The reliability of microvias is high. And the reason it's high, when done right, is because of this low-aspect ratio. The plating is typically more robust and there's less chances for a coefficient of thermal expansion (CTE) mismatch, so the HDI laser via is robust, in my opinion. In design layout of finer pitch uBGAs, you can't fit a normal size via within the ball pattern and you can't pin-escape because on the surface, it is very difficult to pin-escape between two uBGA balls because you have to utilize a very thin trace. When you start considering the outer layer plating, it's difficult for the fabricator to produce a reliable thin trace on the outer surface. It's just not a robust manufacturable feature, especially if you're attempting to maintain a consistent impedance. So, you will typically have to use HDI microvias when you get into the 0.65 mm, 0.5 mm, and smaller pin-pitch uBGAs. Oftentimes, you might save money if you can find a similar functioning device and can live with a larger package size with the larger pin pitch."

Because microvias can only go down one or two levels at a time, they can be very good on signal integrity, or from a power delivery standpoint, according to Creeden. "If you have a very thin dielectric, even a buried capacitance material in layers two and three, it's very good power delivery to just tap down one to two layers to get a very low impedance delivery of your planar capacitance. To that end, it's very helpful for power delivery."

Creeden says that planar capacitance lends itself very well to HDI. "I am seeing that more on boards for mil/aerospace, as well as commercial boards with wall-to-wall components, which have BGAs on both sides of the board, and there's no room for decoupling capacitors. So, using buried planar capacitance is growing in acceptance within the industry. It is an incredibly thin dielectric, and it's a cost adder—

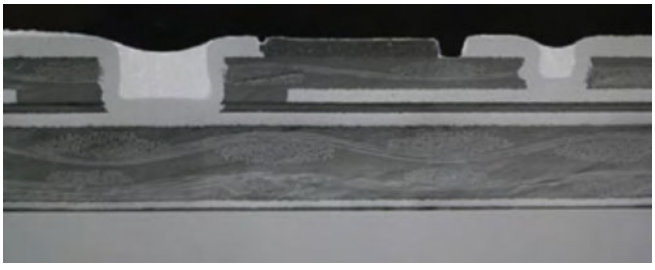


Figure 3: Example of HDI microvias accessing buried planar capacitance layers for robust power delivery.

don't kid yourselves. But it has very good performance. When you have no room for decoupling capacitors, then you may be forced to use it. Or if you work for someone like NASA or the military—maybe you're not as cost-sensitive—I recommend people consider it because it works well with HDI and improves performance."

However, there are sometimes tradeoffs when it comes to pin escape and power delivery. And therein lies the challenge brought by the number of pins in the BGA. "Whenever possible, in HDI, if you can bring your connectivity underground (layer 2), and I mean under 0.0V GND, you have EMI containment. Thus, it is easier to pass any kind of FCC or emissions testing that your product may encounter. Whenever a signal is encapsulated by ground layers, with adjacent return paths, you have good containment of its EM field, so they'll perform better, and you'll reduce noise emissions and susceptibility."

While there are a lot of signal integrity tools that try to help designers detect EMI noise, Creeden says he always encourages PCB designers to "make the EMC correct by construction and not create noise, rather than detect it."

"Another caveat that I would always recommend from a manufacturing standpoint when dealing with microvias is the concept of stacked or staggered vias. It's a methodology by which when you're utilizing microvias to traverse multiple layers, you may stack them on top of each other or stagger them, offsetting them so they're not on top of one another. When you stack a laser via on top of a laser via, they will typically end up metal-filling that. It's okay because they have a thin dielectric, and there's less stress on the via. But what you should never do is stack them on top of what's known as the 'N' or the internal mechanical drilled via, because it is always best if the mechanical drilled via is non-conductive resin filled. There are thermal expansion issues at play that create via failures. You'd see that if you look at a lot of microsections; you can see that the non-conductive fill actually retracts a little bit because it has a thermal shield being inside the via wall. So, if you stack vias on top of it, essentially you have a much greater potential of having an open via failure.

"Typically, the limit of how many microvias can be stacked is a consideration of the number of lamination heat cycles the FR-4 material can withstand, and that number is debatably about four to five. I'm sure higher-end shops may be exceeding this at some point, but the limit is the material. Other methods of stacking vias on every layer is utilized in the telecom for tablets and cellphones that are typically thin boards. This method has been called by names like: full-stack-vias, every-layer-vias, or any-layer-via. They utilize a CU-sintered conductive paste as opposed to conventional plating methods. To this end, always keep an eye out for new methods coming around the bend."

While laser-drilled vias are reliable, they still present a lot of fabrication challenges. "Understanding some of the manufacturing process that your fabricator has to work with, I always encourage people that if you want to design a stack-up, the fabricator needs to weigh in. You don't create a stack-up, then route your board, and then after that, ask for the fabricator for a DFM review. You truly need to theorize your stack-up and all the feature sizes that you need for the layout solvability, such as pin-escapes, smallest features, and overall routing completion; you must ensure that you satisfy the electrical integrity such as impedance and implementing proper EM theory. Then, get your DFM review at the start of layout to make sure this can be built. You do not ask those questions after you routed the board. I repeat: Ask those questions at the start of the design. Considering manufacturability, it's much more of a fabrication issue than it is an assembly issue. Fabricators will provide conformance certificates, and they do a lot of testing; IST and HATS testing,

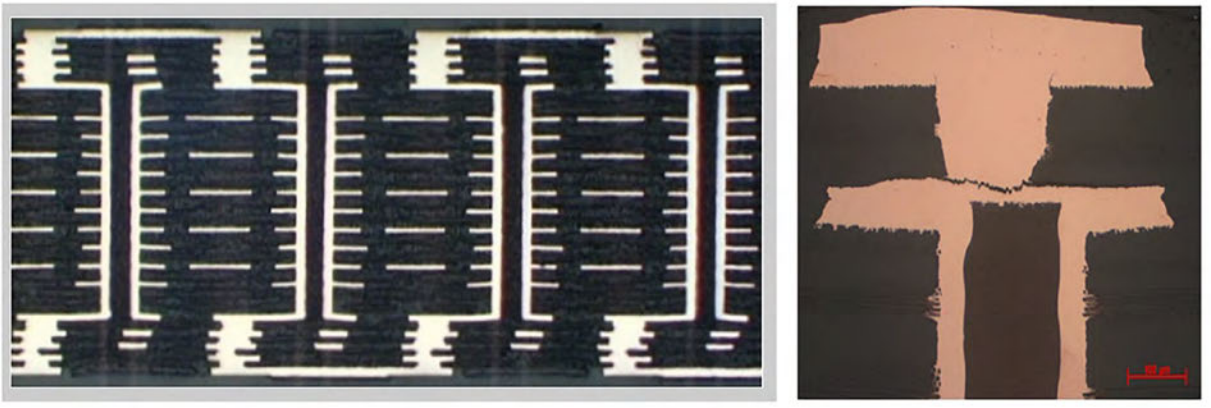


Figure 4: Never stack microvias on resin-filled vias.

are a couple of methods. However, if it's done on a coupon, you always have to ask if that coupon truly reflects the circuit as it's laid out. These designers can theorize the stack-up, but if they violate it, with the way they actually did the design, the coupons are really not representative. An asymmetrical stack-up is a good example of this occurrence, whereby the designer routes signals broadside coupled and not asymmetrical. The amount of cycles by which you test these vias in coupons—some people say 250 cycles at a certain temperature and some reports actually suggest 500 cycles—a person who wants to rely on these different testing methods should really investigate them to see where the sweet spot is, and if that fits with their budget and margin."

Designers have been asked to estimate the scope of schedule, performance probability and then provide technical feasibility for cost estimates and planning. On this, Creeden says, "I must do an estimation of this design; and typically, I can tell you early on if it's feasible and the scope. The first thing I want when estimating the scope is placement feasibility and assembly profile. I consider the placements of components to see if I can fit these components on the space provided—I do a component dispersant, where I just dump them all out on a board; at this point I don't care about the circuit flow—I just want to see wall-to-wall if I can put parts on the board. Because if I can, I could always do a via-in-pad, and I can go underground and solve the routing. The second thing I need to look at is the smallest pin pitch of the BGA. This will dictate if any sort of via grid is required. If microvias are required, now I have taken myself into an HDI scenario. Finally, when you look at a large BGA, you often-times see how many signal pins that need to pin-escape. The amount of signal pins that may need to pin-escape a large BGA may constrain how many layers will go into a stack-up. Third, I will collaborate with my production fabricator to ensure complete high-yield buildability. With these three things, I can typically give you an estimation for feasibility at the beginning of the layout phase. Designers need to talk to their full development team and complete supply chain before they go and layout the boards. It's all about being proactive, not reactive."

Testing Issues

Every circuit has different testing requirements or desires, depending on customer requirements, production plan, or end use. Several methods for testing in the should be given careful consideration depending on what best suits your situation. Different testing methodologies have varied strength and weaknesses.

"From a layout perspective JTAG testing can be one of the simplest to implement," says Creeden. "Some companies would like to have ICT. It's expensive, but way more definitive as to the condition of the manufactured board. But you need full nodal access with ICT fixtures. When I have BGA pins that use microvias such as blind and buried, you do not have accessibility unless you can breach it to the outer surface. Then you might be violating the electrical integrity. And more than likely,

if you are using the small-pin package, you don't have room for that. I design boards that have thousands of nets that would need to come out to the outer surface and often there is no room. HDI does not lend itself well to that. With these high-density challenges testing companies tend to go more into functional test or JTAG."

Assembly Front

HDI concerns lie primarily with designers and fabricators. However, one of the biggest issues when it comes to assembly is component placement feasibility, according to Creeden. "A via-in-pad, even if it's a through-hole via, is a form of HDI. Therefore, it's high-density from a placement perspective because now I can fit all the parts on the board with good DFA considerations. Because I can put a via in its pad, I can route that board. Assemblers typically don't know what it takes to route a board. They don't know what's internal. They see the outer layer—and that's mostly what the assembler will consider. Typically, what the assemblers would care about is the assembly profile. The assembler has three agents: the bare board, the components, and the bonding agent of solder. Assemblers want to ensure that land pattern provides a robust solder connection to match the component, especially getting a good solder connection underneath any BGA," he explains.

"That's critical to them. One of the concerns they are seeing now is package types known as landless grid arrays (LGA), which are like BGA but without elevated solder balls on each contact pin. I see this utilized with a lot of power supply devices. The problem, because of its coplanar mating, they cannot disperse the solder flux residue, causing it to form a barrier on the edge of the device. It's not a normal perception of an HDI issue, but when you're talking about 100 amps coming from a power-supply device, that's a high-density power issue. People have this way of thinking that HDI means only microvias; now I put to you that HDI can be something with larger features such as a landless low-profile part, which may become an HDI assembly concern. So, what a good designer might do is to add vent holes in between the pins of the landless grid arrays so they can outgas the flux residue."

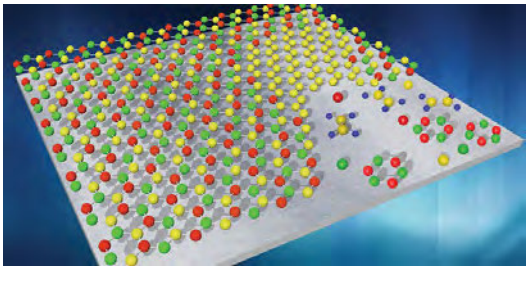
HDI is here to stay, and there are three key perspectives of concern: layout solvability for the geometry and density, electrical integrity, and manufacturability. **PCBDESIGN**

Carbon Atoms Assemble Themselves on Command

Researchers from DTU, Aarhus University, IBM, and Brookhaven have for the first time made self-assembly work in the thinnest films that exist: two-dimensional materials. The most well-known one of these is graphene that consists exclusively of carbon atoms and has outstanding electrical properties. This creates new hope for super-storage media in extremely small scale.

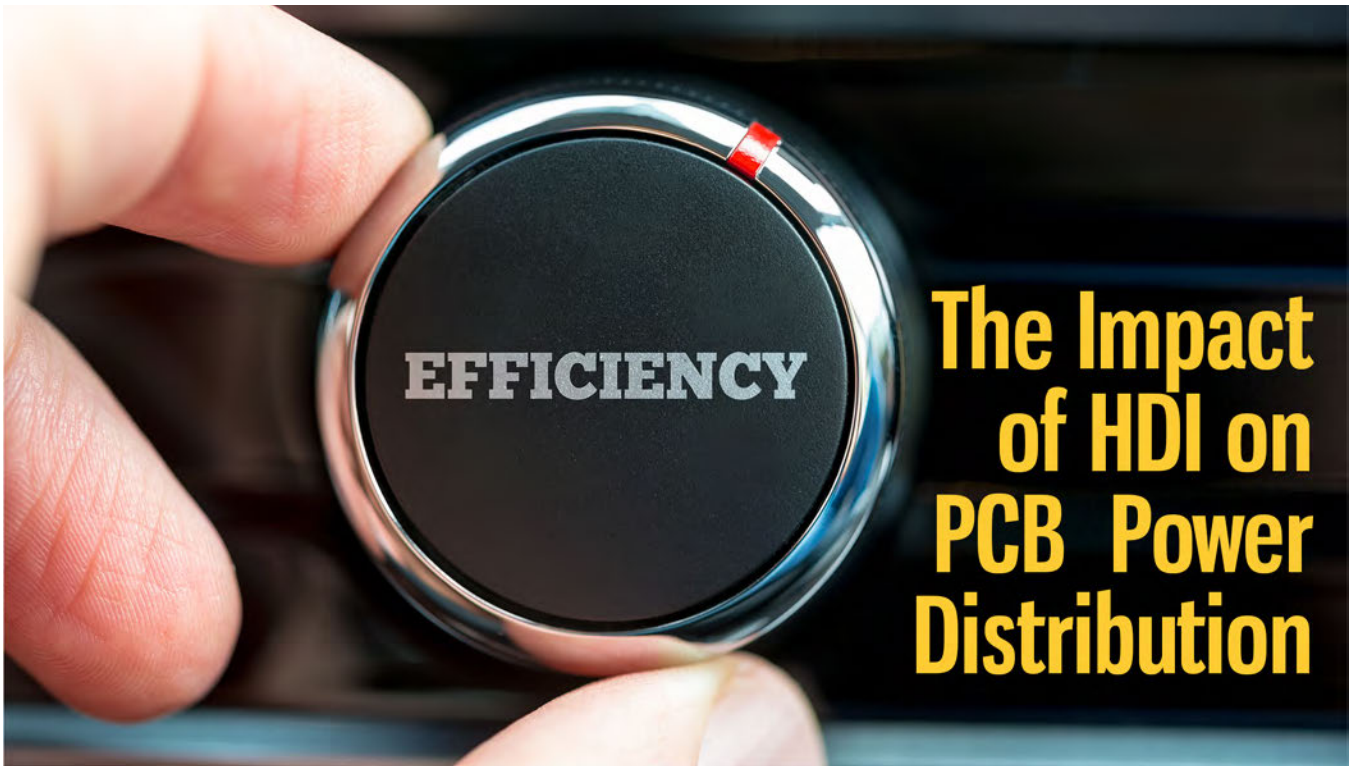
At DTU, Professor Peter Bøggild is thrilled and believes that the new discovery has a huge potential.

"We know that patterning of thin films is one of the keys to produce new properties, and—in my opinion—this is a breakthrough. We already know how we can stack materials one layer at a time, and now it appears that we can also pattern them in something approaching atomic resolution. It will be exciting to see how far we can get with this strategy."



Bøggild believes, however, that it is still too early to say anything about the applications.

"We've basically discovered a new way of controlling nanomaterials at atomic scale. Graphene islands behave like small artificial atoms and can be used for many different applications within the energy sector, biosensors, and optoelectronics. But where it gets really exciting is if we can learn to do the same with some of the hundreds of other atom-thin films that we know today." says Bøggild.



The Impact of HDI on PCB Power Distribution

by Craig Armenti
MENTOR

High-density interconnect (HDI) technology is often used to meet the requirements of today's complex designs. Smaller component pitches, larger ASICs and FPGAs with more I/O, and higher frequencies with shrinking rise-times all require smaller PCB features, driving the need for HDI. Beyond some of the more obvious electrical effects of the microvias used on HDI designs, there is also an impact to the power integrity the PCB. This includes different effects of mounted inductances of decoupling capacitors, changes in plane performance due to reduction in perforation from chip pinouts, and the inherent plane-capacitance changes from using dielectrics of various thicknesses.

HDI Primer

HDI can be a confusing topic, especially for new engineers and designers, or those not well versed in the subject matter. Although this article is not intended to be an in-depth tutorial on HDI technology, a quick review of the key aspects is appropriate.

HDI is a technology that, through a combination of high density attributes, allows for a higher wiring density per unit area as compared to traditional PCB technology. In general, HDI PCBs contain one or more of the following: reduced trace width and spacing, microvias including blind and buried, and sequential lamination.

Current generation HDI designs are typically found in mobile phones, digital cameras, laptops and wearables to name just a few. Basically, whenever a product needs to be compact and/or lightweight, then HDI technology will most likely be applied. The benefits of HDI technology include:

- Reduced space requirement using smaller vias, reduced trace width and reduced trace spacing, all of which allow components to be placed in closer proximity
- Reduced layer count as a result of increased routing channels on internal layers
- Improved signal integrity due to shorter distance connections and lower power requirements
- Improved power integrity due to ground planes closer to the surface parts and improved distribution of capacitance
- Potential to lower fabrication and assembly costs by consolidating multiple PCBs into a single PCB

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When utilizing HDI technology, two basic HDI structures exist:

1. Build-up or sequential build-up (SBU) structures
2. Any-layer structures

Figure 1 shows the breakdown of sequential build-up technologies for HDI. The three basic elements are dielectric format, via formation, and metallization method.

A key aspect of HDI technology is the use of microvias. For reference, the IPC HDI Design Committee has identified microvias as any hole equal to or less than 150 microns. Multiple types of HDI stack-ups associated with blind and buried microvias can be used to meet the density and cost requirements for today's products. Design teams should develop stack-ups in conjunction with the board fabricator to minimize cost and meet signal integrity requirements. There may also be additional requirements related to plating and specific materials. As a rule, the vendor will adjust all the stack-up variables as needed during their process to meet the end-product requirements. Common stack-up approaches when utilizing blind and buried microvias include:

1. Sequential lamination & drill
2. Type III staggered vias
3. Type III stacked vias
4. Type VI any-layer vias

Each stack-up option utilizes the same trace spacing and layer thicknesses, but the Type III and Type VI layer buildups allow for greater flexibility (Figure 2).

Introduction to Power Integrity (PI)

The goal in designing a power distribution network (PDN) for a PCB is simple: minimize the impedance between power and ground for the products frequency range. Successful execution of this goal however is not always easy. With multiple voltage rails and a limited number of planes available to carry those voltages, in addition to ever-shrinking real estate available for capacitors, the task can become quite complex.

The PDN consists of a combination of the DC-to-DC converter or voltage regulator mod-

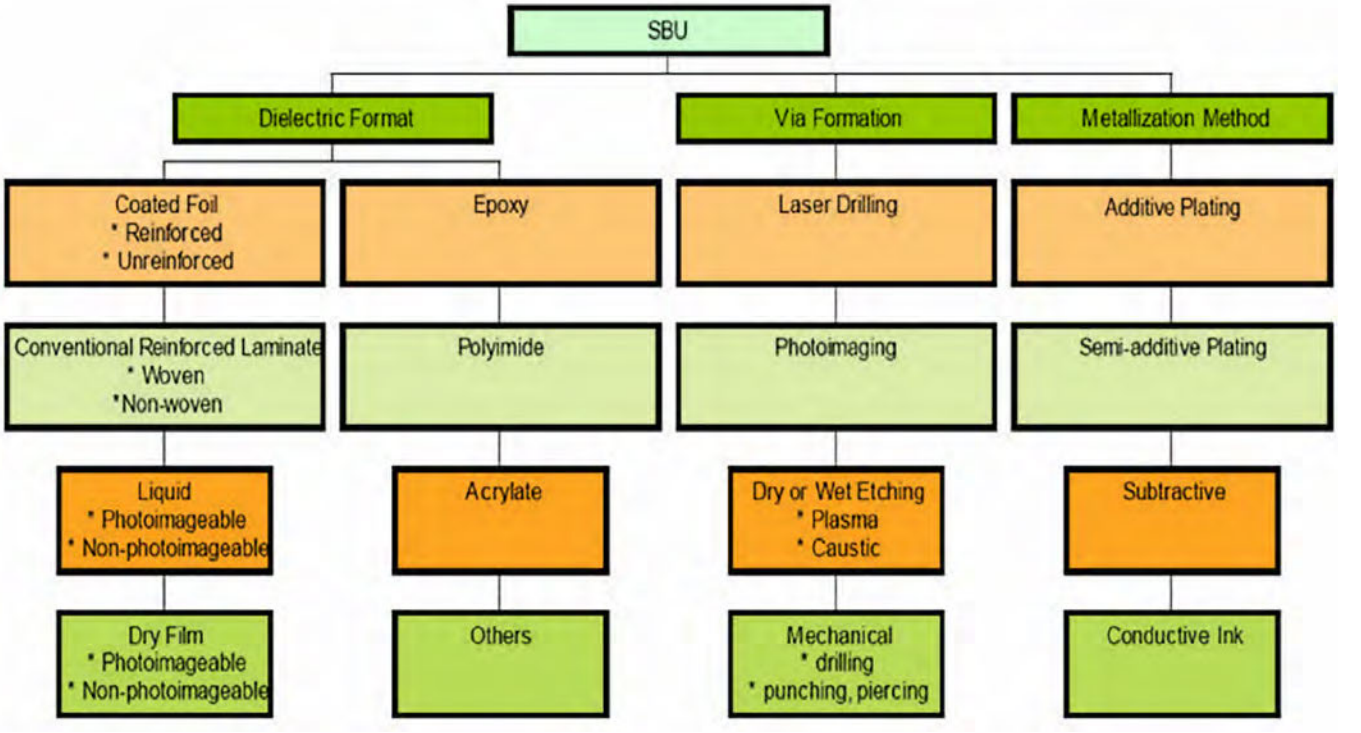

Figure 1: Elements of the HDI sequential build-up process.

ule (VRM) supplying voltage to the rail, the decoupling capacitors tied between power and ground, the planes and/or traces carrying power, on-chip decoupling, and the pins and vias connecting all these elements together.

The VRM is very effective in providing a low impedance path between power and ground up to around 1MHz. For the remainder of frequencies, the low impedance between power and ground must be provided by the board and chip capacitances. The board and chip capacitances combine in parallel, but are each limited in effectiveness by their parasitic inductances and resistances.

Without parasitics, all the capacitances would combine to make one large capacitance, which would equate to a lower impedance with increasing frequency. Unfortunately, each capacitance is only effective in a given frequency range, as determined by its parasitic inductance. For instance, very large electrolytic capacitors reach a low impedance at a lower frequency than smaller surface mounted capacitors, but because their parasitic inductance is also larger, their impedance will also start to rise at a lower frequency.

Another example is the inherent capacitance between planes on the board. The parasitic inductance of the planes is extremely low, making it an effective capacitance even at higher frequencies. Because the amount of capacitance between planes is typically limited by their area and spacing, the plane capacitance does not equate to a low impedance until higher frequencies. As such, each of the board capacitances is only effective for a certain frequency range, and must all work together to provide a low impedance between power and ground across the entire frequency range.

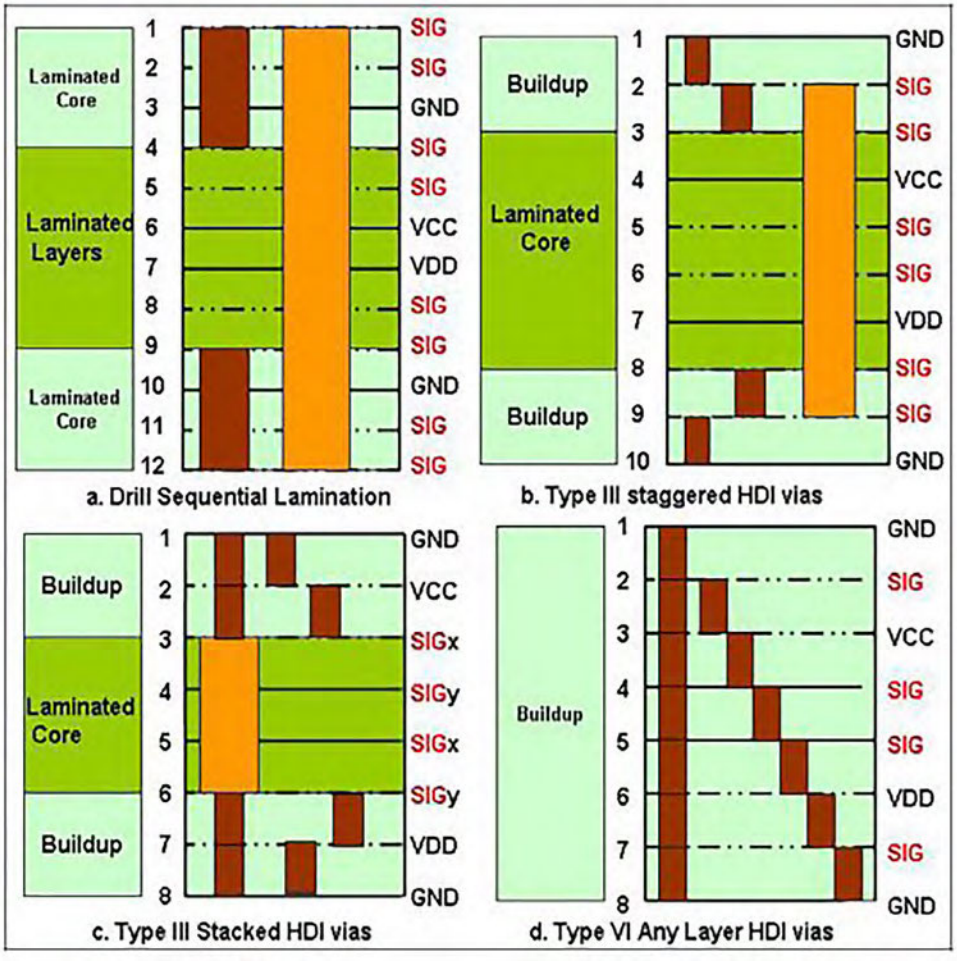

Figure 2: Cross-section illustrations of common HDI layer stack-ups.

One factor that limits the effectiveness of the board capacitances is the inductance of the chip package. This additional inductance adds to the parasitics of the board capacitances, making them ineffective above about 1GHz. Above 1GHz, the on-chip capacitance (not limited by the inductance of the package) provides the low impedance path between power and ground. As such, board decoupling is typically analyzed between about 1MHz and 1GHz, and board PDN design is focused at minimizing the impedance between those frequencies.

To make capacitors effective over the largest frequency range possible, the largest capacitance value possible for a given parasitic inductance is the ultimate goal. Parasitics for

decoupling capacitors consist of both inherent and mounting parasitics. The inherent parasitics, effective series resistance (ESR) and effective series inductance (ESL), are properties of the capacitors themselves. The mounting of the capacitors can add significant inductance and resistance, and minimizing those mounted parasitics maximize the effective frequency range of the capacitor. The most effective means of doing so is by minimizing the loop area of the connection of the capacitor between power and ground. This means placing mounting vias as close together as possible, and placing the capacitor as close as possible to power and ground. It is clear how HDI aids in accomplishing this; by allowing placement of connection vias within the capacitor pads, they are as close together as possible.

Power Integrity and HDI

Common to all methods of HDI is a significant reduction in the numbers of vias going through the inner layers of the board. The main desired by-product of this is the increase in board real estate available for routing. Also evident is the reduction in perforation of the power planes by the large number of anti-pads normally present in a chip pin-out. This results in a greater area of copper used to feed both AC and DC current to the chip power pins. There is less resistance in the current path, both to the chip and throughout the plane in general, resulting in less areas of high current density on the board. There is also less inductance leading to the chip pins, allowing for appropriate switching currents to reach the power pins, while also increasing the effectiveness of the decoupling capacitors surrounding the IC.

“Common to all methods of HDI is a significant reduction in the numbers of vias going through the inner layers of the board.”

The effectiveness of the decoupling capacitors is also affected by the location of the power and ground planes within the board stack-up. The power and ground locations are determined by the type of HDI being used. In all cases the planes will sit more towards the outer layers of the board, but the mounted inductance of the decoupling capacitors will vary based upon whether or not the planes are adjacent, and where they sit in the stack-up. This effect is evident even on a single decoupling capacitor, but becomes even more exaggerated when an entire power distribution system is viewed.

Another significant effect of power and ground plane configurations is the change in the contribution of plane capacitance to the overall power distribution network impedance. Inherent to the use of HDI technologies are thinner dielectric materials, which increase the embedded capacitance in power-ground plane pairs. Very specific thin, high-dielectric constant materials may be used for creating embedded capacitance, but even the dielectrics typically used for microvias will exhibit similar characteristics.

Plane Perforation

Often the primary motivator for utilizing HDI technology is the presence of fine-pitch BGAs on the PCB. When pin pitches approach 0.65 and 0.5 mm, it becomes impossible to route signal traces out of the BGA using conventional via technology. Via pads would be so large they would choke out any room for routing between pins, and could even overlap. Additionally, the via anti-pads would overlap and eliminate the presence of any ground or power plane within the PCB. The narrow web of copper formed by closely-spaced anti-pads, especially in BGA pinfields, can be a major weak point for the PDN, and can cause serious problems at DC. One of the advantages of HDI is the ability to use blind vias to connect IC pins only to the layers they need. This eliminates extra anti-pads on plane layers and can substantially increase the amount of copper feeding the IC power pins. For example, removing all the ground vias from the area of the power plane in a BGA pinfield results in dramatically improved DC power delivery. If ground pin anti-pads are eliminated from the power plane, and the remaining power pin

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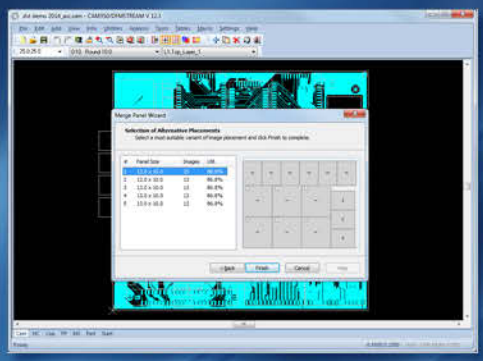

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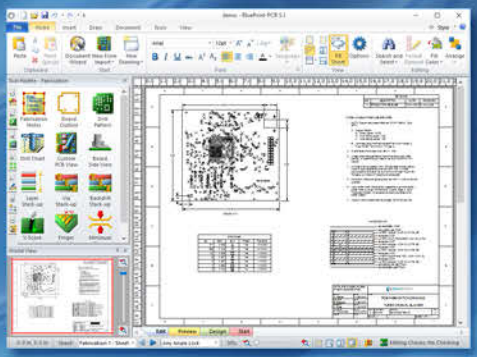

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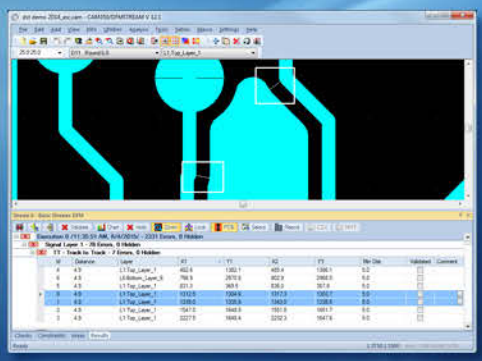

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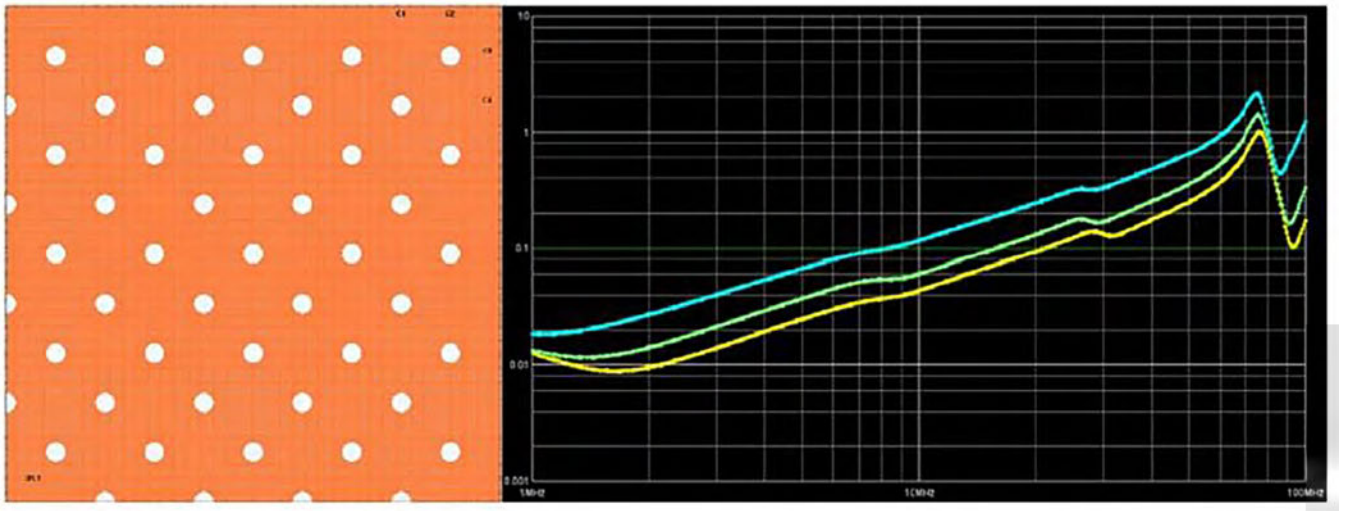

Figure 3: PDN impedance with microvias (lowest), standard blind vias (middle), and no HDI (highest).

connections are for the voltage connected to that plane, then essentially the entire area under the pinfield will be used for power delivery. DC losses will be all but eliminated.

Another benefit of HDI is the reduction in via anti-pad size. Microvias have a much smaller anti-pad than traditional thru-hole vias. The smaller anti-pad size allows for even more copper to be available for power delivery. This effect is further enhanced (though not significantly) by removing anti-pads from the plane due to reduced thru vias. The benefits of reduced plane perforation are not limited to DC power delivery. They also affect the AC impedance of the PDN. This includes the effectiveness of the decoupling capacitors as well as the inherent plane capacitance. The web of neckdowns created by typical anti-pads is high in inductance, which limits the effective frequency range of the decoupling capacitors. The improvement to power delivery by eliminating power and ground plane perforations can be substantial (Figure 3).

Mounting Inductance

Mounting a capacitor is arguably the most vital element in determining its performance. The inductance of the capacitor is dominated by its mounting. Its series resistance is usually determined by its intrinsic resistance, or ESR, but a poor mounting structure can add series resistance on the same order of the ESR. In fact, poor capacitor mounting can render the capacitor almost completely useless for decoupling.

The key to effective capacitor mounting is reducing the size of the loop area connecting the capacitor between power and ground. Ideally the capacitor would be connected directly between power and ground, but a capacitor is placed on the top (or bottom) of the board and connected to the power planes through vias. The length of those vias and their distance from each other are the most dominant factors in determining the capacitor's mounting inductance. Because of this, it is preferred to keep ground and power planes as close to the surface as possible. Keeping ground and power planes on the top layer of the board also facilitates the reduction in plane perforation outlined in the previous section, by allowing power and ground planes to be connected using blind vias or microvias and dramatically reducing the number of anti-pads in the IC pinfield.

In addition to the length of via connections, the distance between the two-capacitor mounting vias is the other main factor in determining the mounting inductance of the capacitor. The mounting vias should be as close together as possible to minimize the current loop area. That is where using HDI and via-in-pad technology become quite beneficial, because putting the mounting vias inside each of the capacitor pads positions the vias as close together as possible. In the example in Figure 4, a 0402 0.01µF

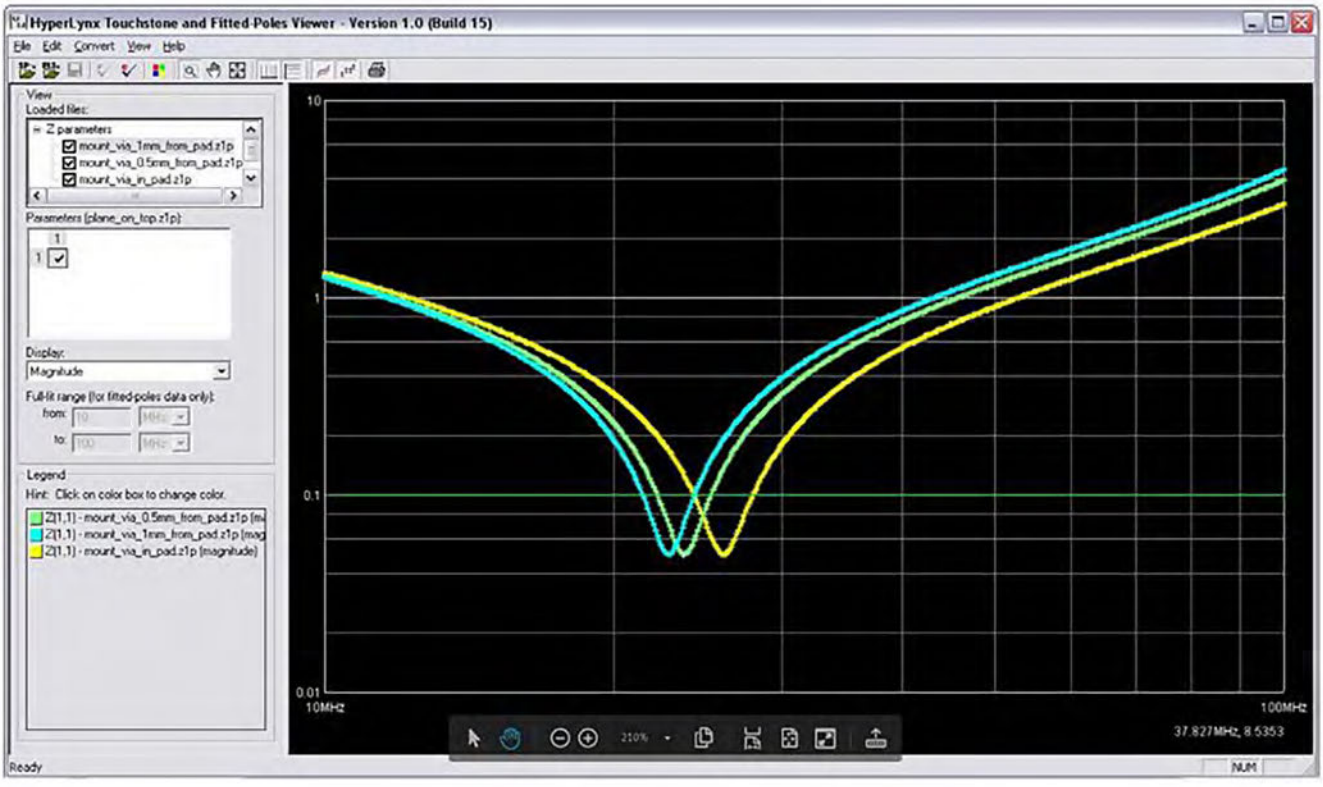

Figure 4: Impedance of capacitor when mounted using vias at 1 mm, 0.5 mm, and 0 mm from the pads.

capacitor is mounted with vias that are 80 mils (1 mm) from the capacitor pads, 40 mils (0.5 mm) from the capacitor pads, and, finally, inside the capacitor pads themselves. The capacitor that is mounted using vias inside the pads clearly shows the least amount of inductance due to the mounting method.

It should also be noted that one capacitor is often not sufficient to provide a PDN with an impedance below the target impedance at higher frequencies. Multiple capacitors must be used in parallel. Also, the capacitance of the power and ground planes must be relied upon to lower the PDN impedance at higher frequencies. This is because the planes have very little inductance.

Plane Capacitance

Increasing plane capacitance can be accomplished in one of three ways. Increase the size of the planes, increase the dielectric constant of the material between the planes, or decrease the distance between the planes. The latter two items are a by-product of using HDI technology in a

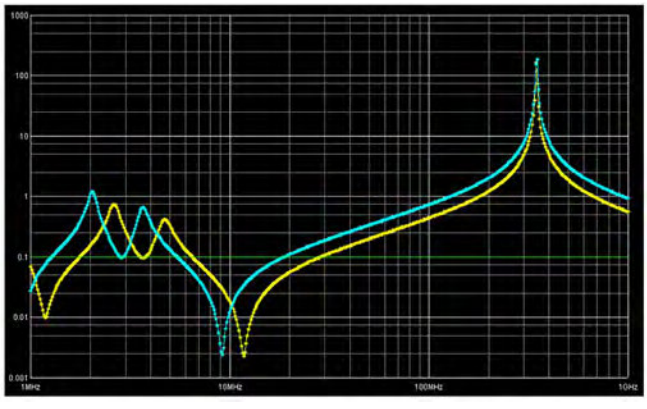

Figure 5: PDN impedance with plane spacing at 5 mils (upper) and 3 mils (lower).

design. Since outer layers are built up separately from the rest of the board, it becomes similarly cost effective to use different dielectric materials that have higher dielectric constants and are thinner than typical dielectrics. For example, when the distance between planes is reduced from 5 mils to 3 mils, a noticeable decrease in the PDN impedance occurs (Figure 5).

This example assumes dimensions and dielectric constants of standard FR-4 materials. More dramatic increases in plane capacitance can be achieved using dedicated C-ply materials, which can have thicknesses well below 1 mil and dielectric constants greater than 10.

Summary

There are several benefits to implementing HDI technology, including routability and electrical performance. One aspect of electrical performance, power integrity, is influenced significantly using HDI technology. Whether it be the reduction in plane perforation, or the reduction in mounting inductance of capacitors, or the increase in embedded capacitance of the board, an HDI board can have superior power integrity when compared to a traditional board design. **PCBDESIGN**

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Craig Armenti is a PCB marketing engineer for the Board Systems Division of Mentor, a Siemens business. Armenti has more than 25 years of experience in the EDA industry. He has held marketing and application engineering positions with several major telecommunication and software companies.

Graphene Performs Under Pressure

Scientists at The University of Manchester have fabricated highly miniaturised pressure sensors using graphene membranes which can detect minute changes in pressure with high sensitivity, over a wide range of operating pressures.

Writing in Nanoscale, Dr. Aravind Vijayaraghavan and recently graduated PhD student Dr. Christian Berger have shown that it is possible to make an atomically thin membrane of graphene float just nanometers above the surface of a silicon chip.

When pressure moves this membrane closer to the surface of the chip, the resulting change in capacitance is measured to read out the pressure change. By fabricating thousands of such floating membranes next to each other, a device can be made of exceptionally high sensitivity to pressure changes.

Dr. Vijayaraghavan said, "Despite its amazing strength, a single atomic layer thin graphene membrane is impossible to grow and handle without causing cracks and pin-holes, which would lead to the failure of the device.

"In order to overcome this, we use this graphene membrane in conjunction with a very thin polymer support layer, which allows us to produce thousands of floating graphene membranes closely packed into a small area, resulting in this highest performance pressure sensor."

Dr. Vijayaraghavan and Dr. Berger have established a spinout company, Atomic Mechanics, with a view of commercialising this technology. Dr. Berger, and fellow PhD student Daniel Melendrez-Armada, were also recently awarded the Eli and Britt Harari Graphene Enterprise award for their touch interface concept based on this pressure-sensor technology.

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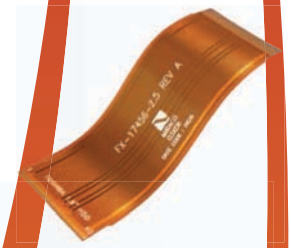

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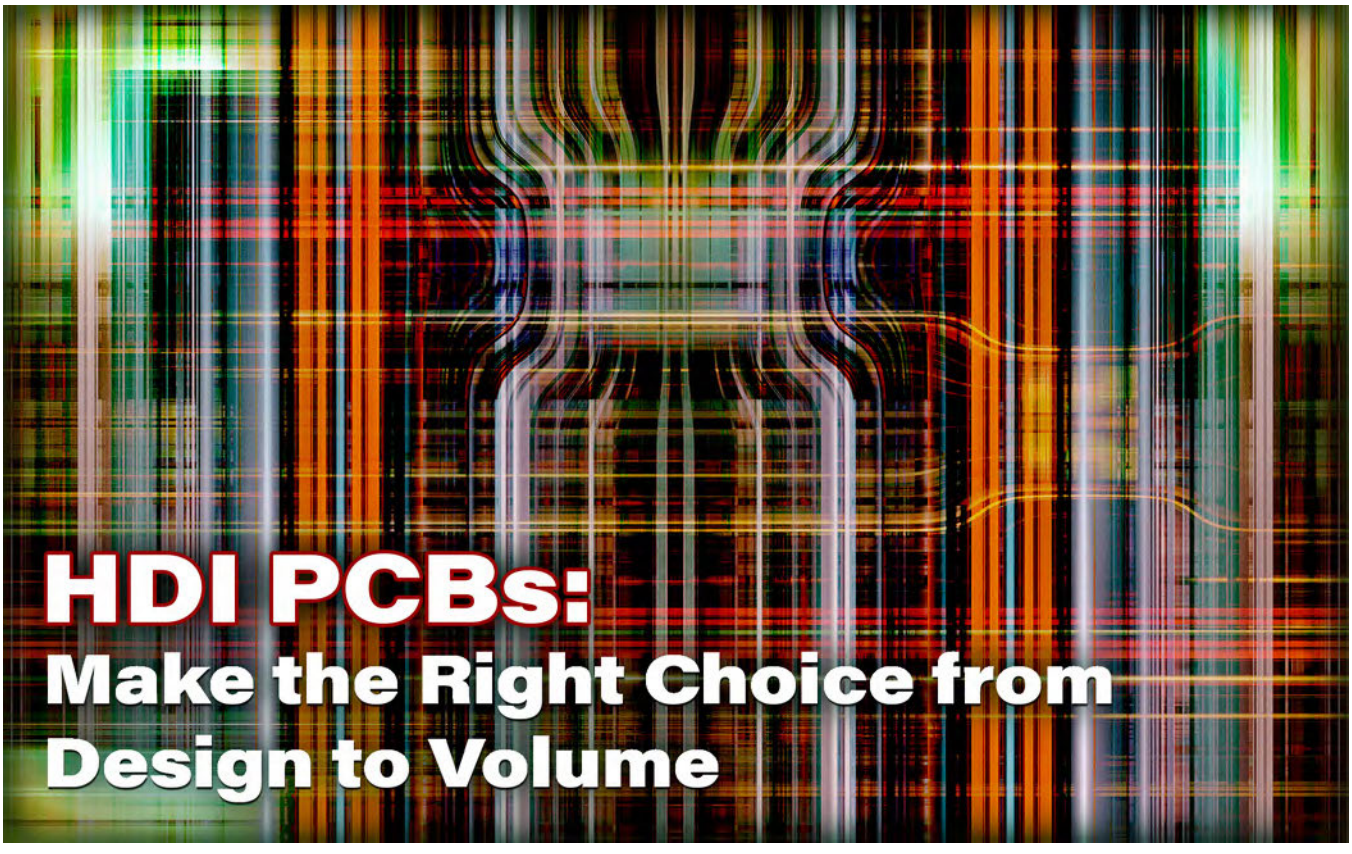

HDI PCBs: Make the Right Choice from Design to Volume

by Chris Nuttall
NCAB GROUP

Modern electronic products are expected to offer evermore advanced functions, while the products themselves are becoming increasingly smaller. This puts greater demand on the PCB design and the aspects relating to the PCB manufacturing process. There are two key factors for the successful production of HDI PCBs: first, making the right choices at the design stage, and then carefully choosing the factory that can support the specific technical demands of the project.

Whether it's consumer electronics, computers, automotive or medical technology, the overall trend is reduction in size. Not just through a reduction in actual or finished product size, but also as the components themselves are becoming smaller, so the assemblies must be more densely packed and use smaller features.

Consider the way mobile phones have evolved. A modern smartphone is so much thinner, lighter and smaller than the mobiles we had 10 years ago, but in terms of what it can do, it is light years more advanced than its predecessors. Therefore, the PCBs inside are having to accommodate more and more functions making the design itself much more complex, and all of this on smaller and smaller circuit boards.

The onset of these increasingly sophisticated electronic products, has led to more advanced PCBs becoming more commonplace.

The specifications here require high-density interconnect (HDI) solutions with greater number of layers, and more connections both on the surface and inside the PCB, utilizing finer conductor widths and narrower spaces between them. This all leads to a design that is based upon smaller, laser-drilled microvias (blind vias), since normal through-hole vias simply wouldn't fit into the space available. Therefore, we are seeing manufacturers producing more boards that also incorporate buried vias. All of which increases the number of interconnections within the board and frees up valuable space on the outer layer for more components to be placed.

The increased number of layers, together with the microvia technology, also requires the use of thinner prepegs and cores than in conventionally manufactured boards which also leads to increased demands upon the factories.

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Widespread miniaturization is putting far greater demands on the production equipment at the PCB factories. Many of the stages in the production of HDI boards are similar to those used for the manufacture of conventional boards. However, HDI production calls for considerably more sophisticated equipment to achieve the tiny geometries that are required.

Not only does incorporating several layers of buried vias and/or microvias into the boards require several additional steps, but these also need to be repeated several times and all that increases the degree of complexity and the risk of error. All the geometries are much smaller on HDI boards, which calls for better dedicated equipment designed for high-tech manufacturing. Many factories do have laser drills, but there aren't, unfortunately, as many who also possess the appropriate plating equipment and processing experience to enable them to make good-quality, reliable HDI boards. NCAB puts a great deal of time and effort into qualifying and verifying a factory before giving it our seal of approval to manufacture HDI boards for our customers.

"NCAB puts a great deal of time and effort into qualifying and verifying a factory before giving it our seal of approval to manufacture HDI boards for our customers."

The first consideration in generating microvias is that of advanced laser drills that can generate blind microvia holes with finished sized of 75 µm and below, although most microvias normally have a diameter of around 100 µm. The latest generations of these machines are capable of drilling hundreds of holes per second.

Following on from that, the transferring of the circuit pattern onto an HDI board is an equally critical operation that calls for the highest precision, which the traditional photography-based techniques can't achieve. Instead, HDI board makers either use CCD camera aligned imaging machines with parallel lighting, or laser direct imaging (LDI) systems, which images the pattern directly onto the bonded photo-imageable material. This makes for improved quality as no phototool film is used, thus enabling a much greater accuracy of transfer of pattern features down to 50µm.

Prerequisites: Correct Equipment and Clean Rooms

To ensure the best possible result in the imaging transfer process, it's vital that it's performed in special clean rooms with carefully controlled temperature and humidity levels. The clean rooms that have been used for these processes meet the US federal standard 209E Class 10000. This class has constituted the industry standard for many years now and stipulates that the concentration of airborne particles ≥0,5 µm (a human hair is typically 20–50 µm thick) in size should not exceed 10,000 particles per cubic foot.

Today the best factories have clean rooms that meet the Class 1000 requirements. To give another idea of what this means; the air in our normal everyday environment contains 1 million particles, of the same size, per cubic feet. However, good quality clean rooms are expensive, both to buy and to properly maintain.

Producing HDI boards also requires a different type of plating line. For non-HDI boards, one can usually make do with ordinary plating lines, with vertically held panels that use mechanical and air agitation, allowing you to get the plating chemicals to facilitate good copper plating onto the surfaces and into the holes (the through hole part of the plating requires good solution flow within the holes or you will not obtain a reliable or uniform plating thickness). However, this method isn't really suitable for HDI boards with blind holes that can measure 100 µm or less in diameter. That's why most factories use both horizontal plating lines as well as vertical continuous plating (VCP) lines. These methods involve spraying the plating chemicals onto the pads under high

pressure, which ensures that the microvias are properly plated.

Positioning the solder mask correctly against the pattern poses a significant challenge, since extreme components, for example 01005 and µBGA circuits with 400 µm or finer pitches, have to provide registration down to 37 µm, or in extreme cases, 25 µm. To achieve this, CCD exposure units are required.

PCB makers now have the possibility to use special LDI units to expose the soldermask, as the soldermask manufacturers have developed special soldermask inks, to support HDI designs that require lower energy to polymerize.

Looking "Under the Hood"

NCAB Group has to carry out a thorough examination of all aspects of a factory's production processes and equipment when assessing whether it meets the demands for HDI manufacturing. It's like looking under the hood and servicing the car before buying it.

If a factory claims that it has laser drills, and is therefore capable of producing reliable HDI PCBs, it's rather like saying that all you need to do to become a new Michelangelo is to get yourself a hammer and chisel. We know that laser drilling equipment is not the start and finish when it comes to HDI production; it's equally as important to have the right kind of plating equipment and the right chemistry, as well as knowing how to handle, control and verify the full plating process. We also look at what kind of chemicals and methods they're using, image transfer equipment and procedures and this is in conjunction with understanding the numbers behind the factories' real experience in this field and their performance, both of which are crucial factors.

NCAB's strategy is to ensure that we maintain and develop a best-in-class and secure factory base. We emphasize the importance of the factory being able to not only manufacture HDI PCBs, but also in keeping the number of production errors to a minimum. Producing this type of board according to the 3-4b-3 method involves laminating, drilling and plating it four times. If they return a 10% rate of failure during each round in the factory, the number of boards they would end up scrapping would exceed the volumes they deliver. In such a case you need to question the quality of the items that make it through to the delivery stage. When you consider that the components on the board can cost more than 100 times the board itself, it's imperative you can rely on the quality of the board. Otherwise, it can be incredibly expensive, if you're forced to scrap the product at a later stage.

"When you consider that the components on the board can cost more than 100 times the board itself, it's imperative you can rely on the quality of the board."

Get the Design Right from the Start

Yet another aspect you need to prioritize with advanced boards is the design itself. The margins are tiny with regard to such factors as conductor widths, isolation distances between copper features, impedance requirements, hole sizes and their relation to capture and target lands. All this poses a considerable challenge at the layout stage. The design rules should be realistic and adapted to volume production right from the start. There are several pitfalls when only considering prototype factory design rules: One example may be making the inner layer cores too thin to produce a good capacitive coupling. It might work in a prototype factory, where great care is taken to basically hand-process these thin inner layer cores. However, it could lead to major problems when the product is in volume production, since they may have different capabilities and in this instance the thinner cores may easily get stuck during the processing through long, volume-oriented etching lines since they are basically too flimsy. We thus recommend working with a dielectric spacing for a microvia layer of 60-80µm as below this may be problematic and our experience tells us that this design guideline works well across our higher-technology factory base.

EIGHT HDI PCB DESIGN PROBLEMS AND SOLUTIONS

COMMON HDI DESIGN PROBLEMS	PRODUCTION PROBLEMS DEPENDENT ON:	BEST SOLUTION
Dielectric too thick for laser vias.	Increased time for laser drilling, lower productivity. High risk for voids in the plating process, especially in the bottom of the microvias. Increased price for the PCBs due to reduced yields.	Use an aspect ratio under 0.8:1.
Too small microvia size.	Increased risk for the microvia to be blocked by unknown material and therefore won't be plated satisfactorily. High risk for poor plating of the microvia, especially in the bottom. Increased price for the PCBs due to reduced yields.	Use microvias of 100 µm with an aspect ratio under 0.8:1 for microvias intended for copper filling.
Too tight geometries in the form of too small capture and target lands for the microvia.	If the target land is too small, the risk will increase for partly missing it (so called overshoot), and material adjacent to the pad will be burnt down to the next layer. If the capture land is too small, it is a risk for the land to be broken, which is not acceptable to any class in IPC-6016.	If possible entry and capture pads should be 200µm greater than the microvia. For tighter geometries consult NCAB.
Too tight demands on permitted dimple on copper-filled microvias.	Increased price for the PCBs due to reduced yields.	Place the requirement of dimple to a maximum of 25 µm.
Too tight demands on the thickness of overplating of plugged vias. (POFV or VIPPO).	Affects the flow of the process, at a reasonable thickness of the overplating all the vias can be drilled in the same operation, which makes the process much easier. If the overplating is too thick this will reduce the possibilities to produce outer layers with thin racks/small isolation.	Set the requirements according to IPC-6012 class II and demand only ≥ 6 µm as overplating thickness.
Epoxy via plugging demands for too many different sizes of vias, this applies to both buried and through vias.	Hard to control that bubbles don't occur in the final plug, and that there won't be a problem with complete filling.	Only one size of the plugged vias are preferred, if more sizes have to be plugged, keep them within a range of 0.15 mm.
Microvia placement.	If microvias are placed directly into SMD surfaces, unnecessarily voids can arise in the solder joints at reflow soldering. The price structure increases if the microvias are copper-filled.	Pull the microvias from the SMD surfaces if possible. If there is no place to do alternative 1, place the microvias right into the pad and demand for them to be copper-filled.
Too small of a distance between the staggered holes and the microvias, microvias or microvias/buried vias.	If the staggered microvias are placed too close to each other, there is a risk that the overlaying hole can intrude on the underlying one with bad plating as a consequence. This can be solved by copper filling of underlying microvias or overplating if buried vias, all this means increased cost and risk.	Where possible we recommend 300µm between microvia holes, 220µm at lowest to ensure no processing issues.

If there's enough space on the board and the component is available with different pitches, we also recommend selecting a component with a larger pitch since it reduces the complexity of the board and saves costs.

Smaller components may be less expensive to purchase or more readily available, but this approach might render the board unnecessarily expensive in relation to its end application. Opting for small components, usually, increases the complexity of the circuitry, and therefore the board will increase in cost also.

This is where the customer should work with their PCB supplier to determine if the design needed for such components is a cost-effective one: Is the reduced cost associated with buying more readily available, but more complex components, balanced with a potentially more expensive PCB? Consider if, for example, it is to be used in mobile phones destined for the con-

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sumer market, or in low-volume production.

We are also seeing more package-on-package (PoP) type components being used in the industry. You should carefully check whether the assembly house is familiar with the technology and the extra costs it might involve. Of course, smaller components are space saving, which could produce a cheaper board, as long as it doesn't mean making it more complex, with several levels of microvias or adding buried structures etc. One invariably has to weigh up the space contra complexity issues at the design phase.

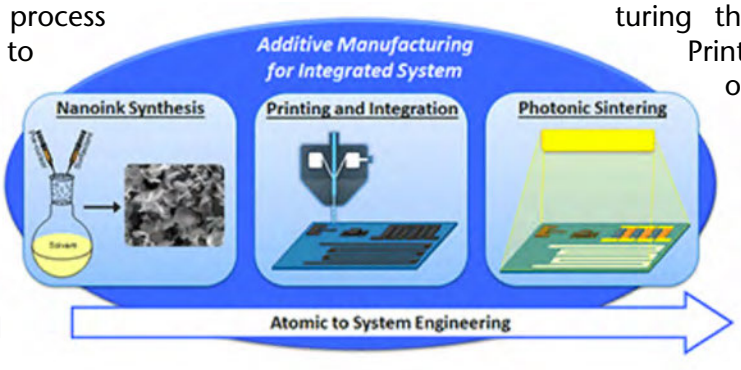
PCB producers should be involved right at the very start to help customers find the right solution. One must realize that there are real differences between producing prototypes and volume production. If you focus on the wrong things from the start, it could jeopardize the entire project if you find that your design can't be applied in volume production. We recommend initiating a seamless project together with your PCB producer at an early stage to ensure that the board can be manufactured at a reasonable cost, with the right level of complexity for the design and for reliable yields. Contact NCAB Group for a complete list of HDI guidelines. **PCBDESIGN**

Chris Nuttall is chief operations officer at NCAB Group, responsible for global operations and technology.

Additive Manufacturing May Hold Key to Transforming Nanomaterials into Multifunctional Devices

Nanomaterials have been widely studied and proven to have unique properties that make them more suited to a variety of applications. However, there is still a need to better understand their structure and property evolutions from nanoscale to macroscale as well as transform nanoscale materials into functional devices using scalable and low-cost manufacturing processes.

Yanliang Zhang, assistant professor of aerospace and mechanical engineering and faculty member in the Center for Nano Science and Technology at the University of Notre Dame, is working to do both. He and his team are developing an innovative and highly scalable additive manufacturing process that may hold the key to transform the nanomaterials into multifunctional devices. Their work aims to fabricate high-performance and flexible energy harvesters, sensors and electronic devices.



Zhang and his team are focusing their efforts on two projects in particular, one funded through a National Science Foundation CAREER Development Award and one funded through the U.S. Department of Energy.

Through the NSF project, they will be studying the additive printing and sintering processes of colloidal nanocrystals to control thermoelectric and electronic properties in printed structures. They are working to establish a scalable and cost-effective additive manufacturing process to fabricate flexible thermoelectric and electronic films.

Zhang's team is also developing advanced 3D conformal sensors using additive manufacturing through a DOE project. Printing the sensors directly onto components enables high measurement accuracy with minimal intrusion. This research has the potential to establish a new sensor manufacturing paradigm for a broad range of industrial applications.

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Strategies for High-Density PCBs

by Vern Solberg

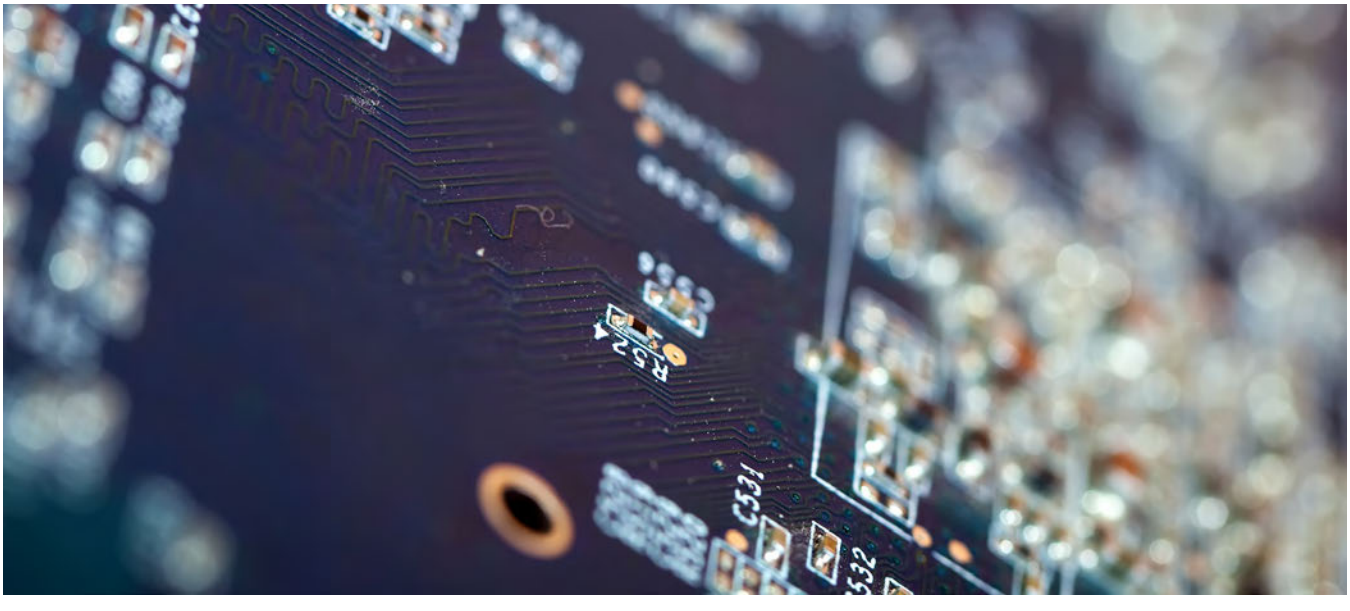
As hand-held and portable electronic products and their circuit boards continue to shrink in size, the designer is faced with solving the physical differences between traditional printed board fabrication and what's commonly referred to as high-density interconnect (HDI) processing. The primary driver for HDI is the increased complexity of the more advanced semiconductor package technology. These differences can be greater than one order of magnitude in interconnection density.

Semiconductor Packaging

Although the development of array-configured packaging for ICs has alleviated circuit routing difficulty somewhat, product miniaturization and performance goals are not easily achieved. To further complicate the PCB design process, many companies furnishing multiple die or multi-functional semiconductor packaging are forced to significantly increasing I/O while reducing both contact size and pitch. This higher I/O and finer pitch evolution is due in part to the OEM need for more capability in an ever-shrinking space. Further complicating traditional PCB design, some companies are doing away with some or all traditional semiconductor packaged semiconductors.

System-in-package (SiP), for example, whether die stack or package-on-package, has rapidly penetrated most major market segments. This includes consumer electronics, mobile, automotive, computing, networking, communications, and medical electronics. The benefits of SiP will differ for various market segments but they can share some very common elements: shorter time to market, smaller size and lower cost. Area efficiency (more functionality in a single package footprint) has resulted in the strongest initial penetration in consumer electronics. These mixed function SiP solutions have become commonplace in small form factor systems, such as mobile phones, memory cards, and other portable electronics products and the number has been increasing rapidly.

In contrast, it has become common for developers to procure bare, uncased die elements that are configured for facedown (flip-chip) mounting. Although flip-chip was originally considered for relatively low I/O die, the redistribution of the peripheral located contact sites to a more uniform area array format has enabled



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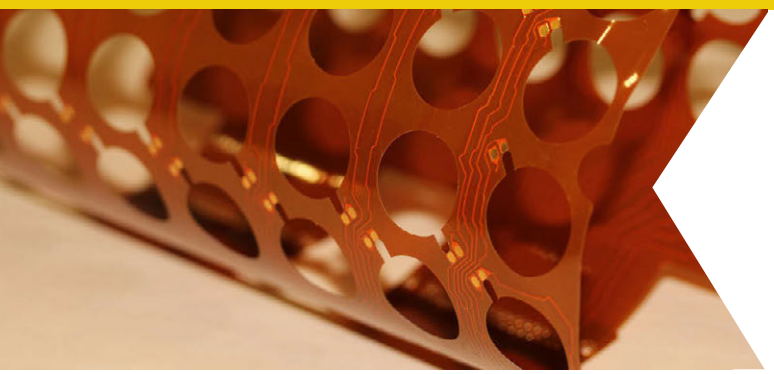

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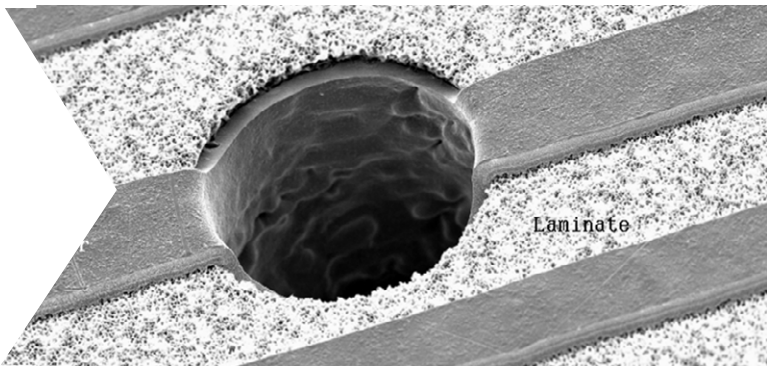

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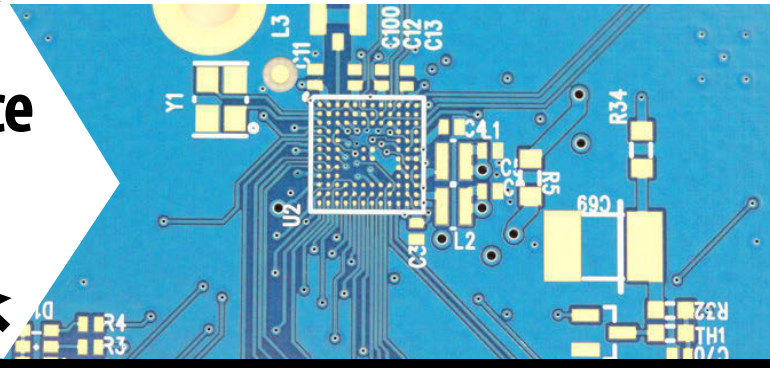

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the commercial use of larger and much higher I/O die elements. Regarding flip-chip mounting, interconnection from die element to the PCB is commonly achieved with alloy bumps, spheres or, for very fine pitch applications, raised copper pillar contacts that, although very small, are compatible with a conventional reflow soldering processes.

Achieving Higher Circuit Density

For many applications, the cost of high-density printed circuit boards has remained a detractor. Although PCB complexity has increased, however, the prices for HDI have declined and analysts expect this trend to continue to decline further each year. This is due in part to increased competition but the trend can be attributed to diligence in refining fabrication process methodology and controlling material utilization. Process refinement includes the development of more efficient imaging capability, improved etching and plating chemistry and refinement in base materials and lamination methods. Many user companies have already established a business relationship with these key suppliers and have qualified their level of expertise and capability. Regarding specifying narrow copper conductor width and spacing, the IPC-2226 has defined three HDI complexity levels for both external and internal locations (Table 1).

Some companies can produce copper conductors as narrow as 25 µm (1 mil) but they likely rely on using dielectric materials that have a very thin copper foil or utilize base materials prepared for a semi-additive copper plating process. But, before committing to adopting any level of HDI technology, the designer should confirm that the PCB suppliers selected are able to meet the required complexity level with acceptable process yields at the anticipated production quantity.

A key contributor to enabling higher density circuits is in the advances made in circuit pattern imaging. Circuit pattern imaging traditionally relied on first digitally imaging the circuit pattern onto polymer-based film masters then, using contact imaging to transfer the circuit pattern onto photo-resist emulsion applied to the copper-clad panel surface. Many fabricators have streamlined their processes by transferring the circuit image directly from the CAD file onto the panels resist coating using laser technology. Both laser direct imaging (LDI) and digital imaging (DI) systems have become mainstream technology for a wide segment of the PCB fabrication industry. Direct imaging eliminates extensive process steps required in preparing the film masters and avoids physical distortions attributed to varying thermal conditions and humidity on the polymer-based film masters.

Hole and Via Forming Methodologies

Mechanical Drilling

Drilling systems are manufactured by a broad number of companies worldwide and can range from a single spindle head system for low volume applications to multiple spindle head configurations to accommodate very high-volume fabrication requirements. Mechanical drilling is the most economical and efficient method for providing holes in circuit boards. The current generations of precision NC drilling systems are designed for accuracy and high throughput and many systems support post lamination profile routing capabilities.

Regarding specifying via hole size, mechanically drilled and plated vias can be furnished as small as 100 µm to 150 µm (4–6 mils) by some, however, the drill bit selected to furnish a finished

Conductor L/S	Level A	Level B	Level C
Internal conductor width	127µm (.005")	75µm (.003")	50µm (.002")
Internal conductor spacing	127µm (.005")	100µm (.004")	50µm (.002")
External conductor width	127µm (.005")	75µm (.003")	45µm (.0017")
External conductor spacing	127µm (.005")	100µm (.004")	45µm (.0017")

Table 1: Complexity levels for HDI technology as outlined in IPC-2226.

Laser Via Diameter	Target Land Diameter	Stop Land Diameter
50 µm (2 mils)	150 µm (6 mils)	150 µm (6 mils)
75 µm (3 mils)	180 µm (7 mils)	180 µm (7 mils)
100 µm (4 mils)	200 µm (8 mils)	200 µm (8 mils)
150 µm (6 mils)	330 µm (13 mils)	280 µm (11 mils)

Table 2: Via diameter to land diameter ratio variations.

hole size of 200 µm (8 mil) diameter will be more practical, less prone to breakage and, because they can be sharpened, facilitate a longer life.

Laser Ablation

When a circuit board design requires hole diameters smaller than 150 µm (6 mils), fabricators will generally adopt the CO_2 laser ablation process to form the vias, however, alternative laser technologies may be employed to initially ablate the copper foil. There are five common variations of laser-ablated and plated vias: through-via, blind via, buried via, stacked via and staggered via. Laser-ablated and plated through-via holes are used for general interconnect applications that connect conductors on the outer surfaces of the board as well as connecting to layers within the multiple layer circuit structure. In addition to through-via applications, laser-ablated and plated blind vias will furnish interconnect from either outer surfaces of the board to conductors on designated innerlayers. These vias may be placed in lands that are only slightly larger than the initial via diameter. Designers can also position the plated blind via within the component's land pattern geometry; however, these via holes must be specified as 'plated closed' and flush with the outer copper surface of the board. This is because any remaining depression within the land pattern's surface can result in void propagation with the solder interface, especially a concern for array-configured components.

The buried via may be mechanically drilled or laser-ablated on one or more inner or core layers of the multilayer board structure. These vias will be specified as plated and filled prior to the lamination of additional build-up layers. Multilayer boards can be designed using vertically stacked via processing. This process is used for more complex structures requiring circuit layers to be processed and laminated sequentially, ablating and plating vias in the copper foil and chemically etching the circuit features before laminating the next layer. A variation of the stacked via process is the staggered via where via lands are slightly offset from one layer to another.

A key issue is the aspect ratio of via diameter to the overall thickness of the copper and dielectric. Via diameter to land diameter ratio requirements may differ from one supplier to another but the following table may be referenced as a base for discussion (Table 2).

Regarding stacked vs. staggered via reliability, some experts acknowledge that, although the small layer-to-layer interconnecting vias will furnish a robust interconnect solution, stacked vias are said to be less robust than the staggered via alternative. As always, the designer is advised to establish dialog with the PCB fabricator early in the design stage of the program. They will be the designers' best source regarding guidance in material selection and fabrication process planning. **PCBDESIGN**

Vern Solberg is a technical consultant specializing in surface mount technology and microelectronics. He has served the industry for more than 30 years in areas related to both commercial and aerospace electronic product development and holds several U.S. patents for 3D semiconductor packaging innovations. To read past columns or to contact Solberg, click here.

EDADOC Discusses HDI Design and Manufacturing

by Andy Shaughnessy
I-CONNECT007

Shenzen-based EDADOC, which has been specializing in high-speed PCB design for 14 years, has now expanded to include multiple manufacturing facilities in China, and offices in the U.S. and Japan. The company now offers HDI design and manufacturing services for customers around the globe. I recently caught up with EDADOC's Bruce Wu, a designer with 18 years of experience, who also serves as vice chairman of the IPC China Designers Council. I asked him to chime in on his company's HDI processes and some of the current trends he's seeing in HDI.

Andy Shaughnessy: Tell us a little bit about your company.

Bruce Wu: EDADOC was founded in 2003. We focus primarily on high-speed turn-key PCB services, including PCB design, fabrication, assembly, and parts sourcing. We are now the largest high-speed PCB design bureau in China, with more than 500 engineers on staff.

We launched our PCB fabrication business in 2009 and currently have factories located in Shenzhen and Sihui, capable of providing 2-64 layers of PCB fabrication for prototype and mass production. We built the first quick-turn SMT facility in China. We also offer testing and box-building services.

Shaughnessy: What percentage of your designs are HDI?

Wu: Each year, our company creates over 10,000 single board designs, and HDI PCBs make up 10% of this total. The percentage is not very high, because we make designs for a wide range of industries, including communications, medical equipment, computers, industrial control, aerospace, military, consumer electronics and other segments. HDI is mainly used in thin, light consumer electronics products, but not commonly in communications, medical, aerospace and other fields where reliability is emphasized.

Shaughnessy: Are these primarily for the domestic market in China?

Wu: At EDADOC, we see demand for HDI technology in the Chinese, North American, and Japanese markets. HDI technology enables the design of end-products that are more miniaturized, while meeting the higher standards

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of electronic performance and efficiency. It is widely used in mobile phones as well as digital cameras, notebook computers, automotive electronics and more. There is market demand for HDI in both domestic and overseas markets.

Shaughnessy: What are the biggest challenges you face with your HDI designs?

Wu: The small board size, more functional modules, and packaging miniaturization (0.35 - 0.5 mm BGA) all cause a design bottleneck. As a result, smaller line widths (<3 mils) and multilevel HDI designs need to be used.

The design of multi-stage HDI boards requires a flexible, powerful constraint manager that recognizes both microvia and common mechanical holes and sets the spacing constraint between microvia and other elements. The constraints of the network become complicated, and need to support the check of the network spacing constraints in various situations. To help the design engineers manage projects, we require the ability to clearly display different types of vias.

With Cadence's design tools' HDI design and processing capabilities, EDADOC's PCB designers have completed countless high-density miniaturization product designs. Figure 1 depicts one such design, a three-stage HDI board. The density, design of the minimum line width and spacing of 2.4 mils challenged the industry's limits. EDADOC also helped this customer with the board fabrication and assembly.

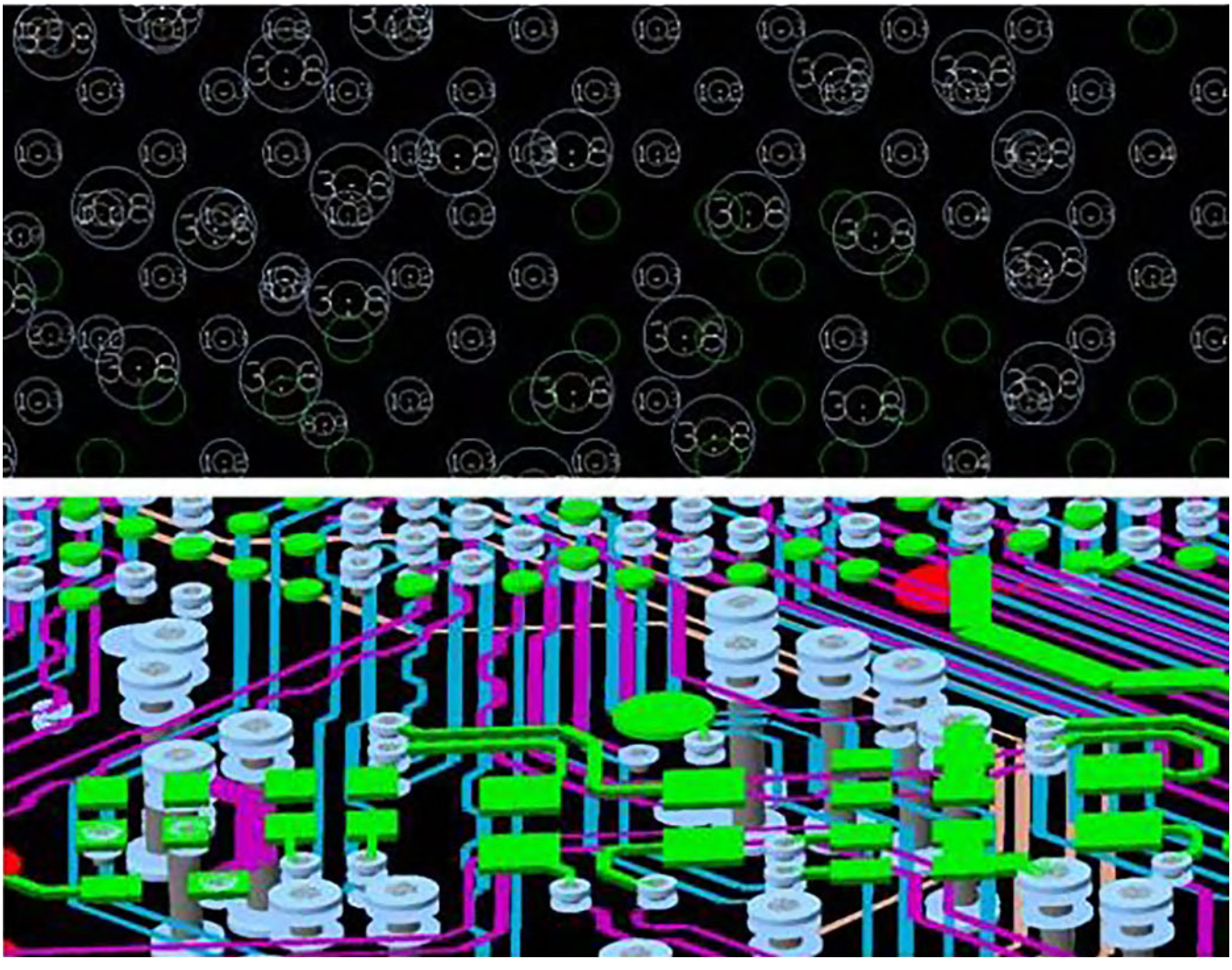


Figure 1: A three-stage HDI board design.

Shaughnessy: What trends are you seeing in HDI?

Wu: The emergence of HDI technology is responsible for the recent growth of the PCB industry. HDI allows the PCB to be populated with denser BGA and QFP parts. With the development of high-speed serial bus technology, signal transmission rates continue to increase, and the impact of the parasitic parameters has drawn more and more attention. Engineers are studying ways to reduce the effects of parasitics in vias. Due to the design requirements of vias-in-pads, you can reduce the parasitic surface device parameters. Therefore, HDI is also gradually applied to high-speed PCB designs to avoid having high-speed signal stubs that are too long. We believe that line width and spacing will transition from the current mainstream of 3/3 to 2/2 in the future. The current mainstream HDI stack-up, 2 + n +2, will transition to stack-ups of any order for HDI carrier boards.

The traditional market for HDI boards has been mobile phones. At present, nearly all this generation's intelligent machines use HDI for the motherboards, and the expansion rate has been improving at a slow rate. However, HDI may be replaced by higher process-level carrier boards in some of the next generation's models. Now that the market is being saturated with smartphones, market growth will continue to slow down.

In addition to the advantages of high wiring density and high signal integration, HDI also provides better electrical performance and signal integrity in data communications, so future opportunities will be emerging in automotive electronics and communications base stations. In the automotive electronics industry, modules for navigation, Bluetooth communication and data require the use of HDI boards. Car electronics, communications base stations, medical equipment and other emerging product areas continue to rise in terms of incremental growth rate, far beyond the traditional 3C products. This area is projected to overtake the smartphone market as the main growth point for HDI technology.

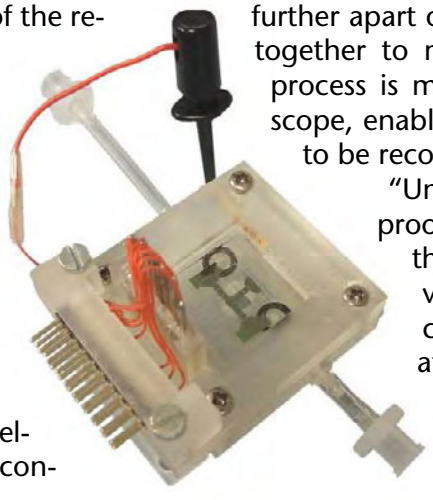
Shaughnessy: Thank you for your time, Bruce.

Wu: Thank you, Andy. **PCBDESIGN**

A Powerful Duo

Fraunhofer researchers have developed a new technology that enables biochemical reactions to be monitored from start to finish at the single-molecule level. All that is needed to perform such tests are tiny sample droplets of the reagent solution.

"The ingenious feature of our system is that for the first time we can observe the details of how the two droplets interact at the single-molecule level—thus allowing us to monitor the entire chain of events," says Lorenz Sparrenberg from the Fraunhofer Institute for Applied Information Technology FIT.



The electrowetting system developed by Sparrenberg and his team consists of an array of electrodes on a chip, hence the name electrowetting-on-dielectric (EWOD) system. Depending on the switching state of the electrodes, the droplets can be manipulated to move further apart or closer together, and be brought together to merge in a predefined spot. This process is monitored using a confocal microscope, enabling high-resolution measurements to be recorded.

"Until now, we have concentrated on proof-of-concept, demonstrating that the combination of our EWOD device with confocal microscopy is capable of providing information at the single-molecule level. We are now looking for industry partners to help us develop concrete applications," says Sparrenberg.

PCB007 Highlights

EPTE Newsletter: Can Toshiba Survive?

Toshiba was the leader in the electronics industry, and developed and marketed many types of electronic equipment and devices that included word processors, printers, VCR cameras, tape recorders, hard disc drives, transceivers, laptop computers, facsimiles, cellular phones, and more.

The Right Approach: Navigating Process Change? TPC is the Key

Change is a given. While this adage may be quite true and normally a good thing, it can wreak process engineering havoc in a printed circuit operation. Change is good, but the operative word phrase is controlled change relative to the complex processes involved in manufacturing a printed circuit board.

Flex Talk: The Man Behind the Curtain

"Pay no attention to the man behind the curtain." This famous quote from The Wizard of Oz conjures up the image of Dorothy, the Tin Man, the Cowardly Lion and the Scarecrow discovering that the great Wizard of Oz isn't as grand or as magical as he seems.

Catching up with FineLine Global

With locations all over the world and technology offerings covering all technologies, I wanted to see for myself what this "broker on steroids" was all about—how they got started and how they grew. So I was delighted to have a conversation with Eli Ikan, Fineline Global's General Manager.

RTW SMTAI: Prototron Continues its Growth

Dave Ryder and Russ Adams of Prototron Circuits discuss the firm's 30th anniversary and their continued growth. Prototron recently hired several new staff members, and the company still has one open position to fill.

American Standard Circuits Upgrades to ISO 9001:2015

American Standard Circuits has recently upgraded their ISO quality management certification to the latest standard, ISO 9100:2015.

3D Printed Electronics for Printed Circuit Structures

Printed electronics is a familiar term that is taking on more meaning as the technology matures. Flexible electronics is sometimes referred to as a subset of this and the printing approach is one of the enabling factors for roll-to-roll processes.

Bay Area Circuits Celebrates Manufacturing Day 2017

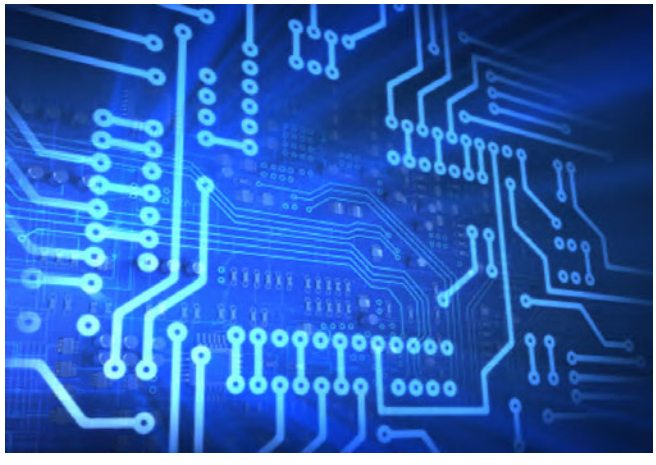
"Manufacturing Day continues to be an opportunity for us to connect with engineering students and introduce high-technology manufacturing to them as a viable career path," said Brian Paper, chief operating officer at Bay Area Circuits.

All About Flex: Flexible Circuit Failure Analysis

Design reviews and early involvement by a circuit board fabrication house can minimize the possibility of field problems, but despite best efforts, there remain occasions when diagnosis of a poorly performing design is required.

A Guide to IPC Survey and Report Season

IPC Director of Market Research Sharon Starr found time to discuss the recently conducted and published surveys and research reports and a few others still in the works. These reports are free to survey participants, which is certainly a great incentive for taking the time to complete them. (Hint: That's a call to action for those of you sitting on the sidelines.)



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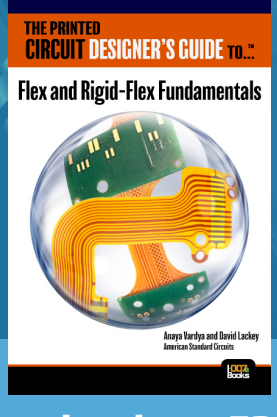

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Next-Gen PCBs—Substrate Integrated Waveguides

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

As PCB transmission frequencies head toward 100GHz and beyond, the current mainstream PCB technology, the copper interconnect, is reaching its performance threshold. Ultimately, it is dielectric loss, copper roughness, and data transfer capacity that are the culprits. However, the biggest performance restriction for PCB interconnects is the size of the conductor. Metallic waveguides, on the other hand, are a better option than traditional transmission lines, but they are bulky, expensive and non-planar in nature. However, recently substrate integrated waveguides (SIW) structures have emerged as a viable alternative and are ideally suited to the high-speed transmission of electromagnetic waves.

SIW are planar structures fabricated using two periodic rows of PTH vias or slots connecting top and bottom copper ground planes of a dielectric substrate as shown in Figure 1 (left). In this month's column, I will review the substrate integrated waveguide and its incorporation with the microstrip transmission line.

Since SIWs are fabricated as part of the multilayer PCB stack, they can be integrated with other planar transmission lines. SIW retain the low loss property of conventional metallic waveguides and are widely used as interconnects in RF and microwave high-frequency circuits to improve bandwidth. However, the signal propagates through the dielectric material rather than through air which slows the signal transmission speed, to about half the speed-of-light, which is still more than adequate for this application.

Transmission lines in the form of microstrip, stripline, coplanar waveguide (CPW), and their derivatives of geometry, have been the backbone of the modern electronic systems for many years. Following the evolution of IC technologies and processing techniques, these fundamental structures have been continuously studied and improved to meet the constantly updated bandwidth and expanded capabilities requirements.

However, the ever-increasing demands for bandwidth and performance, as well as the highly anticipated applications of millimeter-wave (mmWave), have raised the fundamental question of whether classic copper transmission lines are able to cope with the demands for low loss and low dispersion propagation.

Note: mmWave frequencies refer to the electromagnetic spectrum with wavelengths between 1–10 mm representing the frequency range between 30–300GHz. Despite the efforts to evolve and improve the existing transmission line structures, it remains a technological challenge, which necessitates the emergence of a revolutionary concept.

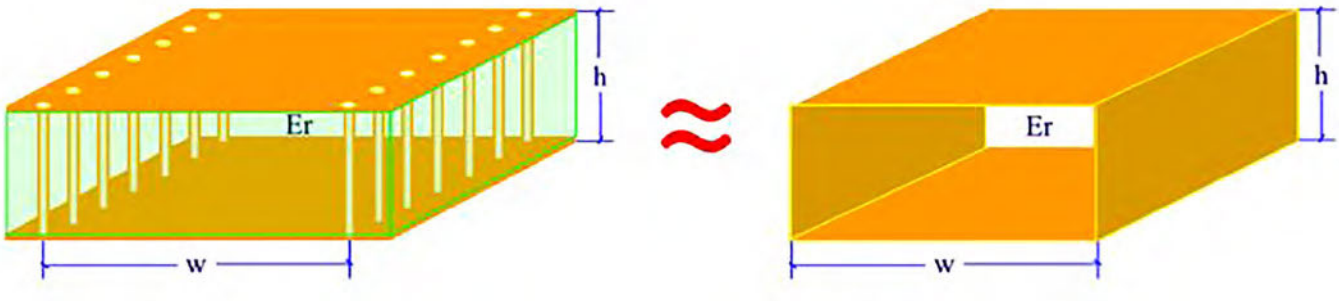
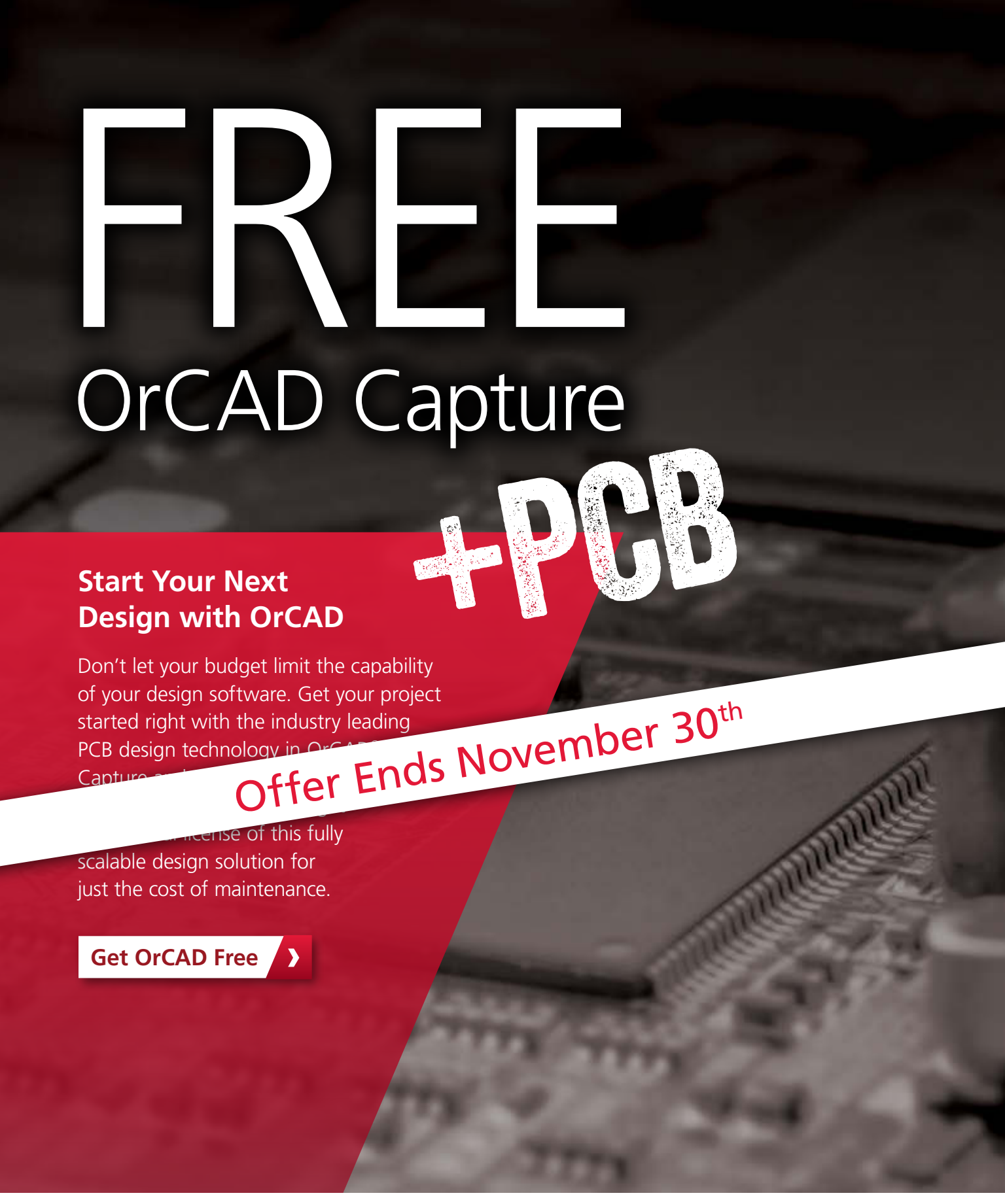


Figure 1: The SIW (left) has similar properties to the metallic waveguide (right).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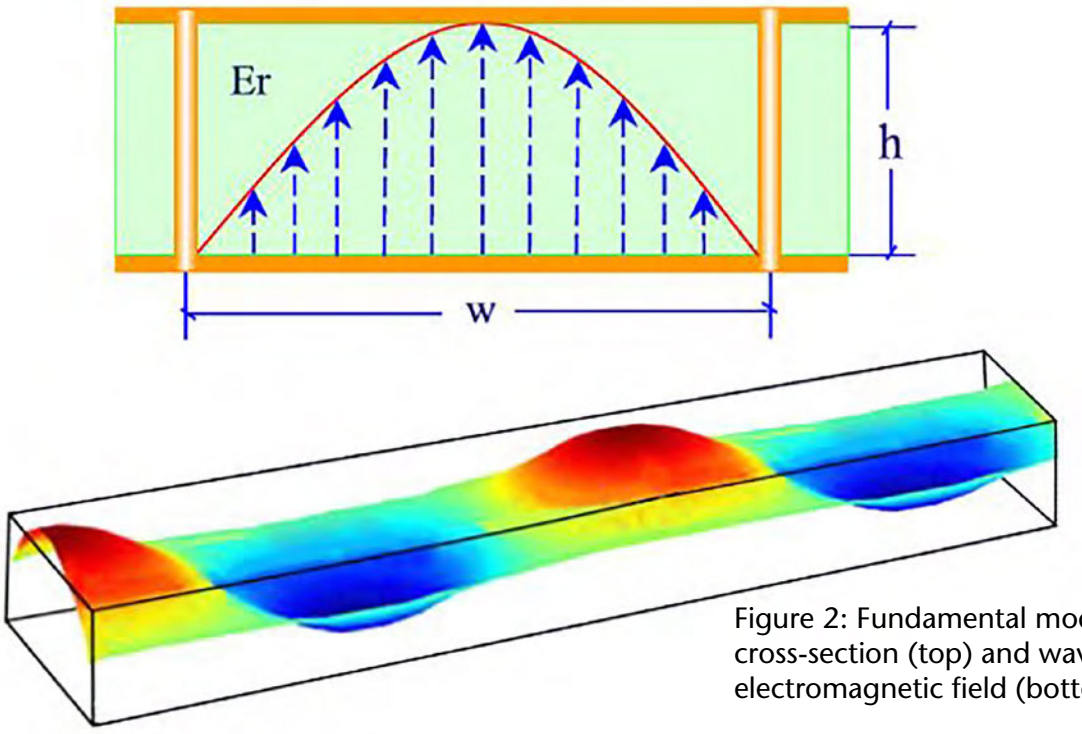

Figure 2: Fundamental mode SIW cross-section (top) and waveguide electromagnetic field (bottom).

Current high-speed PCB interconnects exhibit the following issues:

1. Limited current carrying capacity.

This is basically due to the trace width–3 to 7 mils is the typical range. That is, a signal carrying circumference of 6 to 14mil for stripline and half that for microstrip, without including the sidewall and current crowding. Current crowding, due to the skin effect, reduces the effective capacity by limiting flow, to the outer surface, regardless of the copper thickness.

2. High dielectric loss of the substrate material.

Standard high-speed materials are too lossy however, a more homogeneous, ultra-low loss dielectric solves this problem. Although, the current costs are prohibitive, compared to commonly available dielectric materials, this is likely to come down as the industry accepts them as being necessary.

3. The copper surface is too rough which increases resistive loss.

At high frequencies, the effective resistance of the copper increases relative to the additional distance over which the current must transverse the contours of the surface. This can be alleviated by using smooth copper. However, the copper foil is produced smooth and then roughened purposely, in two stages, to prevent de-lamination.

4. The signal data transfer capacity is limited by distributed losses.

Pragmatic effects, such as frequency dependent losses, come into play at clock frequencies above 1GHz. They are of concern for fast rise time signals, with long trace lengths, such as multi-gigabit serial links. This frequency dependence causes rise time degradation and reduces the upper bandwidth, of the signal, resulting in reduced channel data transfer. Substrate integrated waveguides can be used as an alternative to improve the bandwidth however, the transitioning from the familiar microstrip or CPW to a SIW can be a challenge.

Similar to the signal propagation characteristics of the traditional waveguide, the electromagnetic wave in a SIW also moves forward, reflected along a zigzag route between the two fences of vias. Since the vertical metal walls are replaced by PTH via fences for the SIW struc-

tures, propagating modes are very close to, but not identical to, those of the rectangular waveguides. Each SIW has a specific lowest transmission frequency. The cut-off frequency (fc) is proportional to the width (w) of the particular SIW where c is the speed of light and Er is the dielectric constant of the substrate material.

$$fc = \frac{c}{2 \,.\, w. \,\sqrt{Er}}$$

The most distinguishing characteristic of the SIW is the current distribution of the vias. The surface current on a traditional waveguide can flow forward in any direction. However, the current on the SIW, via barrel surface, is limited to the vertical direction only. As the vias are discrete, the current cannot flow longitudinally across the regular intervals. Therefore, the electric field in the SIW can only travel in the transverse electric mode (TEM), perpendicular to the direction of propagation as shown in Figure 2 (top).

Several types of transition from SIWs to microstrip or CPW structures are possible but as mentioned previously, can be challenging to implement. They can be roughly divided into single substrate or multilayer substrate applications. Dual-layered SIW transitions to microstrip or CPW structures have been successfully applied. But multilayer SIW circuits often suffer from alignment issues. Z-axis alignment, of the multilayer laminate book, has always been a major limitation of implementing any broadside coupled application.

The requirement that the TEM field in the SIW be adapted to the fundamental mode of the transmission line is common to all transitions involving SIWs. However, due to the similarity between the traditional waveguide and microstrip modes, the microstrip to SIW transition is undoubtedly the simplest to implement.

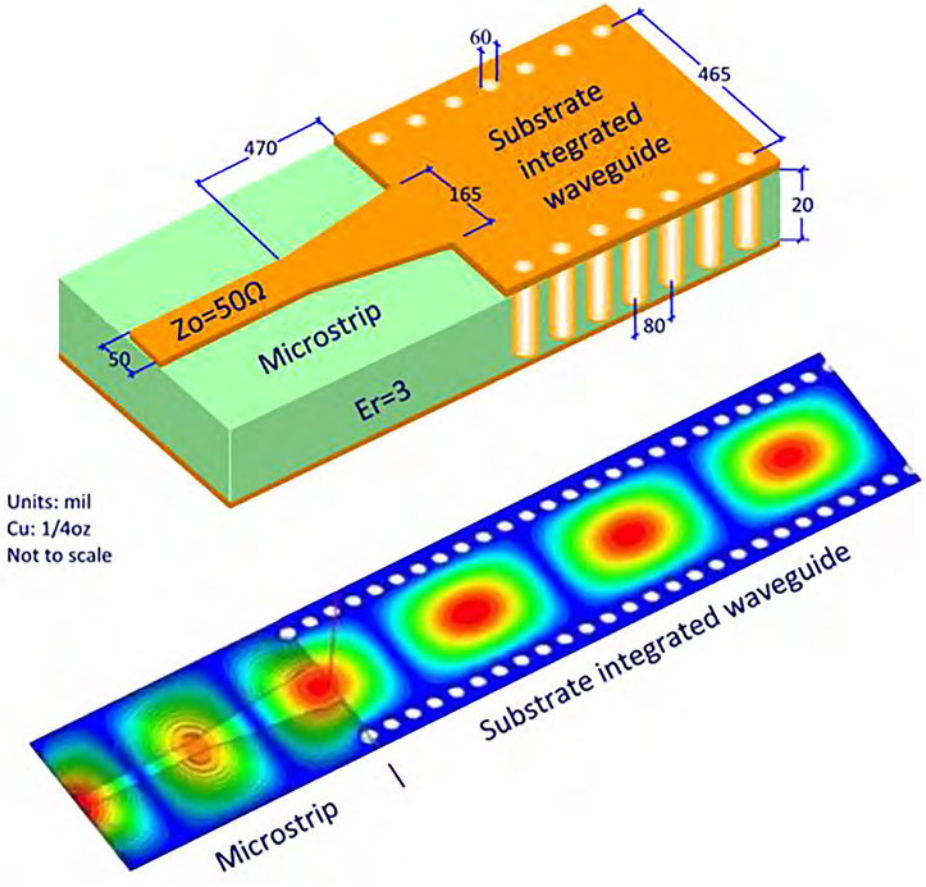

Figure 3: Microstrip to SIW transition and simulated electric field (source: Kumar[3]).

Figure 3 illustrates the transition from a microstrip transmission line to a SIW. The propagating electromagnetic wave, which is guided by the microstrip trace, travels through the dielectric, solder mask and air. However, as the wave enters the SIW, it begins to tunnel between the ground planes and as such, the dispersion losses are solely based on the losses of the substrate material. A homogeneous, ultra-low loss dielectric provides the best frequency response.

Elaborating on how the requirements, of the transition, are calculated is beyond the scope of this column however, the associated equations are provided in a paper by Kumar et al [3]. Although, I can confirm that the impedance of the microstrip trace is 50.45Ω (simulated by the iCD Stackup Planner), one would expect the impedance to remain constant at ~50Ω through the SIW to perfectly transfer the energy. The simulation, of the electric field, shows how the losses reduce as the electromagnetic wave enters the SIW. Here the field become more intense, and less distributed, providing clarity of signal and thus higher bandwidth. Obviously, another similar transition back to microstrip, at the other end to receive the signal, is also required.

Substrate integrated waveguides are low loss structures that provide high bandwidth and eliminate the need for both differential serial (SERDES channels) and space consuming parallel busses. They exhibit similar performance to traditional waveguides but, can be built as planar PCB structures. This greatly reduces the cost and tremendously improves the performance, of data transfer, compared to the traditional PCB interconnect to 100GHz and beyond.

Points to remember:

- Conductor size, dielectric loss, copper roughness, and data transfer capacity impact on the performance of copper interconnects at high frequencies.
- Recently substrate integrated waveguides (SIW) structures have emerged as a viable alternative.
- SIW are planar structures fabricated using two periodic rows of PTH vias or slots connecting top and bottom copper ground planes of a dielectric substrate.
- SIW retain the low loss property of conventional metallic waveguides.
- PCB interconnects have limited current carrying capacity, high dielectric loss, rough copper surfaces and restricted signal data transfer capacity.
- SIW propagating modes are very close to, but not identical to, those of the rectangular waveguides.
- The most distinguishing characteristic of the SIW is the current distribution of the vias, which is limited to the vertical direction only.
- Microstrip to SIW transition is undoubtedly the simplest to implement.
- Substrate integrated waveguides are low loss structures that provide high bandwidth and eliminate the need for both differential serial (SERDES channels) and parallel busses. **PCBDESIGN**

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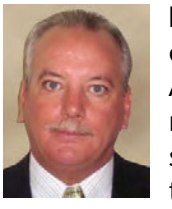

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au.To contact Olney, or read past columns, click here.

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- Barry Olney

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MilAero007 Highlights

Cloudy with a Chance of Radiation: NASA Studies Simulated Radiation

In each life a little rain must fall, but in space, one of the biggest risks to astronauts' health is radiation "rain". NASA's Human Research Program (HRP) is simulating space radiation on Earth following upgrades to the NASA Space Radiation Laboratory (NSRL) at the U.S. Department of Energy's Brookhaven National Laboratory.

Sensible Design: Thermal Management—The Heat is On

Thermal management materials are designed to prolong equipment life and reduce incidences of failure. They also maintain equipment performance parameters and reduce energy consumption by reducing operating temperatures, and minimising the risk of damage to surrounding components.

Update on IPC's Validation Services and Hints of What's to Come

SMTA International is the perfect time to get updates on IPC happenings. One that I'm always curious about is the Validation Services programs. At the busy show, I managed to find a quiet spot so Randy Cherry, IPC's director of Validation Services, could fill me in on the latest.

Developing New Magnetic Device Materials

Assistant Professor of Electrical Engineering Luqiao Liu is developing new magnetic materials, known as antiferromagnets, that can be operated at room temperature by reversing their electron spin and can serve as the basis for long-lasting, spintronic computer memory.

American Standard Circuits Upgrades to ISO 9001:2015

American Standard Circuits has recently upgraded their ISO quality management certification to the latest standard, ISO 9100:2015.

Developing Sensors to Defend Aircraft Against Lasers

MIT Lincoln Laboratory team is working on ground-based cameras that detect sources of laser beam attacks on aircraft and may lessen dangers for pilots.

Drones to Grow Mind of Their Own

The use of drones is gaining popularity among environmentalists and law enforcement officials alike due to the robots' ability to reach far-flung locales not easily accessible to humans. A person typically sets the drone on a pre-determined path to collect data.

New Radar Sensor Provides Clear Vision in Any Weather

DARPA's Video Synthetic Aperture Radar (ViSAR) program recently completed flight tests, successfully demonstrating a new sensor that can capture real-time video through clouds.

Global Defense Spending Momentum will Provide $771 Billion Opportunity for Industry

The Strategy Analytics Advanced Defense Systems (ADS) service report, "Global Defense Spending Outlook 2016-2026," forecasts the global defense budget will grow to $2.41 trillion in 2026, with the opportunities available to industry growing at a CAGR of 3.5%, to reach $771 billion.

Rockwell Collins' Cabinconnect Wireless Offering Addresses the Growing Trend Toward Bring Your Own Device

Rockwell Collins is addressing the growing passenger demand to be connected on their own devices while flying with its CabinConnect™ inflight wireless connectivity and entertainment solution.

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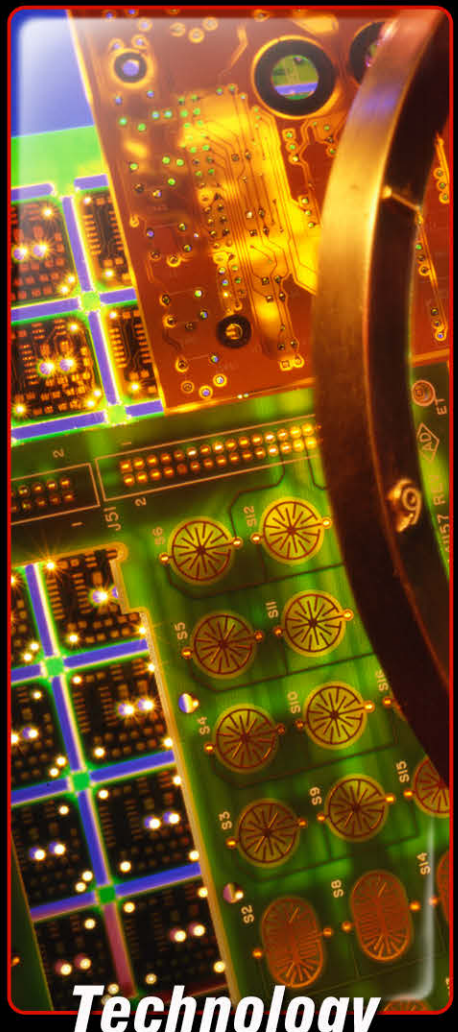

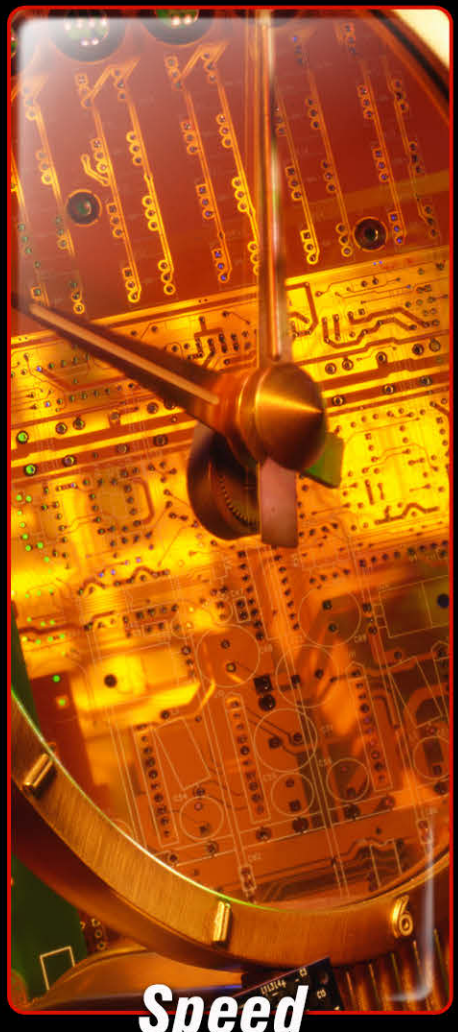

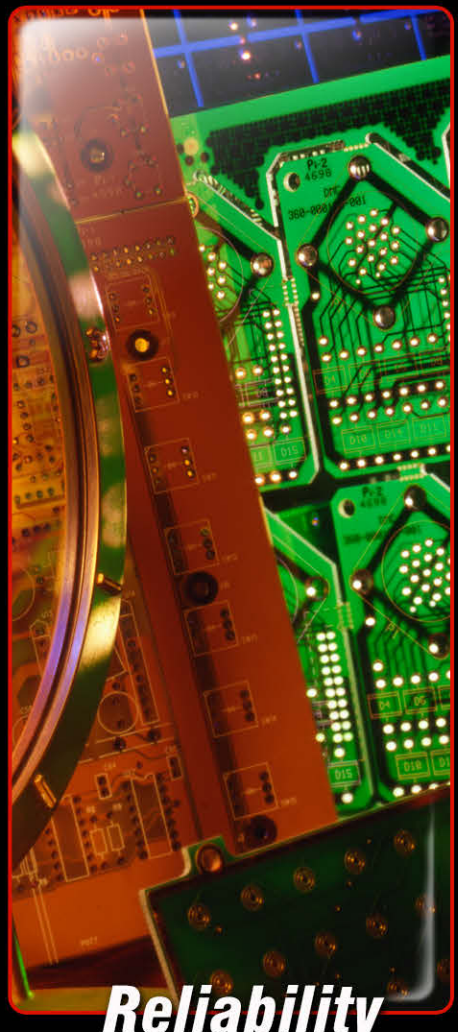

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Don't Lose Sight of Who You Really Are

by Tim Haag
CONSULTANT

"Aviate. Navigate. Communicate!"

When I was learning to fly, my instructor pounded this pilot's credo into me so much that it would pop up in my dreams at night. "Aviate, navigate, communicate" is a phrase that remind pilots the order of priorities when flying. Communicating is important, but not if it interferes with knowing where you are and where you are going. Navigating is the second most important, but not if it interferes with flying the plane, and aviating is the most important of all. In other words, don't allow yourself to be distracted with navigating and communicating so that you make a mistake in flying the plane.

As much as I would like to say that I never made a mistake in this area, I would by lying to you if I did. On one extended solo flight, I got distracted trying to figure out the landing pattern of the airstrip below me. Since I was used to the flat countryside around my home airport, geographical obstacles were the last thing on my mind. I should have been paying more attention to my surroundings, however, as the local terrain was much more interesting then what I was familiar with. There was a river, some meadows, a small town and the freeway. Oh, and there were also several hills close around the airstrip as well.

I was in a gentle turn after crossing the airstrip at the mid-point of the runway in order to align myself for the correct landing pattern. I was also talking on the radio to alert local air traffic of my intentions, and I was keeping an eye out for any other planes in the area. It's not that I was ignoring what was right in front of me; I had just never been in the position before where I had to dodge a mountain. All of a sudden, I realized that the ground was beginning to rush up at me because I had allowed myself to get too close to one of those hills.

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Now, don't panic. I didn't have an impromptu plane-mountain meeting. I was still a good eighth of a mile away from the hill, and by tightening my turn I was able to avoid the problem with a respectable amount of clearance. But that incident taught me an important life lesson about the dangers of distractions, and the need to focus on what is right in front of you first. As PCB designers, we are skilled at what we do and doing a good job is one of our highest priorities in life. All too often though, circumstances and distractions can take our focus off of that priority.

"As PCB designers, we are skilled at what we do and doing a good job is one of our highest priorities in life. All too often though, circumstances and distractions can take our focus off of that priority."

Lately, I've been working on a project that requires me to update and refresh my high-speed design skills. I've been spending a lot of time studying information from several different sources, so much, in fact, that my head began to get overloaded with theories, statistics and figures. When it came time to work with all of this updated knowledge, I found that I was floundering and doubting myself because I had become overwhelmed with all of my research. I was trying to go so deep into the subject and answer questions that weren't even being asked of me that I ended blocking my ability to do the work that actually needed to be done.

Then it hit me; I was trying so hard to become something else that I forgot who I already am. I don't need to become a high-speed designer; I already am a high-speed designer. What I needed was to get my priorities straight. I don't need to reinvent myself; I just need to enhance the skills that I already have. Once I embraced this basic principle, it freed me up to take control of my project with a newfound confidence.

Last month this magazine focused on signal integrity, while this month the theme is HDI. Talk about going from the frying pan into the fire; if you are new to these concepts, you may feel like the heat is on. It's a good thing that next month's issue will focus on thermal management!

If you are suddenly confronted with some of these technologies in your design, and you haven't worked with them before, it may seem like you've just been thrown into the deep end of the pool. When I took swimming lessons as a child, the thought of going into the deep end of the pool was absolutely terrifying. I didn't have confidence that my ability to swim in the shallow end would also work for me in the deep water. But my instructor knew that I could swim without any problems and therefore pushed me to go out into deeper water.

You have the PCB design job that you have now because you are a good PCB designer. It is true that you may not know every aspect of the job or be familiar with every new design technology that's out there, but you are still a skilled designer. Stand firm on that fact then and use it as a foundation to learn and grown with. Don't yield to the temptation to back down from something or give up on yourself just because you have been confronted with something new. You already are a skilled PCB designer; you just need to take the next step to grow with the new design challenges that will come your way.

John Winger, the character played by Bill Murray in the movie "Stripes" said, "We don't have to worry... all we have to do is to be the great American fighting soldier that is inside each one of us." Although that movie is a comedy, those lines hold a measure of truth. What Winger was really saying is that you shouldn't become distracted by what's in front of you. Instead, believe in who you are and what you can do, and then move forward and do it.

Am I suggesting that we shouldn't prepare, study, learn, and grow with the new design technologies that come our way? Of course not. As designers, we are all compelled to continue to grow in our design skills in order to stay on top

of our game. What I am saying is that it is easy to lose our way as if we don't keep our priorities straight. Just because you may not have a lot of experience designing boards with signal integrity and HDI requirements doesn't mean that you have suddenly become a bad designer. It just means that there are new skills awaiting you that you need to learn and add to your repertoire that will make you an even better designer.

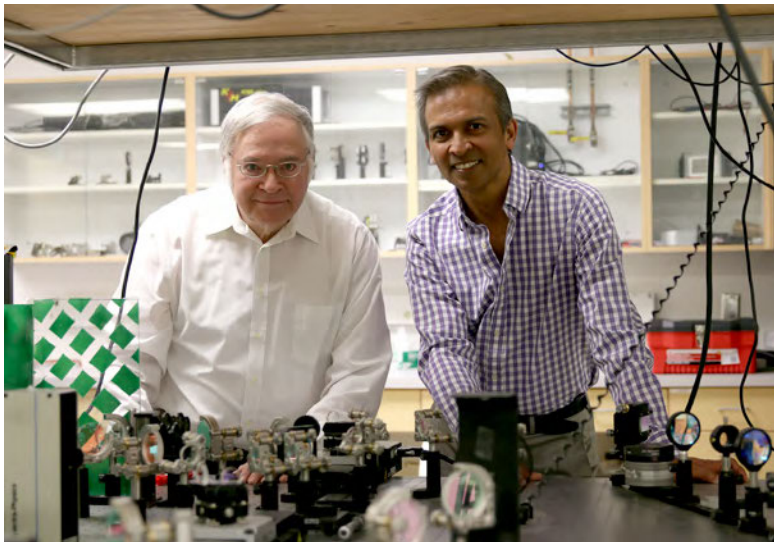
Remember; aviate, navigate, communicate, or perhaps we should rephrase that to say; "design, learn, grow." We all need to grow in our abilities, but we can't do that if we don't focus first on learning new design technologies and skills. But we won't be able to focus on learning those new design skills if we lose sight of who we are: skilled PCB designers. Just as I came close to flying into the side of a hill that day because I was focused on the wrong thing, we too can crash and burn if our priorities aren't straight.

To paraphrase John Winger; "All we have to do is to be the great PCB designer that is inside of each of us." So, never forget that you are already a skilled PCB designer and move forward with the confidence that you are the best person for the job. Also, keep your head up so that you don't fly into any hills. **PCBDESIGN**

Tim Haag is a consultant based in Portland, Oregon.

Lightning-Fast Communications

Researchers from the University of Utah's departments of electrical and computer engineering and physics and astronomy have discovered that a special kind of perovskite, a combination of an organic and inorganic compound that has the same structure as the original mineral, and can be layered on a silicon wafer to create a vital component for the communications system of the future. That system would use the terahertz spectrum, the next generation of communications bandwidth that uses light instead of electricity to shuttle data.



The new research, led by University of Utah electrical and computer engineering professor Ajay Nahata and physics and astronomy Distinguished Professor Valy Vardeny, was published in Nature Communications.

Nahata and Vardeny uncovered an important piece of that puzzle: By depositing a special form of multilayer perovskite onto a silicon wafer, they can modulate terahertz waves passing through it using a simple halogen lamp. Previous attempts to do this have usually required the use of an expensive, high-power laser.

Vardeny says what's unique about the type of perovskite they are using is that it is both an inorganic material like rock but also organic like a plastic, making it easy to deposit on silicon while also having the optical properties necessary to make this process possible.

Nahata says it's probably at least another 10 years before terahertz technology for communications and computing is used in commercial products, but this new research is a significant milestone to getting there.

HEAT TRANSFER AND THERMAL CONDUCTIVITY: THE FACTS

by Jade Bridges
ELECTROLUBE

In my first two columns in this series, I presented a broad introduction to the subject of thermal management of electronic circuits. I hope my "quick start guide" and "problems and solutions" items have sparked readers' interest in this elemental but essential aspect of electronic system design.

This month I'm taking a closer look at thermal interface materials—how they can be applied to achieve efficient heat transfer, and the significance of bulk thermal conductivity in relation to heat transfer and thermal resistance. I'll also be touching on the influence that product miniaturisation is having on thermal management techniques, and I will return to this recurring question: Why do I have to spread my thermal interface material so thinly?

As in previous columns, my approach will be based on the frequently asked questions that our customer support teams field every day on the phone, at exhibitions and when visiting customer premises. I've selected five of the most common questions, followed by their respective responses, and I hope they offer useful guidance for readers who may be experiencing design problems related to achieving a satisfactory heat transfer performance in their electronic assemblies.

First and foremost, read the thermal interface material manufacturer's advice about optimum application methods. They've been around the block a few times and they know what they're talking about! Remember, more is not necessarily better; uniform and thin applications of the heat transfer medium always work best. Most products are likely to have an optimum thickness of application, as determined by the manufacturer, and you should try to achieve this for best results.

It is important to understand your application. What are the environmental conditions under which it must operate, and how variable are they? Will the chosen heat transfer compound perform consistently as environmental conditions swing from one extreme to the other? Consider the heat sink; is this the actual casing surrounding the assembly or a separate heat sink placed on top of a component? Where cases are concerned, is there a gap between the case and the component?

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What key issues must be considered when trying to achieve efficient heat transfer?

Again, think variability of environmental conditions. Just because the heat transfer is efficient under standard ambient conditions, doesn't mean that it will remain stable over the lifetime of the product. Accelerated testing might be able to reveal related design issues; however, in-application testing is more likely to provide definitive information about the long-term performance of heat transfer materials.

Application of the heat transfer compound will depend on the type of interface or gap filling material being used. These compounds provide a medium for improving the conditions under which heat transfer takes place and thereby maximise its efficiency. Compounds should not be applied in excess amounts in the belief that they will achieve the thermal conductivity of a solid metal heat sink.

Remember, high thermal conductivity doesn't necessarily mean high heat transfer. This will depend on the thermal resistance achievable with a particular thermal compound and how effectively it can be applied in an optimally thin film.

What tips can you give about measuring bulk thermal conductivity and making effective comparisons between different thermal management products?

Bulk thermal conductivity can be measured in lots of different ways. Nowadays, the equipment available for measuring this parameter is very accurate, but the methods of measurement are likely to differ from one laboratory to another. If a true comparison of bulk thermal conductivity is required, it is advised that the same equipment and conditions are used for comparison purposes.

Bulk thermal conductivity is only the transfer of heat through the thermal management material itself. The measurement is usually taken using much greater thicknesses of the material than would be used in a real application and it will not be representative of the thermal resistance that would be expected for that application. My company always advises that thermal management products are applied in a real-world application so that the efficiency of heat transfer can be tested under the specific conditions of use.

How has the trend for product miniaturisation affected the thermal management materials market?

Product miniaturisation is increasing the need for efficient thermal management within devices. As devices get smaller, the spacing between components also gets smaller and any heat generated by these components is concentrated at specific areas of the PCB. Components that generate a lot of heat could therefore adversely affect other nearby components which, due to miniaturisation, are much closer to one another. Excessive heat can age PCBs and components, consequently shortening their lifespan. By using effective thermal management techniques, excessive heat can be dissipated, enabling densely populated designs to be realised without compromising the life expectancy of the device.

Why do the majority of thermal interface materials have to be applied in very thin layers?

A heat sink is usually made from a solid piece of metal that has a much higher bulk thermal conductivity than a thermal interface material. At a microscopic level, the interface between the component and the heat sink is likely to be uneven and air will be trapped within this space. Air is a very poor conductor of heat so an intervening thermal interface material layer is applied to remove these air pockets and therefore improve the interface's thermal conductivity.

The thermal interface material reaches optimum thickness when all the air is expelled and a uniform film is achieved, maximising the contact area of the component to the heat sink. Anything in excess of this is relying upon the thermal conductivity of the thermal interface material itself and as we know, this is nowhere near as thermally conductive as solid metal. So, the golden rule is: apply only as much as is required to remove air and improve the quality of the mating surfaces; that way you will achieve the most efficient heat transfer between a component and its heat sink.

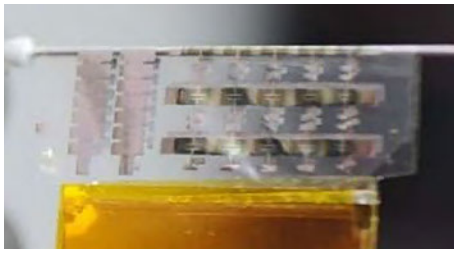
As always, I strongly recommend you get some expert advice before you settle on any particular material or processing method. **PCBDESIGN**

Jade Bridges is the European technical support specialist for Electrolube.

Highly Flexible Organic Flash Memory for Foldable and Disposable Electronics

A KAIST team reported ultra-flexible organic flash memory that is bendable down to a radius of 300μm. A joint research team led by Professor Seunghyup Yoo of the School of Electrical Engineering and Professor Sung Gap Im of the Department of Chemical and Biomolecular Engineering said that their memory technology can be applied to non-conventional substrates, such as plastics and papers, to demonstrate its feasibility over a wide range of applications.

Flash memory is a non-volatile, transistor-based data-storage device that has become essential in most electronic systems in daily life. With straightforward operation and easy integration into NAND or NOR array architecture, flash memory is the most successful and dominant non-volatile memory technology by far.



The solution processing used for the preparation of most of the polymeric dielectric layers also makes it difficult to use them in flash memory due to the complexity involved in the formation of the bilayer dielectric structure, which is the key to flash memory operations.

The research team tried to overcome these hurdles and realize highly flexible flash memory by employing thin polymeric insulators grown with initiated chemical vapor deposition (iCVD), a vapor-phase growth technique for polymers that was previously shown to be promising for the fabrication of flexible TFTs.

The KAIST team produced flash memory with programming voltages around 10 V and a projected data retention time of over 10 years, while maintaining its memory performance even at a mechanical strain of 2.8%. This is a significant improvement over the existing inorganic insulation layer-based flash memory that allowed only a 1% strain.

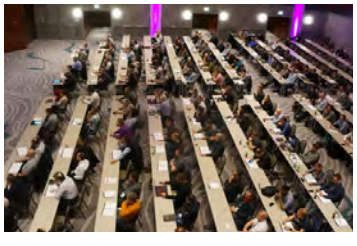
TOP TEN

Recent Highlights from PCBDesign007

1 Mentor Announces 27th Annual PCB Technology Leadership Awards Winners

Mentor has announced its 27th annual printed circuit board (PCB) Technology Leadership Awards. Started in 1988, this program is the longest running competition of its kind in the EDA industry. It recognizes engineers and designers who use innovative methods and design tools to address today's complex PCB systems design challenges and produce industry-leading products.

2 AltiumLive 2017 Munich: Sold Out!



I recently sat down with Ted Pawela, Lawrence Romine, and Judy Warner of Altium to wrap up their sold-out AltiumLive 2017 PCB Design Summit in Munich, Germany. We discussed some of the highlights of the show, including designers' reactions to a new version of Altium Designer 18 and the brand-new Altium Nexus tool.

3 Happy Holden and Charles Pfeil Discuss the Past and Future of PCB Design, Part 1

When it comes to the PCB design community and the challenges facing it, as well as where design has been and where it's heading, there aren't many people as qualified to speak on the topic as industry veterans Happy Holden and Charles Pfeil. Joined by I-Connect007's Barry Matties at the recent AltiumLive 2017 event in San Diego, the three sat down for a discussion about the current state of PCB design, what the future holds, and what it means to be a designer.

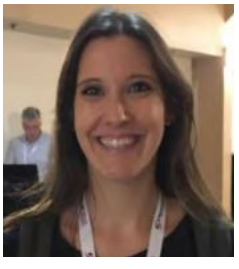
4 Cadence Reports Revenue Growth in Q3 2017

Cadence reported third quarter 2017 revenue of $485 million, compared to revenue of $446 million reported for the same period in 2016. On a GAAP basis, Cadence recognized net income of $81 million in the third quarter of 2017, compared to net income of $65 million for the same period in 2016.

5 Insulectro Teams with Isola to Address Signal Integrity Needs

Insulectro and Isola recently shared a combined booth during PCB West 2017. Insulectro has distributed Isola materials for years, and the companies wanted to focus on Isola's line-up of high-speed, low-loss material sets. Insulectro's Chris Hunrath, VP of Technology, and Norm Berry, Director of Laminates and OEM Marketing, sat down with me to discuss the challenges facing signal integrity engineers today, and some of the Isola low-loss, low-Dk materials that can help with signal integrity.

6 Sunstone Integrates SnapEDA Libraries into PCB123



Sunstone Circuits and SnapEDA recently announced that SnapEDA's parts library would be integrated into Sunstone's PCB123 design tool. During PCB West, I interviewed EDA Product Manager Nolan Johnson of Sunstone Circuits and SnapEDA President Natasha Baker. We discussed their new partnership, the changing parts library landscape, and where the companies see this alliance heading in the future.

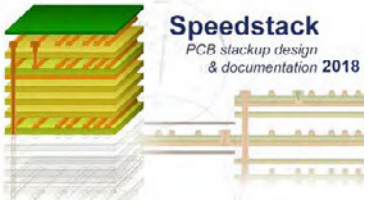
7 Beyond Design: Plane Cavity Resonance

When return current flows through the impedance of a cavity, between two planes, it generates voltage. Although quite small (typically in the order of 5mV) the accumulated noise from simultaneous switching devices can become significant. And unfortunately, as core voltages drop, noise margins become tighter. In this column, I will cover plane cavity resonance and look at how it impacts electromagnetic radiation.

8 Carl Schattke: I Started Designing Boards When I Was 12

Growing up with a father who owned a PCB design bureau, Carl Schattke, CID+, may have been predestined to design circuit boards for a living. In fact, he's been designing boards for nearly his entire life. Carl gave a keynote speech at the recent AltiumLive event in San Diego, where I caught up with him to discuss a lifetime spent in PCB design.

9 Polar Speedstack Si Integrates Insertion Loss Field Solver; To Exhibit at productronica



Polar Instruments, a specialist provider of tools for PCB design, fabrication and test, announces a major enhancement for Speedstack Si at productronica. Speedstack Si 2018 edition now contains an integrated insertion loss field solver, which lets the user both design and add comprehensive insertion loss graphs and stackup specification into Speedstack's professional report engine.

10 SiSoft Preparing for DDR5 Simulation Next Year

DDR5 is expected to double the memory bandwidth and density of DDR4. I recently spoke with SiSoft CTO Walter Katz about his company's efforts to hit the market with this game-changing technology in 2018.

PCBDesign007.com for the latest circuit design news and information—anywhere, anytime.

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For just $500, your 200 word, full-column—or, for $250, your 100 word, half-column—ad will appear in the Help Wanted section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs and suppliers.

Potential candidates can click on your ad and submit a résumé directly to the email address you've provided. If you wish to continue beyond the first month, the price is the same per month. No contract required. We even include your logo in the ad, which is great branding!

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Barb Hockaday at barb@iconnect007.com or +1.916.608.0660 (-7 GMT)

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SMT007 pcb007 pcb design007

SALESPERSON WANTED · MAINLAND SOUTH CHINA

Work where you live!

The I-Connect007 China team is seeking an experienced salesperson to generate and manage a revenue stream for our Chinese publications.

Key Responsibilities include:

- Sell advertising contracts for monthly magazine
- Develop and cultivate new business
- Keep timely and accurate records
- Generate and follow up on all leads
- Manage contract renewals
- Account management: work with local and international team to provide customer support
- Phone and email communications with prospects
- Occasional travel

Qualifications

Successful candidates should possess a university degree or equivalent, experience with managing and cultivating leads, projecting, tracking and reporting revenue. We are looking for positive, high-energy candidates who work well in a self-managed, team-based, virtual environment.

Compensation

This is a base salary-plus-commission position. Compensation commensurate with experience.

Requirements

- Must be located in China Mainland, South China area preferred
- Good command of Chinese language, proficient with English speaking and writing
- Able to follow established systems and learn quickly
- Able to maintain professional external and internal relationships reflecting the company's core values
- 2-5 years' sales experience
- Experience with Microsoft Office products
- Must be highly motivated and target-driven with a proven track record for meeting quotas
- Good prioritizing, time management and organizational skills
- Create and deliver proposals tailored to each prospect's needs
- Experience in the electronics industry desirable

QUALIFIED CANDIDATES: CLICK HERE TO APPLY

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ACE
ACCURATE
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ENGINEERING

PCB Assembly Supervisor—full time
Accurate Circuit Engineering—Santa Ana, CA

Position Summary: Responsible for all assembly processes to ensure continued growth as directed by management.

Essential Job Functions:
- Create, implement, and supervise in-house manufacturing facility
- Recruit, hire, train, and supervise assembly floor personnel
- Extensive hands on experience with all aspects of PCB assembly
- Understanding of IPC-A-610 standards
- Research and acquire additional assembly resources
- Gather data on product shortages, lead times, price changes, etc.
- Coordinate the assembly activities with sales to ensure 100% on-time delivery
- Create, implement, and supervise daily quality processes to ensure 100% accuracy
- Document, monitor and review progress of the business unit
- Respond to internal and external customers in a timely manner
- Coordinate walk-through, site audits, etc.

Qualifications:
- Minimum 3 years as operations supervisor of electronics assembly house
- 5+ years' experience in the electronics industry
- Previous experience as a quality or operations supervisor preferred
- Ability to solve practical problems using pre-established guidelines
- Strong facility in Microsoft Office applications
- Excellent verbal and written communication skills
- Ability to work with people of diverse backgrounds
- Highly organized/excellent time management skills
- Ability to perform at the highest level in a fast-paced environment
- Valid California driver's license.

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ENGINEERING

PCB Process Planner

Accurate Circuit Engineering (ACE) is an ISO 9001:2000 certified manufacturer of high-quality PCB prototypes and low-volume production for companies who demand the highest quality in the shortest time possible. ACE is seeking a skilled individual to join our team as a PCB process planner.

Responsibilities will include:
- Planning job travelers based on job release, customer purchasing order, drawings and data files and file upon completion
- Contacting customer for any discrepancies found in data during planning and CAM stage
- Consulting with director of engineering regarding technical difficulties raised by particular jobs
- Informing production manager of special material requirements and quick-turn scheduling
- Generating job material requirement slip and verify with shear clerk materials availability
- Maintaining and updating customer revisions of specifications, drawings, etc.
- Acting as point of contact for customer technical inquiries

Candidate should have knowledge of PCB specifications and fabrication techniques. They should also possess good communication and interpersonal skills for interfacing with customers. Math and technical skills are a must as well as the ability to use office equipment including computers, printers, scanners, etc.

This position requires 3 years of experience in PCB planning and a high school level or higher education.

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騰輝電子

Ventec Seeking U.S. Product Manager for tec-speed

Want to work for a globally successful and growing company and help drive that success? As a U.S.-based member of the product and sales team, your focus will be on Ventec's signal integrity materials, tec-speed, one of the most comprehensive range of products in high-speed/low-loss PCB material technology for high reliability and high-speed computing and storage applications. Combining your strong technical PCB manufacturing and design knowledge with commercial acumen, you will offer North American customers (OEMs, buyers, designers, reliability engineers and the people that liaise directly with the PCB manufacturers) advice and solutions for optimum performance, quality and cost.

Skills and abilities required:

- Technical background in PCB manufacturing/ design
- Solid understanding of signal integrity solutions
- Direct sales knowledge and skills
- Excellent oral and written communication skills in English
- Experience in making compelling presentations to small and large audiences
- Proven relationship building skills with partners and virtual teams

This is a fantastic opportunity to become part of a leading brand and team, with excellent benefits.

Please forward your resume to
jpattie@ventec-usa.com and mention
"U.S. Sales Manager—tec-speed"
in the subject line.

www.venteclaminates.com

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ARLON

Arlon EMD, located in Rancho Cucamonga, California is currently interviewing candidates for **manufacturing** and **management positions.** All interested candidates should contact Arlon's HR department at 909-987-9533 or fax resumes to 866-812-5847.

Arlon is a major manufacturer of specialty high performance laminate and prepreg materials for use in a wide variety of PCB (printed circuit board) applications. Arlon specializes in thermoset resin technology including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, high density interconnect (HDI) and microvia PCBs (i.e., in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2008 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customer's requirements.

more details

Altium

Application Engineer

The application engineer is the first contact for our customers who have technical questions or issues with our product. We value our customers and wish to provide them with highest quality of technical support.

Key Responsibilities:

- Support customer base through a variety of mediums
- Log, troubleshoot, and provide overall escalation management and technical solutions
- Create various types of topic based content, such as online help, online user guides, video tutorials, knowledge base articles, quick start guides and more
- Distill complex technical information into actionable knowledge that users can understand and apply
- Continually develop and maintain product knowledge

Requirements:

- Understanding of EDA electronic design software, schematic capture and PCB layout software
- Bachelor's degree in electronics engineering or equivalent experience
- Sales engineering and/or support engineering experience
- Circuit simulation and/or signal integrity experience
- Understanding of ECAD/ MCAD market segments
- Understanding of micro controllers, SoC architecture and embedded systems market
- Database experience preferred (i.e., MySQL, PostgreSQL, Microsoft Access, SQL, Server, FileMaker, Oracle, Sybase, dBASE, Clipper, FoxPro) etc.
- Experience with PLM/PDM/MRP/ERP software (Program Lifecycle Management) preferred
- Salesforce experience a plus

Salary based upon experience. Comprehensive benefits package and 401k plan. Openings in USA, UK, and Germany.

For more information, contact Altium.

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CHEMCUT

BOUNDLESS INNOVATION | UNBEATABLE PRECISION

Field Service Technician

Chemcut, a leading manufacturer of wet-processing equipment for the manufacture of printed circuit boards for more than 60 years, is seeking a high-quality field service technician. This position will require extensive travel, including overseas.

Job responsibilities include:

- Installing and testing Chemcut equipment at the customer's location
- Training customers for proper operation and maintenance
- Providing technical support for problems by diagnosing and repairing mechanical and electrical malfunctions
- Filling out and submitting service call paperwork completely, accurately and in a timely fashion
- Preparing quotes to modify, rebuild, and/or repair Chemcut equipment

Requirements:

- Associates degree or trade school degree, or four years equivalent HVAC/industrial equipment technical experience
- Strong mechanical aptitude and electrical knowledge, along with the ability to troubleshoot PLC control
- Experience with single and three-phase power, low-voltage control circuits and knowledge of AC and DC drives are desirable extra skills

To apply for this position, please apply to Mike Burke, or call 814-272-2800.

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Do you have what it takes?

MacDermid Performance Solutions, a Platform Specialty Products Company, and daughter companies manufacture a broad range of specialty chemicals and materials which are used in multi-step technological processes that enhance the products people use every day. Our innovative materials and processes are creating more opportunities and efficiencies for companies across key industries – including electronics, graphic arts, metal & plastic plating, and offshore oil production. Driving sustainable success for companies around the world, and at every step of the supply chain, takes talent. Strategic thinking. Collaboration. Execution.

The people of MacDermid Performance Solutions stand united by a guiding principle: If it doesn't add value, don't do it. This belief inspires a unique culture where each team member has opportunities to imagine, create, hone and optimize. Do you have what it takes? Join our growing team of over 4,000 professionals across more than 50 countries with openings in research, finance, customer service, production and more.

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311 Turquoise Street Milpitas, CA 95035 (Phone) 408-945-8787

SALES ACCOUNT MANAGER

This is a direct sales position responsible for creating and growing a base of customers. The account manager is in charge of finding and qualifying customers while promoting Lenthor's capabilities to the customer through telephone calls, customer visits and use of electronic communications. Experience with military and medical PWB/PWA a definite plus. Each account manager is responsible for meeting a dollar level of sales per month and is compensated with salary and a sales commission plan.

Duties include:

- Marketing research to identify target customers
- Initial customer contact (cold calling)
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Quantity and delivery requirements
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Bonding
- Submitting quotes and sales orders
- Providing ongoing service to the customer
- Problem solving
- Developing customer information profiles
- Developing long-term customer strategies to increase business
- Participate in quality/production meetings
- Assist in customer quality surveys
- Knowledgeably respond to non-routine or critical conditions and situations

Competitive salaries based on experience, comprehensive health benefits package and 401(k) Plan.

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NCAB GROUP
Integrated PCB Production

Outside Sales/ Key Account Managers

NCAB Group USA is adding to our existing outside sales team in various U.S. locations:

- Ontario, California
- Itasca, Illinois
- Vancouver, Washington

This is a sales position that requires the ability to convert those cold calls into high-value customer meetings. What we are looking for:

- A "hunter" mentality
- The ability to create solid customer relationships
- A desire to excel and not settle for mediocrity
- 5+ years of experience in the PCB or semiconductor industry
- An excellent ability to present a product and do the "deep dive" during customer visits by asking open ended questions and identifying customer pain points
- The energy to move from prospecting to cold calls to getting the win
- Knowledge of "SPIN" selling
- A college degree
- Willingness to travel, domestically and globally
- U.S. citizens with a valid U.S. passport

Interested? Send your resume.

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Visit us at www.NCABGroup.com

INDIUM®

Technical Content Specialist

Indium Corporation is seeking a technical content specialist to guide the development of data-rich, high-level content for the company's semiconductor and advanced assembly materials (SAAM) sales and technical literature. The technical content specialist will work with multiple departments to ensure that all externally-facing technical and sales collateral and internal training materials are consistent in format and of superior quality.

The technical content specialist will:

- Assist in the development of key content and ensure consistency of message and format across platforms
- Develop a technically-detailed understanding of Indium Corporation materials and offerings to the SAAM industry
- Curate a library of technical conference papers and associated materials, including content related to Indium Corporation materials and their performance
- Assist in the development of, and ensure consistency for SAAM promotional materials, such as product datasheets (PDS), images, brochures, whitepapers and presentations (technical and sales)
- Attend at least one technical conference and its paper session per year

Requirements:

- Technical undergraduate degree (BS in Chemistry/Physics/Metallurgy/Materials Science or Engineering discipline)
- 5 years of work experience in semiconductor assembly or advanced electronics assembly
- Excellent written and spoken English language skills; fluency in Chinese desirable
- Proven ability to work independently with verbal or written instructions

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TECHNICA, U.S.A.
Fulfilling Manufacturing Needs
Throughout the Electronics Industry

Southern California Territory Sales Engineer

Technica, USA, a Western regional manufacturer's representative/distributor, has an open sales position for our Southern California territory. The position will be responsible for selling and servicing our entire product line within the specified territory to the PCB manufacturing industry.

This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Required Skills:

- BA/BS degree-desired, in a technical area is preferred
- Two years of outside/inside sales or manufacturing experience in the PCB manufacturing environment is desired
- Self-motivated self-starter with the ability to initiate and drive business with little supervision
- Independent worker with a strong commitment to customer satisfaction
- Understanding of consumable sales process
- Ability to organize activities and handle multiple projects simultaneously with effective and timely follow-up
- Ability to solve problems and make decisions for which there are no precedents or guidelines and be resourceful in nature
- Positive attitude while operating under pressure and be an independent problem-solver
- Computer skills in Windows, Outlook, Excel, Word and PowerPoint
- Must have a valid driver's license with good driving record

Please send resume.

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TECHNICA, U.S.A.
Fulfilling Manufacturing Needs
Throughout the Electronics Industry

Western Regional Equipment Service Technician

Technica, USA, a Western regional manufacturer's representative/distributor has an opening for an equipment service technician covering the Western USA, including but not limited to, California, Oregon, Washington, Utah, Colorado, and Arizona. The position will be responsible for servicing our PCB fabrication equipment product line, including installation, troubleshooting, repair service, rebuild service, etc. This position requires a highly self-motivated, hands on, confident individual of the highest integrity.

Key responsibilities are to install and service equipment, conduct equipment audit, and provide technical service when appropriate to solve problems.

Required Skills:

- 2+ years of experience in a PCB manufacturing environment or similar
- Willingness to travel
- Positive "whatever it takes" attitude while operating under pressure
- Self-motivated self-starter with the ability to initiate action plans
- Ability to work independently with a strong commitment to customer satisfaction
- Excellent communication and interpersonal skills
- Strong ability to use all resources available to find solutions
- Computer skills with ability to write detailed service and equipment reports in Word
- Understanding of electrical schematics
- Able to work in and around equipment, chemical, and environmental conditions within a PCB manufacturing facility

Please send resume.

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BLACKFOX
Premier Training & Certification

IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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Prototron Circuits

Experienced PCB Sales Professional

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. Prototron of Redmond, Washington, and Tucson, Arizona are looking for an experienced sales professional to handle their upper Midwest Region. This is a direct position replacing the current salesperson who is retiring after spending ten years with the company establishing this territory.

The right person will be responsible for all sales efforts in this territory including prospecting, lead generation, acquiring new customers, retention, and growth of current customers.

This is an excellent opportunity for the right candidate. Very competitive compensation and benefits package available.

For more information, please contact Russ Adams at 425-823-7000, or email your resume.

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Process Engineer (Redmond, Washington)

With more than 30 years of experience, Prototron Circuits is an industry leader in the fabrication of high-technology, quick-turn printed circuits boards. We are looking for an experienced PCB process engineer to join the team in our Redmond, Washington facility. Our current customer base is made up of forward-thinking companies that are making products that will change the world, and we need the right person to help us make a difference and bring these products to life. If you are passionate about technology and the future and believe you have the skills to fulfill this position, please contact Kirk Williams at 425-823-7000 or email your resume.

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Electronics Expert Engineer

Orbotech is looking for an Electronics Expert Engineer to handle various hardware activities, including communication, data path processing, device interfaces and motion, as well as system supporting functions in a multi-disciplinary environment.

What Will Your Job Look Like?

- Providing cutting edge hardware solutions for challenging product line needs
- Developing board design and Logic in VHDL
- Defining and managing interfaces (software, algorithm, mechanics and electricity)
- Successfully integrating hardware with other product disciplines
- Supporting the product needs during and following release

What Do You Need to Succeed?

- BSc in electronics engineering
- At least 5 years of R&D experience in complex board design, mainly FPGA (communication interfaces, DDR controller, algorithm implementation)
- Experience in an Altera/Xilinx development environment
- Experience in ECAD design tools (DxDsigner, ModelSim) is an advantage
- Knowledge in laser interfaces, RF and analog is an advantage

Who We Are

Virtually every electronic device in the world is produced using Orbotech systems. For over 30 years, Orbotech has been a market leader in developing cutting edge inspection, test, repair, and production solutions for the manufacture of the world's most sophisticated consumer and industrial electronics.

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Electronics Team Leader

Orbotech is seeking an Electronics Team Leader to join our electronics team, which develops multi-disciplinary systems, including vision/laser, image processing, and control and automation missions.

What Will Your Job Look Like?

- Lead a team of electronics engineers in a multi-disciplinary environment
- Lead electronic activities from requirement phase to development, integration and transfer, to production
- Be the focal point for other disciplines and projects managers
- Maintain and improve existing electronics platforms

What Do You Need to Succeed?

- BSc/MSc in electronic engineering/ computer science from a well-recognized university
- 5+ years' experience in digital board design, high-speed links, computing embedded systems, and HW/SW integration
- 2-3 years' experience in leading a team of engineers
- Solid skills in complex FPGA design with multi-modules
- Solid skills in high-speed board design, DDR3/4, PCIE, USB, IO, and optic links
- Ability to design and execute end-to-end solutions

Who We Are

Virtually every electronic device in the world is produced using Orbotech systems. For over 30 years, Orbotech has been a market leader in developing cutting-edge inspection, test, repair, and production solutions for the manufacture of the world's most sophisticated consumer and industrial electronics.

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FPGA Design Expert

Orbotech is seeking a FPGA Design Expert to join our electronics team, which develops multi-disciplinary systems including vision/laser, image processing and electro-optics.

What Will Your Job Look Like?
- Lead image acquisition and processing activities in the team
- Engage in all aspects of FPGA design activity: requirement phase, coding, synthesizing, verification support and LAB bring up
- Participate in system definitions for current and next generation products
- Collaborate with other teams: SW, algorithm and QA

What Do You Need to Succeed?
- BSc/MSc in Electrical Engineering from a well-recognized university
- Extensive knowledge of VHDL
- 5+ years of FPGA development experience (requirement, architecture, RTL coding, simulation, synthesis, timing analysis, P&R, board level integration and verification)
- Experience in designing and implementing low-latency, high-throughput FPGA designs utilizing PCIe Gen2/3, Gigabit Ethernet, SERDES, DDR3/4
- Experience in complex FPGA such as Altera Stratix-II and Arria 5&10 devices
- Authoring documentation experience such as FPGA specifications and FPGA verification plans

Who We Are
Virtually every electronic device in the world is produced using Orbotech systems. For over 30 years, Orbotech has been a market leader in developing cutting-edge inspection, test, repair, and production solutions for the manufacture of the world's most sophisticated consumer and industrial electronics.

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CHEMCUT
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Chemical Process Engineer

Chemcut, a leading manufacturer of wet-processing equipment for the manufacture of printed circuit boards for more than 60 years, is seeking a Chemical Process Engineer. This position is located at Chemcut's main facility in State College, Pennsylvania. Applicants should have an associate degree or trade school degree, or 4 years equivalent in chemical process engineering.

Job Responsibilities Include:
- Developing new industrial processes
- Providing process criteria for both new equipment and modifying existing equipment
- Testing new processes and equipment
- Collecting data required to make improvements and modifications
- Assisting in investigating and trouble-shooting customer process problems
- Ensuring that equipment works to its specification and to appropriate capacities
- Assessing safety and environmental issues
- Coordinating with installation/project engineers
- Ensuring safe working conditions and compliance with health and safety legislation

Key Skills:
- Aptitude for, and interest in chemistry, IT and numeracy
- Analytical thinking
- Commercial awareness
- Ability to perform under pressure
- Communication and teamwork
- Problem-solving

Experience with circuit board processes is a plus.

Contact Arlene at 814-272-2800 or by clicking below.

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“This micro eBook should be required reading for every PCB designer or design engineer, whether novice or veteran.”

Andy Shaughnessy
Managing Editor, The PCB Design Magazine

In this second micro eBook from Mentor, A Siemens Business, written by signal integrity engineer, Fadi Deek, provides a thorough investigation of power distribution network performance and will help PCB designers and engineers of all experience levels make better design decisions.

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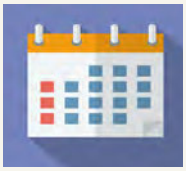

IPC Calendar of Events, click here

SMTA Calendar of Events, click here

PCB Design Calendar of Events, click here

productronica 2017
(IPC Committee meetings held in conjunction with productronica)
November 14–17, 2017
Munich, Germany

HKPCA/IPC International Printed Circuit & South China Fair
December 6–8, 2017
Shenzhen, China

47th NEPCON JAPAN
January 17–19, 2018
Tokyo Big Sight, Japan

DesignCon 2017
January 30–February 1, 2018
Santa Clara, California, USA

EIPC 2018 Winter Conference
February 1–2, 2018
Lyon, France

MD&M West
February 6–8
Anaheim, California, USA

IPC APEX EXPO 2018 Conference and Exhibition
February 27–March 1, 2018
San Diego, California, USA

China International PCB and Assembly Show (CPCA)
March 20–22, 2018
Shanghai, China

KPCA Show 2018
April 24–26, 2018
Kintex, South Korea

Thailand PCB Expo 2017
May 10–12, 2017
Bangkok, Thailand

Medical Electronics Symposium 2018
May 16–18, 2018
Dallas, Texas, USA

JPCA show 2018
June 6–8, 2017
Tokyo, Japan

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