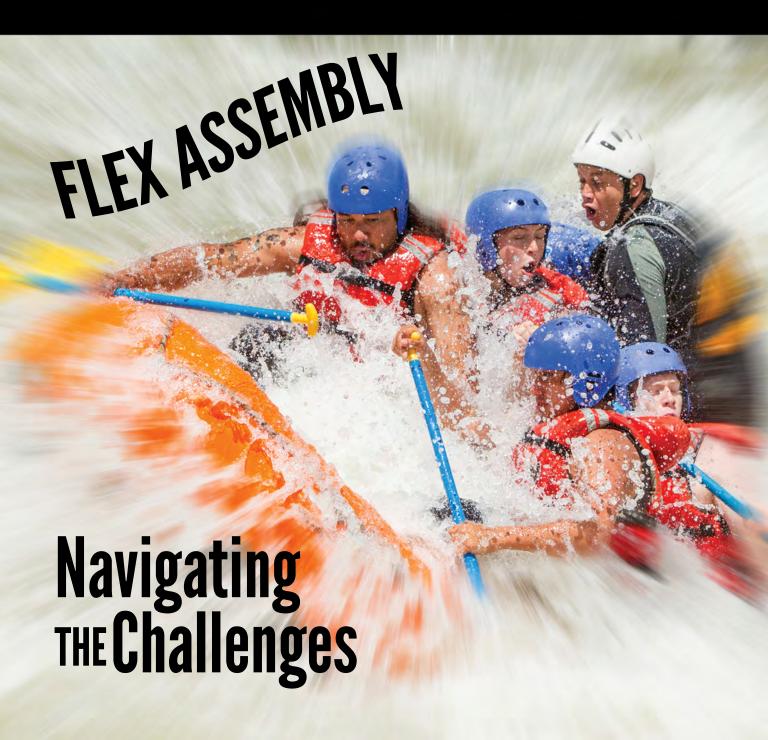
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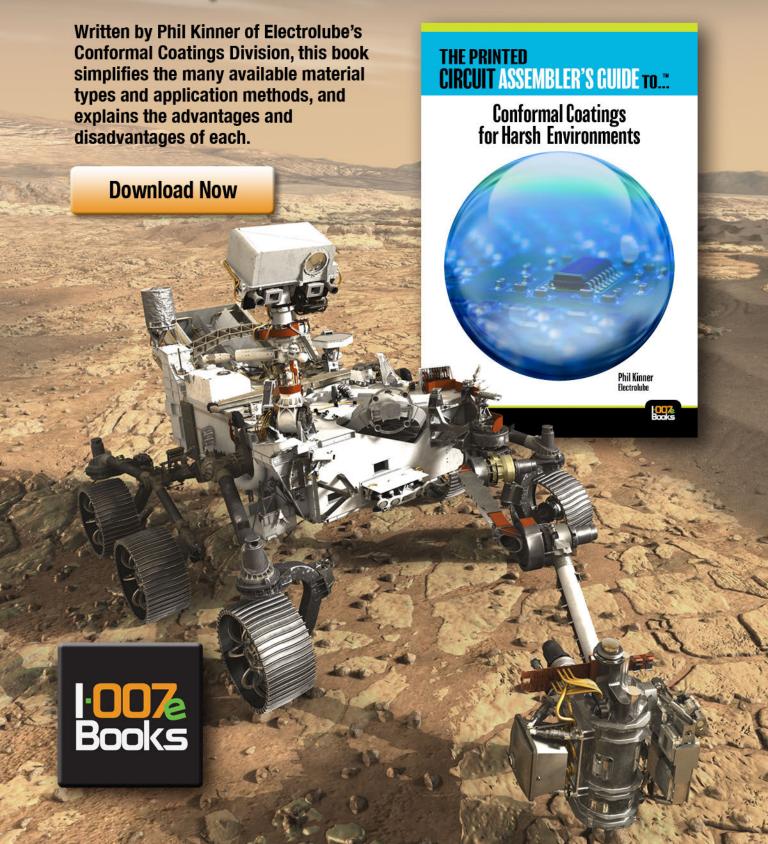
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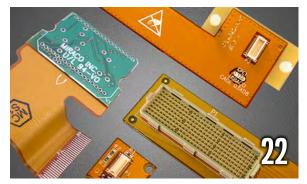
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Flex Circuit Assembly

Manufacturers are having to navigate critical challenges that rock their boat when faced with assembling flexible printed circuits. The flex market continues to be one of the fastest growing segments of the circuit board industry, mainly driven by the significant rise in the consumer electronics sector. In this issue, we examine these concerns and highlight some of the strategies and techniques used to address them.

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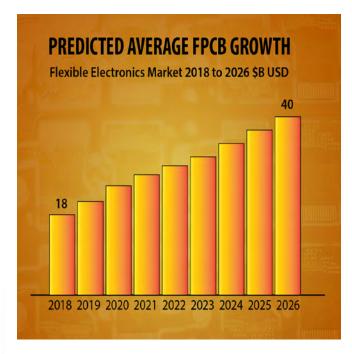
Tackling the Challenges in Flex Assembly

Editor's Note by Stephen Las Marias, I-CONNECT007

We recently released the inaugural issue of *Flex007 Magazine*, which is dedicated to flex system designers, electrical engineers, flex PCB designers, and anyone responsible for integrating flex into their products at the OEM/CEM level. (If you haven't seen the first issue yet, which features some of the top flex experts sharing thoughts about flex, rigid-flex, and the flex market, click here.)

As my colleague and *Flex007* Managing Editor Andy Shaughnessy wrote, it was time to expand our *Flex007 Weekly Newsletter* into a magazine after seven years due to the increas-





ing use of flex circuits in many electronics applications.

Indeed, the flex printed circuit market continues to be one of the fastest-growing segments of the PCB industry. According to a report by industry analysts Transparency Market Research (TMR), the global market for flexible printed circuits is expected to expand at a CAGR of 11.8% to reach a value of \$38.27 billion by 2026, up from about \$14.51 billion in 2017. Mainly driving this growth is the significant rise in the consumer electronics industry, led by the growing demand for smartphones, tablets, and LCD displays. Meanwhile, multilayer flex circuits are enjoying a greater demand among products in this sector, and this trend is projected to remain so over the next few years, according to TMR.



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While we were planning the launch of *Flex007*, one of the flex experts we spoke with mentioned that apart from the design and manufacturing of flex printed circuits, a critical challenge that needs attention is assembly. Their flexible nature requires specific strategies for paste printing, chip mounting, soldering—whether reflow, wave, or hand—and rework/repair

processes. And this brings me to the June issue of *SMT007 Magazine*.

This month, we investigate the many challenges in flex circuit assembly and highlight some of the strategies, techniques and best practices to help assemblers deal with flex circuit issues.

First, we feature an experts' discussion with Lenthor Engineering's David Moody and Matt Kan, as well as BEST Inc.'s Bob Wettermann, who offer their wide-ranging views on flex and rigid-flex circuits. Among the issues highlighted are materials, paste printing, depan-

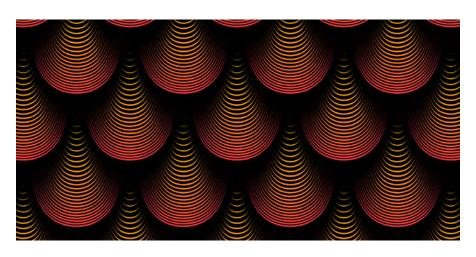


Steven Fang

elization, and moisture, and ways to address those challenges—including upfront engagement between designers and assemblers.

Meanwhile, at the recent NEPCON China 2018 event in Shanghai, I spoke to Steven Fang, director of sales for Asia at OK International,

who shared the challenges he sees in flex circuit assembly. Fang notes that soldering is critical, given that flex circuits may easily be damaged when subjected to extreme temperatures during soldering and rework. Among other things, Fang believes that operators need smarter hand soldering systems, which would help them recognize whether the solder joints are good or not.



At NEPCON, I also interviewed Ralf Wagenfuehr of Rehm Thermal Systems, to get his unique insights on the topic of flex assembly challenges, from the perspective of a reflow oven technology supplier.

Michael Gouldsmith and Zen Lee, both with Themaltronics, provide their views from a hand soldering technology standpoint in a short article.

This month, we are also featuring an interview with Jason Michaud of Miraco, and Harry Chan of Vexos Corp.

In our columns department, Michael Ford discusses digitalization and the use of Internet of Things (IoT) in the manufacturing environment, and IPC's John Mitchell examines the manufacturing industry skills gap, and how his organization is helping bridge that gap through training and education.

Finally, we have a couple of technical articles that highlight microflux coated solder preforms as a novel approach to void reduction and evaluate the impact of solder alloy powder size and stencil technology on the transfer efficiency of solder pastes.

I hope you enjoy this issue of *SMT007 Magazine*. In next month's issue, we'll feature best practices in PCB assembly. Watch out for it. **SMT007**



Stephen Las Marias is managing editor of SMT007 Magazine. He has been a technology editor for more than 14 years covering electronics, components, and industrial automation systems.



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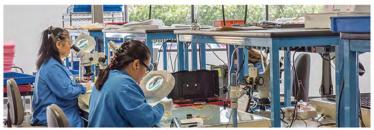




FLEX CIRCUIT ASSEMBLY:

Challenges and Strategies for Success







Feature by Stephen Las Marias I-CONNECTO07

The continuing trend towards miniaturization and the increasing functionality in smaller and smaller devices are the primary drivers for the growth of the flexible printed circuit market. Everything is getting smaller, faster, and more complex. The segments that have consistently driven it are more on the consumer side, such as mobile phones and smart electronics. On the industrial side, contributing markets include medical—portable medical electronics, diagnostic electronics—and military/defense.

Of course, dealing with flex circuits during assembly is very different from rigid PCBs. And among the key challenges here are the material itself, and the word "flexible," according to David Moody, director of sales and marketing at Lenthor Engineering: "Flexible circuits are flexible; they aren't flat, they aren't rigid, and they conform to a shape. The other portion of it is the three-dimensionality of a flex circuit; you're trying to do circuit mount

assembly with small components, BGAs, and working on substrates' flex circuits that often have different plane levels. There are higher portions on the circuit, so evening things out is really the challenge to getting the nice, flat, secure surface to mount the components on."

Lenthor has been in the flex and rigid-flex fabrication business for 35 years. It brought in-house flex and rigid-flex assembly 10 years ago as a value-add for its customers. Moody notes that it had been difficult for them and their customers at the time to find people in the assembly business that had a proficiency in flex circuit assembly, because there are some peculiarities regarding flex circuitry that you don't find in rigid board assembly. "Being able to bring that in-house, we've been able to advance that portion of our offering to the customers."

Dealing with flex circuit assembly, Lenthor does a good mixture of hand assembly and automated assembly. "Flex circuits themselves generally have a combination of some hand assembly, and automated, surface-mount line,

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reflow, and pick and place," explains Moody. "Rigid-flex design typically replicates rigid-board assembly, because most of the functionality on a rigid-flex board is all centered in the rigid area. The flex area of a rigid-flex is usually the interconnect between the flex areas. So, it becomes a little less problematic; but flex circuits themselves do lend themselves far more to the multiple process environment."

Lenthor found flex circuit assembly challenging initially. "Luckily for us, we hired a really good engineer who's been able to design a lot of the fixturing that we use, and that's what really makes us succeed in assembly," says Moody. "In the beginning it was difficult, there was far more rework than we have today. But the techniques, the equipment that we've got now, have really lent themselves to an assembly that's predictable. We get a very good first yield rate. I would guess it's 96-97% in the first pass yield. It wasn't that way 10 years ago."

Indeed, when dealing with flex circuits, the overarching theme to ensure successful assembly is proper fixturing.

According to Bob Wettermann, principal of BEST Inc., an electronics rework/repair and PCB assembly firm, "In the rigid world, you have a coplanar surface and components with known fixed dimensions, and so the pick and place machine knows exactly how and where to place the device. It's always a planar surface. Now, you add the three dimensionality as well as the lack of rigidity of the surface and it becomes very difficult to place micro components on essentially a noodle."

"Fixturing is key to tackling this problem. Having a good coplanar surface to remove and replace devices is key to reworking complex devices on flex circuitry. In terms of physical repair, such as IPC-7721-related type of physical repairs, there just aren't any standards for flex materials. You have to make the process up as you go along. The other day, a client sent us a case where we were refereeing the acceptability criteria

for the solder joints of an SOIC placed onto a flex circuit. We were dealing with an epoxy attachment to flex. And guess what? There are no industry acceptability criteria. So, it's still a little bit of the Wild West, I would call it, in terms of standards, knowledge and practices. You make it up as you go along."

Throw it Over the Wall

In our conversations with industry experts, they always mention a critical factor to success when it comes to design, fabrication, or assembly—communication along the supply chain. Because most often than not, the industry continues to have a 'throw it over the wall' mentality.

This case is no different. "It's just because of the kind of business that we are in in terms of assembly—we're the prototyping guys, so our job is to get the customer functional units so they can go to round two or round three," says Wettermann. "Generally, the boards are not ending up in end customers' hands. Our job is to get functional units."

Moody echoes what Wettermann is saying. "In the prototype stage, a lot of customers are just simply looking to get some functionality out of the initial product, and they just want you to go figure it out. On the other hand, because we do get into some production stuff with our customers, and it's still interesting to me that when we begin the conversation, and we begin in sometimes even at the design stage, the assembly aspect of the build is still not being considered until it's almost necessary. No matter how much you try to drive the conversation in the beginning, I don't know why, but there is still some reluctance to concentrate on what the assembly is going to

look like or how you're going to be able to fulfill it. Engineers come in with an idea; it's a conglomeration of a mechanical guy, and an electrical guy, and somebody else sitting down there trying to figure out what they want, and they've already selected the components, and now what to back-fill the design to meet the component requirement. And there are occa-

sions when a component's been chosen that just is going to end up being problematic for the design that they're doing at the assembly aspect. It's hard to talk them out of that, so in general, I don't think there's enough emphasis being placed on the final assembly requirements in the initial stage of the design."

Their advice to the designers?

For Wettermann, it's this: "Consider how you're going to put this thing together. Somebody who is what we jokingly call the "mouseketeer", the design engineer sitting at their workstation designing a product, whether it's a wearable or a rigid-flex part that's going to go on a missile system, they likely will not have any "how-to-put-it-together" experience. It's rare that this experience exists at the design level in flex. Once in a while, a consulting firm will get involved with the design and they'll have some experience in how the flex and rigid-flex goes together, so we invite them into the process and show them what the problem is. We want to show and tell them about some of the difficulties of how the assembly is actually done. I think helps put them on the learning curve a little faster. Whether it's rigid or flex, there's a lot of people in the design community have design expertise. That's why

people like David and I exist, to help put their products together."

Moody adds, "I would completely agree. When we're talking to somebody and they haven't vet laid



Bob Wettermann

another; it could have different height variation, it's going to start at a lower section of the box and fold and mold its way up to a higher section and understand where those aspects of the design are going to take place, where the bends are going to occur. And there are just some things you need to avoid. You can't put a component in an area of the flex circuit—even though we all talk about it being flexible—you still can't or shouldn't put a component in an area where you want to bend the circuit.

out the circuit, some of the first

questions we want to ask them is

what the application is, the envi-

ronment, what the final config-

uration of the circuit is going to look like, and how it is going to

fit inside the box or the device,"

says Moody. "If it has circuits, we assume that it's going to trans-

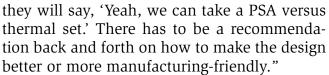
fer something from one end to

"Oftentimes, the engineers come in with preconceived notions about placement, 'Well, no, it's got to go here because I need to access something now that's over here.' Well guys, you're going to have to rethink that idea, because it isn't going to last. That's really the aspect, we try to understand the application and what that final configuration is going to look like so that we can advise where you want to put stiffeners on the flex if it's just flex, or where you're going to put your components, or at least the keep-out areas where you can't or shouldn't put components."

"There's one example that we ran across where the customer specified a stiffener close to a printer pad area for surface-mount. The customer would require thermal set, and that



has to be done before assembly. So, we gave them a recommendation that instead of thermal set, this stiffener can be applied using PSA [pressure sensitive adhesive] after assembly to save cost," says Matt Kan, EMS manager at Lenthor Engineering. "Sometimes, the customers will come back and say, 'No, we need it thermal set,' or sometimes



Moody says it's very important to have upfront engagements before the design gets set so that potential assembly issues can be addressed. "Often times, we found this to be very true before we brought assembly in-house. As Bob said earlier, it's that throw it over the wall mentality, let them figure it out—and that can add costs to the program, not only in dollars but in the delay of getting the product out the door," says Moody. "The time that's spent upfront to help design everything, including the assembly efficiently, in the end, gets you a better product and more efficient and all of those things. It's really important to do it all upfront."

Material Considerations

Most of the time, there are still misconceptions when it comes to flex materials to use to ensure better assembly.

Wettermann says some of their customers misunderstood the fallacies of some of the materials that flex circuits are made of, such as KaptonTM. "If you talk to people who are our

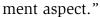


Matt Kan

customers, generally they're the product managers or the project managers, and you tell them that Kapton can actually rip—even though it has this great temperature withstand spectrum and it's got great mechanical stability, good thermal withstand properties, good dielectric properties, all the reasons they're using it—it still can actually shear and rip.

They respond with 'No way, it can't happen.' Well, yes, it can happen," he adds.

And Moody notes that there is not a real good understanding of the limitations of the material. "The other thing that I would point out is, and it's not strictly part of a component attachment aspect of the assembly, but when you're taking the flex circuit and you're going to then put it into a box, and that flex circuit has its components on it, ready to go, there's still somewhat of a misunderstanding about how flex circuits can bend and what degree of bend they can have. You could make it too inflexible, to the point that it really won't bend, and therefore you have a very difficult time reaching that curve aspect that you are looking for, or the function of the circuit to get from one level to another," he explains. "We have a lot of cases where we have to counsel people in regard to the materials stackup in order to fit the functionality or the form function of the circuit in the assembly. And again, that has nothing to do with these difficulties or peculiarities of getting the components on the circuit itself. It's just trying to get that circuit to conform within the box, once it is assembled. So that's another aspect of flex assembly that goes beyond just simply the component place-



Printing Considerations

When dealing with flex circuits, the standard paste printing method is still being used most of the time. However, there

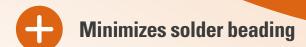
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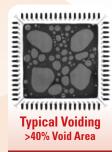


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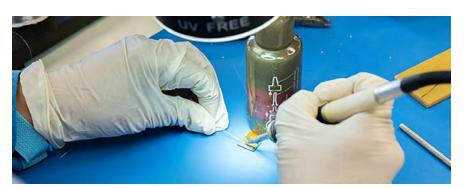
are some instances when jet printing is used, depending on the design of the flex circuit and the different thicknesses of the flex circuit.

"There are times where we used the traditional printing and then in addition we would use jet printing. A combination of both," says Matt Kan, EMS manager at Lenthor Engineering. "For example, you have double-sided components close to a stiffener, and that area, the stiffener or the rigid portion, is higher than the pads. So, you can print everything else traditionally. But in those areas where it's so close to the stiffener, you can't bend the flex, so you would have to opt to your jet printing. Or, if you don't have a jet printer, you may have to deploy hand soldering."

Kan adds that the speed of jet printing will impact flex circuit assembly from the paste printing standpoint, but he says he doesn't see jet printing taking over the whole process any time soon.

"From an equipment standpoint, the options are very limited," says Wettermann. "Mydata [Mycronic] certainly is one of the drivers there, ASYMTEK has a version. Making it more ubiquitous will allow you to use different kinds of either solder paste or conductive inks, and not just specific ones. That's a whole different engineering problem, but that would be advantageous for flex assembly if that printing problem were to be solved, and inkjet might be one of the ways.

"The only other thing I would add to that part of the discussion is that we do a lot of syringe dispensing using robotics, and then we do some pin transfer when the devices are very small. We seem to be able to control solder paste volume a little bit better than syringe printing, when that's the case."



Depanelization

Another topical area that is considered a big challenge when it comes to flex circuit assembly is depanelization.

According to Wettermann, most of these circuits are not the typically large such as 8" x 12" or 12" x 14" rigid boards. "Most of the time, they're multiple up flex circuits on a panel, part of one assembly. And the customer at the end of the day needs to put it into a housing, or we're putting it into a little housing, or doing some other secondary operation to it. But now, how do we depanelize—which is also a misnomer when you talk about flex, but how do you get individual circuits out of the multiple up panel? There are many cases where you have multiple kinds of material that we need to cut through or separate from the skeleton to singulate the individual assemblies. It's not just simply Kapton; it could be Kapton and copper, it could be Kapton, copper, and a laminate of some sort; the list goes on. Again, we're trying to depanelize essentially a giant noodle, and turn it into little noodles. This depanelizing operation on its own is very challenging; whereas in the rigid world, there are lots and lots of options for depanelization—breakouts and routing and laser scribing, etc.—while in the flex world, there are fewer options. In addition to the other problems that we already talked about—the three-dimensional nature, the multiple types of materials, and the lack of rigidity—singulating the circuits is also very challenging." To address this issue, Wettermann says lasers are commonly used to depanelize.

"We have five lasers here at Lenthor," says Kan. "We determine how we depanelize

upstream where, depending on the design, for rigid areas we pre-score both sides, leaving about 12-16-mils material thickness. There are times when we do a flex tab, leaving just the material of the flex circuit, and then we can just come in and use an X-ACTO knife and cut that away."



Kan notes, with flex the processes are not straightforward. "It's much different than your regular rigid board. There are back-end processes to consider as well, such as rework, wave solders, selective solder, 2nd operation, forming, etc., that you have to cope with. You can easily burn a flex circuit or damage a trace without knowing it. If you're not careful in what you're doing, not optimizing your rework temperature for instance, you can easily damage the flex itself before you even damage the components."

Moisture is a big factor with flex circuits as well, as they absorb moisture at least 30% faster than the traditional rigid PCBs. Which is why prebaking before assembly is essential.

According to Kan, they bake two to three hours prior the assembly process. He notes that planning correctly will avoid impacting cycle time.

"If you bake, use dry cabinets. Sometimes, things don't always go according to plan. Back when we started, we just kept rebaking the heck out of them...not good. Over time, we started using dry cabinets. After baking, we seal and store in the dry cabinets. Most cases, you don't even need to seal, just bake and store. Dry cabinets are essential when dealing with MSD, especially with flex circuits. We find that it works really well for us, and you don't have to keep rebaking as often," says Kan.

A Growing Market

The flex printed circuit market continues to be one of the fastest growing segments in the PCB industry. According to a new report by industry analyst firm Transparency Market Research, the global market for flexible printed

circuits, which was worth \$14.51 billion in 2017, is anticipated to expand at a CAGR of 11.8% over the period from 2018 to 2026 and reach a value of \$38.27 billion by the end of the forecast period. In particular, multilayer flex circuits are enjoying a greater demand among the products in this sector, and this trend is projected to remain so over the next few years, according to the report.

Mainly driving this growth is the significant rise in the consumer electronics industry, led by the growing demand for smartphones, tablets, and LCD displays, according to the report.

Moody sees the wearables market as one of the key sectors driving the flex circuit industry. "The wearables market sees a lot of things conforming to your body, or going around your wrist, going around your ankle, strapped to your back or your chest or your forehead. The conforming of that circuit to meet the environment that the circuit is going to live in, let's just say if it's something that's going to be around your wrist, there's going to be a flat portion of it that needs to be there so that you can have your components, and then there's got to be an aspect of that circuit that's going to be able to conform around your wrist. We want to keep components out of the areas where the circuit is bending or folding or conforming."

It's a fascinating field, according to Moody, wherein you get challenged with something new almost every day. "That's actually the fun aspect of this industry. Every day, somebody's coming in with a new application and you think, 'Wow, haven't thought of that. Let's try to figure that one out." SMT007



MilAero Highlights

Celestica Releases Q1 2018 Financial Results

Celestica Inc. has announced revenue of \$1.5 billion for the quarter ended March 31, 2018, up by 1% compared to the first quarter of 2017.

CTS Reports Strong Sales and Earnings Growth in 01 2018 ►

CTS Corporation has reported sales of \$113.5 million for the first quarter of 2018, up by 13.4% year-over-year.

Libra Industries Offers Complete AOI Traceability ►

Libra Industries has expanded its factory-wide Cogiscan Track, Trace & Control (TTC) Software to cover its AOI operation on multiple lines.

Neways Records Higher Turnover and Order Intake in Q1 2018 ►

Neways recorded fully organic net turnover growth of 13.7% in the first quarter of 2018, compared with the same period of 2017.

Solid Growth and Improved Profitability for Kitron in Q1 2018 ►

Kitron's revenue in the first quarter increased by 11%. Profitability expressed as EBIT margin



was 6.0%, compared to 5.3% in the first quarter of 2017.

Poor Supply Chain Management Will Cost You Money ►

If you can't trust your components to be legitimate and trustworthy, backed by a solid chain-of-possession, then every aspect of your electronics operation may be in jeopardy.

Sanmina Reports Revenue of \$1.68 Billion for Q2 Fiscal 2018 ►

Sanmina Corp. has posted revenue of \$1.68 billion for the second quarter of 2018, down from \$1.74 billion in the prior quarter and almost flat compared to the same period last year.

SMTA/CALCE Announce Program for Symposium on Counterfeit Parts and Materials >

The SMTA and the Center for Advanced Life Cycle Engineering (CALCE) announce the technical program for the Symposium on Counterfeit Parts and Materials this June 26-28, 2018 in College Park, Maryland.

Nortech Systems Reports Sales of \$26M in Q1 ►

Nortech Systems Inc. reported net sales of \$26.4 million for the first quarter ended March 31, 2018, which includes \$0.7 million of revenue recognized under new FASB accounting guidelines adopted this fiscal year.

Plexus Expands Presence in Malaysia ►

Plexus Corp. has expanded its presence in Malaysia with an acquisition of a new 432,000 square-foot manufacturing facility in Penang.



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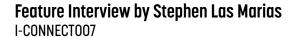
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Conversation with...Miraco:

Strategies for Successful Flex Circuit Assembly



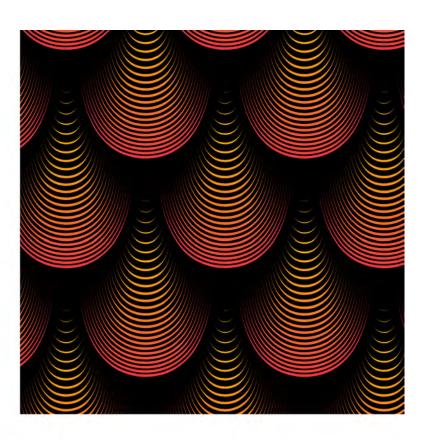
Miraco Inc. offers design, sourcing and value-added assembly of flexible interconnect products, including flex circuits, flat cables and wire/cable assemblies. The company services its diverse customer base from multiple locations—including headquarters in Manchester, New Hampshire, and its principal manufacturing site, Miraco South facility, in Tijuana, Mexico. The company also has additional satellite offices in the north and southeastern parts of the United States.

Jason Michaud, a 19-year veteran at Miraco, is the company's new vice president of

Jason Michaud

sales. In an interview with *SMT007 Magazine*, Jason speaks about the challenges in flex circuit assembly, and the best practices to address those issues.

Stephen Las Marias: Are you seeing increasing demand for flexible circuits?



Jason Michaud: Yes, with packaging sizes getting smaller, the need for creative flex solutions is growing. Overall, we are seeing an increase in demand for flexible printed circuits.

Las Marias: What factors are driving this?

Michaud: What's driving a good portion of new business for Miraco is the redesign and sourcing of flexible printed circuits for customers who had gone directly offshore with their flexible circuit requirements previously and have experienced problems doing so. We are seeing a lot of flex circuits that were underdesigned or improperly designed to meet their intended use.

Lus Marias: What are the top three challenges when it comes to flexible circuit assembly?

Michaud: The challenge for flexible circuit assembly is balancing electrical, mechanical, environmental and cost requirements with the material availability of suppliers and the manufacturability of the complete interconnect system. Pressure sensitive adhesive is a



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good example of something that is simple in relative terms compared to the flexible circuit layers; however, it drastically complicates the assembly process by limiting handling and cleaning options post soldering. However, if you process the soldering and cleaning of the assembly first, it is labor intensive and costly to apply the pressure-sensitive adhesive in piece form. It's a double-edged sword.

Lus Marias: Which parts of the assembly process are greatly impacted when doing flex circuit assemblies?

Michaud: When considering assembly, panelization and fixturing during design become important, as to panel size and panel stability. The number and type of components will dictate these parameters. These are important to facilitate the proper oven location during reflow. Oversized panels or unstable panels can greatly affect reflow and profile results in turn affecting yield and cost. Singulation post assembly is always a concern that is flexible circuit- and component-specific.

Las Marias: What strategies do you employ to address these challenges?

Michaud: Understanding the capabilities of the assembly equipment and its limitations is vital. Having calibrated equipment and a

known repeatable process is key. Outlining post assembly can be accomplished through steel rule die, hard punch dies or lasering. Depending on the components that are assembled, the number you are outlining, and the required outline tolerance determine the best and most cost-effective route.

Las Marias: How different is the assembly of flex circuits from rigid- or rigid-flex circuits? What are the critical factors to consider?

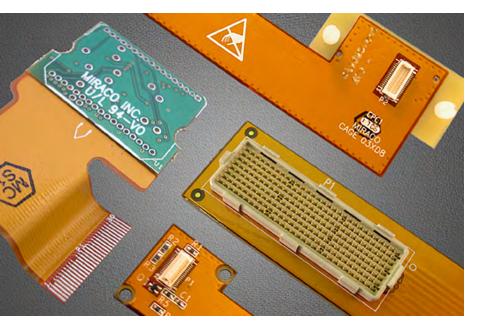
Michaud: Flex circuits are typically more sensitive to assembly processes than their rigid-flex counterparts. In either case, as both products are hydroscopic, pre-bake cycles are a critical precursor to any assembly. In flex assembly, consideration must be given to added support for solder pad and/or through-hole areas with stiffening materials, preventing stress from transitioning to the soldered joint as, of course, flex circuits want to flex. In rigid-flex, you are more typically assembling to the rigid area and it provides self-stress relief. Proper pad sizing and thermal relief during design helps optimize reflow and hand solder assembly.

Las Marias: What new technology or process do you employ to ensure flex circuit assembly success?

Michaud: We use a variety of SaaS (software-as-

a-service) collaboration systems that allow us to engage with customers, vendors, and internally to ensure the proper design, compatibility of materials, and the non-conflict of manufacturing processes used, in real time.

What we are trying to facilitate here is the involvement of evolved technology in communication. We've been using collaborative technologies from the U.S. to problem solve issues at Miraco South within hours—not days, not weeks, without personnel boarding flights. A photo or a video appears, and a meeting is held



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Las Marias: What are the best practices to consider when dealing with flex circuit assembly?

Michaud: Honestly, the best practices to consider when dealing with flexible circuit assembly is to engage with individuals that have experience with handling, processing, and designing flexible printed circuits. Miraco has 200 + combined years of flexible circuit and flexible circuit assembly experience.

Las Marias: What can you say to our readers about choosing EMS partners for their flex circuit assembly?

Michaud: Doing the proper due diligence when choosing an EMS partner is unequivocally the

best investment you'll make in a program. It is necessary to go beyond the standard quality audit and take the time to get to know the vendor's history and experiences with similar product on an intimate level, also choose partners that will engage early in the design process.

Las Marias: How do you see the flex circuit assembly market in the next 12 to 18 months? Do you see continued growth?

Michaud: I do see continued growth based on the emergence of medical and robotic technologies that are making it out of the R&D stages and into pre-production and production.

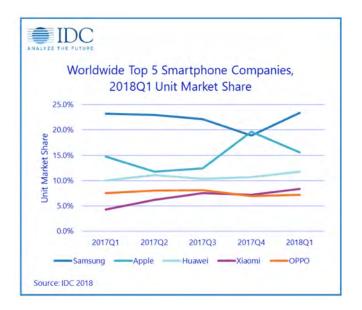
Las Marias: Do you have any final comments?

Michaud: Thanks for reaching out. I hope this helps some of your readers in their flex circuit projects. **SMT007**

Global Smartphone Market Fell 3% in Q1 on China Slowdown

Smartphone vendors worldwide shipped a total of 334.3 million units during the first quarter of 2018 (Q1 18), resulting in a 2.9% decline when compared to the 344.4 million units shipped in the first quarter of 2017, according to International Data Corp.'s (IDC) Worldwide Quarterly Mobile Phone Tracker.

The China market was the biggest driver of this decline



with shipment volumes dipping below 100 million in the quarter, which hasn't happened since the third quarter of 2013.

Samsung remained the leader in the worldwide smart-phone market, grabbing 23.4% share despite experiencing a 2.4% decline from Q1 2017. Apple Inc.'s first quarter saw the iPhone maker move 52.2 million iPhones representing a modest 2.8% year-over-year increase from the 50.8 million units shipped last year.

Huawei climbed to a new market share high of 11.8% even as it remained in third overall. While its high-end smartphones are popular in China, the bulk of its shipments are of the more affordable class of smartphones, and it also introduced a few new models in the low-end and mid-range segments.

Xiaomi's strong performance has no doubt been due to its strong growth outside of China. In Q1 2018, less than half of its shipments were domestic, a transition that very few Chinese companies have reached. OPPO held the fifth position, with its year-over-year decline of 7.5% more a result of the China slowdown than of its performance overseas, as both share and shipment volumes abroad increased in the first quarter.



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Session Topics

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Impacts on Industry and Society

What is Being Counterfeited & Beyond Electronics
Are the Standards Adequate to Protect You?
Technological Solutions: Tagging, Tracing & Authenticating

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Advanced Digitalization Makes Best Practice Part 1: Digital Remastering

Accelerating Tech–Insights from the Smarter Factory by Michael Ford, AEGIS SOFTWARE

As digitalization and the use of IoT in the manufacturing environment continues to pick up speed, critical changes are enabled, which are needed to achieve the levels

are needed to achieve the of performance and flexibility expected with Industry 4.0. Existing practices must be questioned and re-evaluated in the digital factory context. In this series, we look at examples of the traditional barriers to flexibility and value creation and

new

digital best practices to see how these barriers can be avoided, or even eliminated.

suggest

To understand more advanced opportunities provided by factory digitalization and IoT, we will consider both the manufacturing operation and the plight of the machine vendor, who has invested time and money, working hard to create an excellent automation technology that meets an industry need in a highly competitive environment. Even after the core technology of the machine has been developed and refined, there have traditionally been significant barri-

ers to overcome related to the communication of critical information. The machine itself in isolation is an example of Industry 3.0, an automated, self-contained process.

The connection of the machine into the digital infrastructure of the factory is the

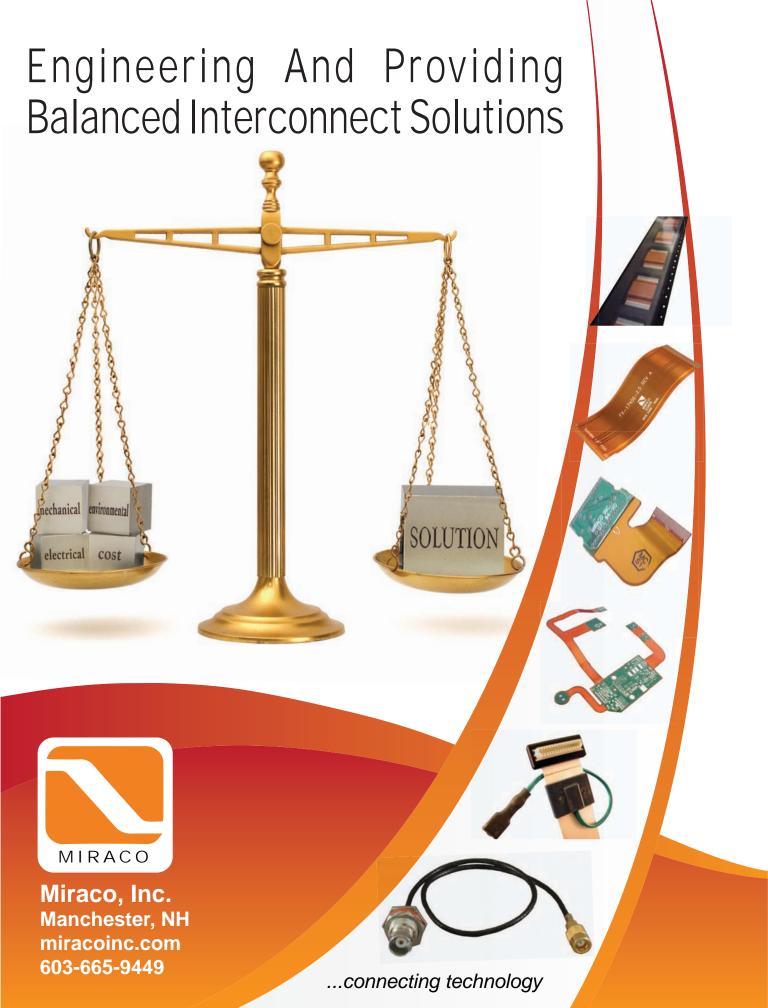
first key step towards

Industry 4.0. The part played by the digital IoT revolution is to remove these communication barriers and bring a real value to the machine vendor, not only reducing needless costs, but also enabling the of addicreation added-value tional in the machines themselves. The first such information exchange is the

engineering data needed to create the detailed machine instructions.

From Legacy Engineering Data Processing...

For any automated machine to operate, it is necessary to have a sequence of digital instructions to follow. The creation of these involves a clear and detailed understanding



of the product design and the bill of materials (BOM). As there are many automated machine processes involved with the assembly of a circuit board, each assembly process needs to understand their role, and select the data from the design/BOM combination that is relevant. This is repeated at every process, hopefully without duplication or anything missing. For assembly processes, the materials or actions that need to be performed at the process will be selected, with an understanding of what has been done at prior processes. For test or inspection processes, the clear and detailed knowledge of what has been done at prior processes is essential. Production engi-

For test or inspection processes, the clear and detailed knowledge of what has been done at prior processes is essential.

neers using the machine vendor software must make sense of information and select the appropriate data from what is given in whichever format the customer makes available. As there is so much variation in data formats and potentially many documents and files, there is a lot of checking and adjustment or translation of data to be done to avoid conflicts. This is a major pain for the machine vendor, as the customer ends up needing many layers of user-interfaces with which to perform these tasks, which the machine vendor is expected to provide. Any mistakes in the data preparation manifest themselves as incorrect machine operation, which often is initially attributed to the machine itself. A lot of effort is expended by the machine vendor to try to eliminate risks and issues, even though these are not essentially the vendor's responsibility.

The machine data preparation software should be focusing on taking the product data, together with knowledge of the machine features and capabilities, to create the most

efficient and effective operation as possible. With the continuous increase in product mix, the frequency of changes from one product to another increases, which brings a greater frequency of new product introductions and changes in machine setup. In many cases already, the time taken to change the setup of the machine between sequential work-orders representing different products exceeds the actual time that the machine is working to add value. Were the machine vendor to have visibility of the data for the whole sequence of expected production work-orders in the nearterm, their operational optimization could be extended to include consideration of how to reduce setup time between products (e.g., through the creation of the common location of materials, as long as machine execution time was not too severely affected). This can be especially effective where multiple processes in a connected line are grouped and managed through a single overall machine vendor software platform such as those currently provided by the larger machine vendors. However, this creates the need for product data to be available to the machine vendors' software earlier. As Industry 4.0 brings a yet higher level of flexibility requirement, this easily overloads the engineering data preparation capability. In most operations it is already a challenge to keep up with data preparation on a done-byone basis. Neither machine vendors nor manufacturing engineering will be able to achieve the expected flexibility in the flow of data required for Industry 4.0 without the help of digitalization.

...To Digital Best Practice

Having data from design (both electrical and mechanical) and BOM delivered as a single digital product model, in the form for example of the IPC-2581 standard, means that a vast amount of product data processing of the otherwise many documents and files is eliminated. This approach really makes sense considering that practically every product is designed digitally and every BOM is maintained digitally. There is simply no reason any more why the product data should be split

into legacy formats intended for humans to process. Issues raised about product IP protection are nonsense, as however the data is sent, the product data itself is eventually re-created by the manufacturing entity in a format that can easily be replicated. The core issue is that the use of legacy formats forces human intervention, which creates unnecessary cost, delay, and the likelihood of mistakes, all of which fundamentally affect the business performance of the product. Being an open standard, the use of the IPC-2581 digital product model is available as a standard singleclick output from professional design systems. The design through manufacturing flow, that is the communication of the product model to manufacturing can therefore be done in seconds, rather than hours or even days.

The next stage of the digital process is to utilize a digital manufacturing engineering system that has knowledge of production configurations, that will apply the digital product model to a line configuration, automatically splitting out the data as required by each of the processes. Once again, the digital solution reduces work that once took hours or days into a few seconds. As this data assignment process can be done so quickly, the selection of a specific line configuration need not be fixed far in advance. The assignment of line and creation of the work-order can in fact be done very close to the start of production without risk. This means that there is the ability to have a choice of multiple line configurations, each of which can be assessed to decide which one meets the immediate customer need in the most efficient way. The best manufacturing engineering systems therefore support assignment of product to line configuration "on demand." This enables real-world factory schedules and work-order assignments to be made just in time, such that immediate reaction can be made to changes in customer demand. This contrasts significantly with prior Industry 3.0 practices, where decisions had to be made at the shop-floor level many days or weeks in advance, with only crude and often ineffective simulation techniques for planning optimiza-

tion. This new best practice of digitalization of the engineering data preparation process is therefore completely in line with the requirements of Industry 4.0, and in fact without it, there is no chance that an Industry 4.0 operation could practicably be sustained.

DDD Best Practice

Digital best practices, including the use of the digital product mode for both automated machine processes to take place and the creation of paperless product documentation/work-instructions for non-automated processes, which will be covered in more detail later, means that everything required for manufacturing is created digitally, transferred digitally, and executed digitally. For those who remember the birth of digital music on CD, this is the sought after DDD format of music, where no analogue, or in this case human manipulation of the data has taken place.

This is the first piece of our digital re-mastering of MES, where new best practices are developing. As a summary of the digital best practice flow for preparation of data for automated processes:

1. Digital Design Process

- a. A digital product model is created by the design system in IPC-2581 format, including both the electrical and mechanical design features.
- b. Where supply-chain data is managed centrally (in a multi-site organization with centralized PLM for example), the production BOM is applied to the IPC-2581 file directly before it reaches manufacturing

2. Digital Manufacturing Engineering System

- a. The single IPC-2581 digital product model file is received into manufacturing
- b. Where supply-chain data is managed locally by ERP, the BOM data is merged, on receipt of a single digital file
- c. The manufacturing engineering tool identifies capable line configurations, which are communicated to the digital production planning system

3. Digital Planning Process

a. The decision about which choice of line configuration to use is made depending on the immediate customer demand requirement. The decision-making algorithm considers the capabilities and availability of machine processes, effects of the commonality of product mix and availability of resources.

4. Digital final process optimization and execution:

- a. Information is transmitted from the digital manufacturing engineering system to the identified machines. This is best done using the digital IPC Connected Factory Exchange (CFX) IoT protocol.
- b. The machine vendor receives an assured dataset, which can be used reliably to create the optimized machine operation. In high-mix or Industry 4.0 scenarios, the machine vendor can include optimization of the machine setup together with execution optimization based on the sequence of products that will be executed.

Following this digital best practice, the manufacturer receives their expected benefit, with a significant reduction in new product introduction lead-times, a step change in flexibility,

the elimination of engineering mistakes, and the ability to support an Industry 4.0 operation from an engineering perspective. For the machine vendor, there is a huge reduction in the work needed by the software to resolve external data issues. This enables them to focus on optimization, that includes grouping of products planned in a flexible way, to be executed in a known sequence, such that changeover times can be reduced. Though the time needed to prepare and setup the machine has greatly reduced, the effectiveness and performance of the machine overall will increase, thus increasing the value proposition of the machine especially in Industry 4.0 scenarios.

This is the first part in a series in which we look at new digital best practices. The series includes looking at manual processes, the supply-chain, quality management as well as planning, and how digital data formats and communication standards combine to create the new paradigm of digital manufacturing and Industry 4.0. SMT007



Michael Ford is the European marketing director for Aegis Software.

Infrared Spectrometer on a Chip

Scientists at the University of Campinas's Device Research Laboratory (LPD-UNICAMP) in Brazil, collaborating with colleagues at the University of California San Diego in the United States, have developed a Fourier-transform infrared (FTIR) spectrometer based on silicon photonics.

Resulting from Mário César Mendes Machado de Souza's PhD research and a research internship abroad, supported by scholarships from FAPESP and supervised by Professor Newton Frateschi, the new spectrometer is described in an article published in *Nature Communications*.

Various projects have appeared in recent years to

develop an FTIR spectrometer based on integrated photonics, but progress had so far been scant owing to several technical challenges, such as the highly dispersive profile of silicon waveguides.

The researchers succeeded in overcoming these challenges by creating a laser calibration method to quantify and correct the distortions caused by silicon waveguide dispersion and non-linearity. As a proof of concept, they developed a 1 mm² FTIR spectrometer chip based on standard silicon photonics fabrication procedures.

The researchers now plan to engineer a device that is totally functional and integrated with photodetectors, light sources and optical fibers.

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IPC E-Textiles 2018 is a one-day technical and business education workshop on e-textiles that will bring together innovators, technologists and engineers to collaborate on solutions, identify partners and identify solutions to propel growth for the e-textiles market.

Topics will deal with all aspects of e-textile development, including:

- E-textile wearables for consumers, sports, medical, military and safety markets
- Bringing the IoT to textiles
- How to develop an e-textiles business model
- How to collaborate with the supply chain to get the end-product you envision
- Materials and components that make up e-textiles and how to select the right ones for your

Visit www.ipc.org/E-Textiles-2018 for seminar updates and to register today.

IPC E-TEXTILES COMMITTEE MEETING

In addition to the technical education and networking on **September 13**, **IPC E-Textiles 2018** will also be host to an open-forum **IPC E-Textiles Committee Meeting on September 12**. Plan to arrive a day early to meet with others from your field to brainstorm standards and test methods needs and learn how to influence industry standards being developed by the IPC E-Textiles Committee.

Want to learn more about the IPC E-Textiles Committee and how you can join? Email ChrisJorgensen@ipc.org for availability.

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Conversation with...Vexos: Doing it Right the First Time

Feature Interview by Stephen Las Marias I-CONNECTO07

Vexos Corp. is a high-mix, low to mid-volume EMS provider with facilities in the United States, Canada and China. Vexos primarily focuses within the automotive, industrial, networking, communication, medical and security market segments.

Harry Chan, Deputy GM and VP Manufacturing for Vexos Shenzhen, is responsible for all aspects of manufacturing through continuous process improvement, production management, and development of manufacturing talent and teams. In an email interview with *SMT007 Magazine*, he shared the challenges when dealing with flexible circuit assemblies, and strategies and techniques to address them.

Stephen Las Marias: What's driving the increasing demand for flex and flex assemblies?

Harry Chan: The major factor for flex circuits is new technology and the need to work with PCBAs that can be manipulated to conform to the finished product. Also, moving to smaller devices means limited space allocation for key components. As OEMs and device manufacturers work with smaller components for their products, flex circuits provide a viable solution.

Lus Murius: What are the top three challenges when it comes to flexible circuit assembly?

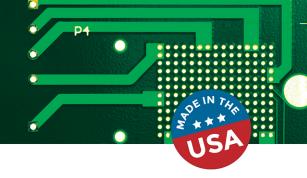
SUCCESS with FIFX

Chan: We have developed key processes through our manufacturing systems to better manage the way we build products that use flex circuits. The most common areas we encounter are:

- 1. Flatness and temperature profile control in the SMT process: Understanding the nature of the board and controlling environment at the SMT level is very important to the success of the product.
- 2. Difficult or impossible to repair/rework:
 Sometimes, we come across RMA request from our customers that can be a challenge from a repair or rework standpoint.
- 3. Handling/storage issues: We adhere to proper storage conditions. Vexos has key handling and manufacturing processes in place to ensure we meet these challenges when handling or storing flex printed circuits boards.

Las Marias: What strategies do you employ to address these challenges?





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Harry Chan

Chan: Our strategy is, do it right the first time (DIRTFT). Early manufacturing engineering is very important; we start from design level to minimize the unnecessary cost and manufacturing impact. We review the design with the customer in the early stages and provide flex circuit layout design guidelines. We replace or minimize the design to rigid-flex circuits, if there is no special size, weight, impedance, electrical noise, or other limitations.

Las Marias: How different is the assembly of flex circuits from rigid circuits, and what are the critical factors to consider?

Chan: There are several key factors that must coincide when working with customers that require a solution using flex circuit boards—these are technology through to manufacturability and the landed cost.

- 1. Cost efficiency: Manufacturing and assembly costs are significantly more expensive compared with rigid-flex circuits.
- 2. SMT process: Special assembly carriers are required to control the flex

- circuit flatness during the screen printing/SMT and other processes.
- 3. Repair/rework: Difficult or impossible to repair/rework.

Las Marias: How do you ensure flex circuit assembly success?

Chan: Controlling the manufacturing processes can minimize the manufacturing issues.

- 1. Storage: Requires proper storage conditions.
- 2. Baking: Requires proper baking before flex SMT.
- 3. Assembly carrier: Special design assembly carrier required to keep the flex circuitry flat during the screen printing/SMT processes, etc.
- 4. Solder paste: Selecting low-temperature solder pastes (i.e., ALPHA OM-550) can minimize any delamination or heat damage after reflow.
- 5. Soldering wire: Selecting the lowtemperature soldering wire can minimize any delamination or heat damage during the hand soldering/repair or rework process.

Las Marias: What are the best practices to consider when dealing with flex circuit assembly?

Chan: Due to the flexible circuit technology, certain design and assembly considerations must be accounted for. Fortunately, the design rules for flex circuits are very similar to the design rules for traditional PCBs. That is, the designer must pay attention to certain design aspects: minimum hole sizes, minimum trace widths, minimum space between traces and pads, minimum distances to design edges, flex circuit/board outline tolerances, distance of copper geometries from flex circuit/board edges, and copper and overall design thicknesses.

Traditional PCBs and flex circuits share some, but not all, of the manufacturing process steps. For instance, the flex material—usually copper clad polyimide—is selected, drilled,

plated, photo-imaged, developed and etched just like the traditional PCB process. The next step, also similar for both PCBs and flex circuits, involves the panels being baked to remove any moisture from the wet processes. It is after this step where the traditional PCB and flex circuit processes begin to differ. Instead of going to the solder mask station, as would happen with traditional PCBs, flex circuits go to the coverlay station.

- 1. PCB layout design support: Review and provide flex layout design guidelines to the designer.
- 2. Manufacturing tooling design: Review and design the proper assembly carries.
- 3. Manufacturing process: Review and create the proper assembly processes for SMT/ hand solder and repair or other processes.

Las Marias: What can you say to our readers about choosing EMS partners for their flex circuit assemblies?

Chan: Choose the right manufacturing partners with a proven track record. From small consumer handheld products to sophisticated medical or avionics systems, flex circuits are integral to almost every product that we use today. The demand for more compact, highperformance products and a competitive market has brought flex circuit technology into sharp focus. Product quality, viability, performance and cost all depend on your flex circuit design.

While fulfilling our customer needs is critical, success and profitability also depend on how the manufacturing partner can support the product design and development process.

With applications and materials continually being designed and developed, the latest technology promises to revolutionize many aspects of electronic circuit design.

It's important to consider the following key areas when choosing an EMS provider:

- Make sure your EMS provider has experience in flex circuit assembly
- Ensure your EMS provider is involved in your flex layout design and support
- Know whether your EMS provider can give flex design layout guidelines

Las Marias: How do you see the flex circuit assembly market in the next 12 to 18 months?

Chan: I see the flex circuit market continuing to grow. The growth is largely fueled by the Internet of Things movement. With everything becoming interconnected in cars, homes, and mobile devices, the requirement for flex circuits will grow.

Las Marias: Do you have any final comments?

Chan: Although it seems that an assembly is an assembly is an assembly, that is not always the case. Working with flex circuits brings unique challenges and unless you have been working with them repeatedly, an assembler will not know what pitfalls to avoid. When you couple the component knowledge, flex and rigid-flex circuits with the manufacturing acumen, you have a winning combination.

Las Marias: Thank you very much, Harry.

Chan: Thank you. SMT007





Supply Line Highlights

Alpha Assembly Solutions and Fairphone to Study Responsible Recycling ▶

Alpha Assembly Solutions has joined forces with Fairphone, the creator of the world's first ethical, modular smartphone, to research and raise awareness on the challenges associated with sourcing recycled materials in the electronics industry.

Seika Announces Plans for Optimized Drying Units to be Incorporated into all McDry Cabinets

Seika Machinery Inc. has announced that all McDry cabinets will soon be able to maintain one percent RH levels with the new optimized drying units, like the McDry DXU-1001A UL Quick Dehumidifying Model.

RTW IPC APEX EXPO: MEK on Increasing Demand for THT AOI Systems

Henk Biemans, managing director of MEK Marantz Electronics Ltd, speaks with I-Connect007 Managing Editor Stephen Las Marias about what's driving the increasing demand for THT AOI systems.

SMT Renting: A Trend for the Future? ▶

In this interview, Martin Ziehbrunner explains how his latest company—SMT Renting—is



challenging the normal way of acquiring SMT capital equipment.

Koh Young Supports Hermes Standard Meeting at NEPCON China 2018 ▶

Koh Young Technology recently attended the 3rd Hermes Standard (THS) initiative meeting in Shanghai, China, which focused on many critical topics like field testing, synergy with the IPC CFX (Connected Factory Exchange), and further protocol development.

Indium's Solder Paste Wins SMT China Vision Award ►

Indium Corporation has earned the SMT China Vision Award for its Indium10.1HF Solder Paste at the recent NEPCON China 2018 event in Shanghai.

Electronic Systems Expands Capabilities with Fuji AIMEX Placement Machines

Electronic Systems Inc. has strengthened its capabilities by acquiring three new Fuji AIMEX III surface mount placement machines.

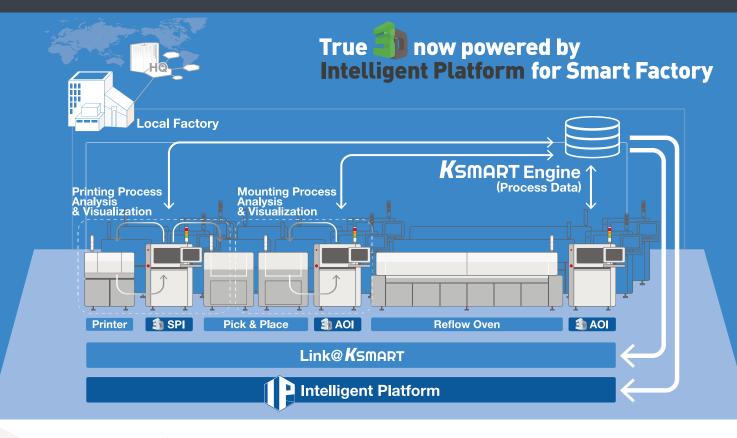
Techcon Systems Names David Reyes Territory Sales Manager ►

Techcon has hired David Reyes as the new territory sales manager, who will manage the company's Midwest and Mexico divisions.

RTW IPC APEX EXPO: Mycronic Broadens Product Portfolio

Thomas Stetter, senior vice president of assembly at Mycronic, discussed with I-Connect007's Pete Starkey how their company continues to broaden their product portfolio towards a full-line SMT solution and the Industry 4.0 automated factory.





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Conversation with... Thermaltronics:

Addressing Temperature Challenges in Flex Circuit Rework



Feature Interview by Stephen Las Marias I-CONNECTO07

During NEPCON China 2018, I met with Zen Lee, technical director, and Michael Gould-smith, sales and marketing director of Thermaltronics, a manufacturer of soldering products and rework equipment. We discussed the challenges of flex circuit assemblies, especially during the rework process. They highlighted the power-on-demand feature of smarter hand-soldering systems, as well as how Curie Point helps operators avoid temperature overshoots during rework.

Stephen Las Marias: What are the top challenges when working with flexible circuits?

НОТ

(hint: not too hot!)

Zen Lee: The most important consideration is that the parts are very small. You need to have a fixture, since you cannot hold the flex board. The tip needs to be of the correct geometry, for the application and you need address, (touch), and the joints in the correct manner – in other words – "not heavy handed". Basically, you cannot fool around, when doing this kind of rework, because the real challenge is the potential for delamination of the flex circuit. Good solder joints are essential —you have to take away the energy

from the tip and give it to the joint, but you don't want to overshoot. Otherwise, you will also have solder splash issues, on top of delaminating the flex circuit. That's the problem.

Las Marias: When reworking flex circuits, what are the key issues to consider?

Lee: I think it is the control issues. Because if soldering is done by hand, the operator needs training as well as the knowledge to select the right soldering tip.

Michael Gouldsmith: One of the key points Zen is making is concern-

ing the tips we manufacture, which feature a unique technology called Curie Point. There is no overshoot in temperature; we maintain the temperature very well. It's also a power-ondemand basis. So, if there's enough stored energy in the tip, unlike a conventional soldering iron, which is providing constant power, there's less

chance of delamination, less chance of solder splash, less chance of rework problem, and losing the flexible circuit.



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Las Marias: What are the best practices to consider when dealing with flexible circuits during rework?

Lee: Ideally, it should be one touch, and you make the joint. That means you cannot use the tip to do it twice, or many times. Too many touchups, and you will have a problem, because the joint is very small, and the tip geometry is very small, and of course, as I said previously, the operator needs good manual soldering skills.

The tool, the tip cartridge or soldering iron, is an equipment issue. You need to select correctly the equipment first. The second part into making a good rework is the operator. You need to have both. If you have a good operator, but you don't have good equipment, you will get delamination. If you have good equipment, but not a good operator, you will still have a problem. So, it's the combination

of the human factor and good soldering iron.

Gouldsmith: It's a combination of two skill sets: the skill sets of the operator and the quality and performance of the tip. Because we use the Curie Point, there is no chance for any of the problems that occur with conventional



Zen Lee



Michael Gouldsmith

soldering irons. With conventional soldering irons, you have the potential for overshoot of temperature, constant power, instead of "power on demand", and as a result delamination or solder splash.

Las Marias: Do you think there will always be an issue when dealing with flex circuit assemblies?

Lee: Yes, always. Once they use a flexible printed circuit, that means assembly issues, that means space issues—they need tight solutions, so they use flex circuits. That means the joints and components are very small.

Las Marias: In which markets do you see the use of flex circuits increasing?

Lee: Mobile phones, cameras, whatever device that's getting smaller

and thinner. They're always going to need flexible circuits.

Las Marias: Great. Thank you both very much.

Zen: Thank you. SMT007

RTW NEPCON China: Koh Young Discusses Smarter Inspection

At the recent NEPCON China 2018 event in Shanghai, Harald Eppinger, managing director of Koh Young Europe, speaks about the need for improvements in process capabilities to optimize the PCB assembly processes. He notes that catching defects is already a given, and that manufacturers now should focus on how to prevent them.

Other topics discussed include the increasing use of artificial intelligence (AI) in inspection systems and its impact in the overall process; the Hermes standard and the IPC CFX Demo; and new technologies from the company.

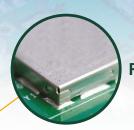


Watch the interview here.

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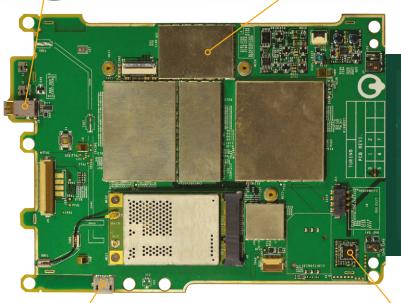


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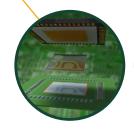


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IPC Addresses Skills Gap

One World, One Industry

by John Mitchell, IPC-ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

In a recent IPC global survey, we found that while the skills gap may vary depending on the job role and geographic location surveyed, many companies in our industry are struggling to find the talent they need, and the problem is expected to continue over the next decade.

Sixty-four percent of companies reported difficulty finding skilled production workers, and 71% indicated similar trouble hiring qualified engineers. Respondents also noted a low level of satisfaction with training options, a willingness to utilize online training, and a need for training options for different roles in the company. The IPC survey follows a joint Deloitte Consulting LLP and the Manufacturing Institute survey reporting that 74% of industry executives noted a significant skill deficit in their skilled production workers, ranging from

operators to technicians. With this feedback in hand, IPC is working hard to provide solutions to these workforce education challenges.

For example, IPC's online learning management system, IPC EDGE, is designed to provide training and testing services via the internet for a global audience. Launched in 2016, IPC EDGE hosts a variety of learning opportunities including white papers, webinars, IPC standards, skills development resources, and IPC certification courses, as well as access to an extensive library of educational content globally.

One of the first programs to be released on our new platform was the six-week online Electronics Program Manager training and certification program. The classroom version of this course launched in 2003, but with

Skills in which manufacturing employees are most deficient:



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69% problem solving skills



67% basic technical training



60%

math skills

Note: Percentage indicates the percentage of executives who did not opt for "Extremely sufficient" or "Sufficient"

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member feedback, we updated and streamlined the course, which was relaunched within IPC EDGE in Q3 2018.

The revised program will be offered in two different models: a traditional classroom course, which will be help periodically at select locations, and an online training program that can be completed remotely. The online program will run for six weeks, with fixed start and end dates, instructor lectures, group discussions, role-playing exercises, team projects, and peerlearning opportunities.

In addition to revising the EDGE platform, IPC formed the Jobs Task Analysis (JTA) Committee, a group of industry experts who are tasked with defining a competency model for the electronics industry. The JTA Committee will examine various job roles to determine what knowledge, skills, and abilities (KSA) are required to meet the needs of the current and future workforce and will construct accurate and valid job descriptions.

Through IPC EDGE, we will work toward providing training for each job role and offering a variety of educational opportunities for every individual to gain the competencies needed to take the next step in their career.

We welcome your input and involvement in addressing the workforce needs of our industry. Please consider joining our JTA Committee to help us identify and define job roles and provide feedback to the various subgroups that will branch out from the main committee. By participating in the committee, you will help us to ensure that the content we are creating is designed to meet specific industry needs.

For further information on the JTA Committee, please contact David Hernandez, IPC senior director of learning and professional development, at DavidHernandez@ipc.org. SMT007

References

1. The Skills Gap in U.S. Manufacturing.



John Mitchell is president and CEO of IPC-Association Connecting Electronics Industries. To read past columns or to contact Mitchell, click here

Imec Develops Screen-Printing Process for Highly Efficient n-PERT Solar Cells

@ imec

Imec has partnered with EnergyVille to develop a highly efficient n-PERT (passivated emitter and rear totally diffused) solar cells using an industry-compatible screen-printing process. Together with Jolywood, imec developed bifacial cells with an average front-side conversion efficiency of 21.9 percent. Based on this process, imec also demonstrated screen-printed monofacial

n-PERT cells with a conversion efficiency up to 22.8 percent.

The new bifacial cells use narrow printed silver (Ag) fingers on the front-side and printed aluminum (Al) fingers on the rear. Using Al instead of AgAl lowered the cost per cell to 0.01\$/Wp, as well as reduced the recombination in the contact area by avoiding the typical spiking of AgAl contacts—allowing to optimize the emitter independently

from the contact firing and giving an additional boost to the efficiency.

On a batch of M2-sized cells, an average conversion efficiency of 21.9 percent was demonstrated, with the best cell topping 22.1 percent. These results were measured using an ISE CalLab calibrated reference cell, under stan-

dard test conditions using a AAA-class WACOM solar simulator. Used in bifacial operations under

standard front illumination conditions in conjunction with an additional 0.15 sun rear illumination, these cells can achieve an effective efficiency of 25 percent.

Imec also fabricated screen-printed monofacial nPERT cells with efficiencies up to 22.8 percent, which is a state-of-the-art result for an industry-compatible fabrication process.





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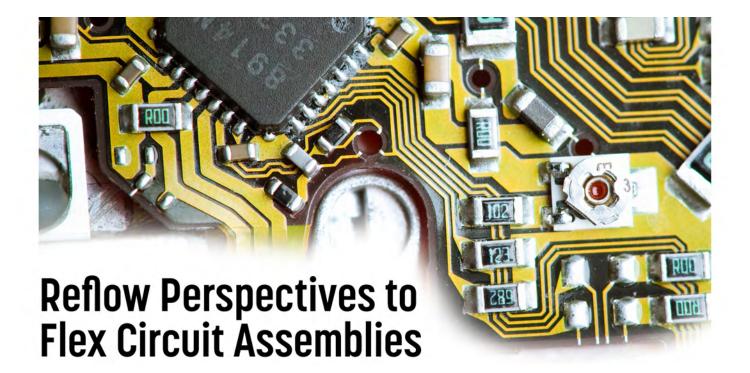
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Feature by Stephen Las Marias I-CONNECTO07

At the recent NEPCON China 2018 event in Shanghai, I spoke with Ralf Wagenfuehr, plant manager at Rehm Thermal Systems (Dongguan) Ltd, to gain insight into flex circuit assembly, and the challenges of reflow soldering.

According to Wagenfuehr, flex circuits are increasingly being used in mobile phones over the past two years as manufacturers have been redesigning their phones with more curves and more functions and additional components inside.

"The PCB is getting smaller, and modules are being built on the flex printed circuits, not only the connector. Now, it's integrated circuits in the flex boards, and sensors, which are becoming much smaller. As an example four years ago, the smallest chip component was 03015. Now, the 008004 chip component is also on the market. The 008004 component is 35% smaller than the 03015 component. The challenge of reflow soldering is how to ensure the oxygen content in the reflow chamber and how to ensure the stability of the reflow air volume to avoid such defects as tombstone." Wagenfuehr says. "You can now bring the components in mobile phones to the position that is good for the user. More and more, these applications—mobile phones, smart devices, and other similar applications—are definitely increasing the market demand for flex circuits. But I think, in big components like in automotive, it is very seldom used because of the reliability of flex circuits in such applications. They should last for years, not only just for a short time., They are using other components, for instance, the flex circuits may be integrated in housings, MID's moldings—in automotive electronics. But flex circuits, definitely more and more in handheld devices."

One of the biggest challenges when it comes to the reflow soldering of flexible circuit assemblies is warping. "First of all, flexible circuits are very light. While some customers are trying to process flex circuits without holders or carriers, experienced manufacturers are using magnetic holders or similar things to keep the flex circuits in place. But I think soldering is not only the biggest issue. I believe, printing and chip mounting are definitely a challenge for manufacturers when it comes to flex circuits because they are not steady."

According to Wagenfuehr, mitigating this problem starts with the design. He says designers should consider not only the application but also the manufacturing. In fact, there is a clear definition of IPC-6013 with



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Amendment 1, Qualification and Performance Specification for Flexible Printed Boards. As long as the FPC has the correct design, it can be reasonably used in the manufacturing process.

"Some applications are very hard to realize; and some applications cannot be processed in the reflow. Some applications may be unsuitable for condensation soldering systems. So, the manufacturer of flex circuits should consider the

manufacturing processes, the whole step," he explains. "Ordinarily, we are just supporting the applications in general. When we're having issues and the customers cannot solve it, this very point that's just mentioned, maybe the manufacturer of such boards should come with the equipment suppliers earlier in the stage. That will be much more helpful. Also, having them early at the design stage, to fit it in the whole process chain, will make it easier to manufacture the flex circuit assemblies."

Wagenfuehr also stresses the importance of communication with their customers and users. "There are a lot of limits that they should



Ralf Wagenfuehr

consider—limits in the design, in preparation of the fixtures—to ensure proper soldering. We can support our customers in applications where we have certain experiences, such as in mobile phone manufacturing, for instance. We also have to know more about our customers issues. We are happy to help in the process steps. We have a rich experience and we can also consider the early design stage with our application teams

in China and Germany."

In fact, Wagenfuehr notes that they will be willing to join forums to address these issues. "It will be nice if it is focused on soldering flex printed circuits. There is not much forums happening in manufacturing in this front. It's always driven by the designers—that's the problem. They don't ever consider the equipment. They just do the designs, which, sometimes are impossible or quite challenge to manufacture. It will be good if forums will be created to bring the designers and equipment manufacturers together to discuss the issues. That will be helpful in the future." SMT007

Northwestern Researchers Predict Materials to Stabilize Record-high Capacity Lithium-ion Battery

A Northwestern University research team has found ways to stabilize a new battery with a record-high charge capacity. Based on a lithium-manganese-oxide cathode, the breakthrough could enable smart phones and battery-powered automobiles to last more than twice as long between charges.

The study was published online in Science Advances.

A French research team first reported the large-capacity lithium-manganese-oxide compound in 2016. But it was not without its challenges—the battery's performance degraded significantly within the first two cycles that researchers did not consider it commercially viable. They also did not fully understand the chemical origin of the large capacity or the degradation.

After composing a detailed, atom-by-atom picture of the cathode, Christopher Wolverton, the Jerome B.

Cohen Professor of Materials Science and Engineering in Northwestern's McCormick School of Engineering, and his team discovered the reason behind the material's high capacity: It forces oxygen to participate in the reaction process. By using oxygen—in addition to the transition metal—to store and release electrical energy, the battery has a higher capacity to store and use more lithium.

The Northwestern team turned its focus to stabilizing the battery to prevent its swift degradation. The computations pinpointed two elements: chromium and vanadium. The team predicts that mixing either element with lithium-manganese-oxide will produce stable compounds that maintain the cathode's unprecedented high capacity. Next, Wolverton and his collaborators will experimentally test these theoretical compounds in the laboratory.



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Electronics Industry News and Market Highlights

Chrome OS Detachable Tablets Paint a Brighter Future While Tablet Market Struggles >

Global tablet shipments in the first quarter of 2018 reached 31.7 million, declining 11.7% from the prior year, according to preliminary data from the International Data Corporation (IDC) Worldwide Quarterly Tablet Tracker.

Micro-LED Market Worth \$20.5B by 2025 ►

Increasing demand for brighter and more power-efficient display panels for smart watches, mobile devices, and NTE (AR/VR) devices is expected to propel the micro-LED market to grow from \$0.6 billion in 2019 to \$20.5 billion by 2025, at a CAGR of 80.1%.

Six Predictions that Will Shape the Global Energy Storage Sector in 2018 ►

Frost & Sullivan's recent analysis, Global Energy Storage Market Outlook, 2018, finds that the total installed capacity will grow 15.9% between 2017 and 2018, and the top six countries—China, United States, South Africa, Chile, France, and Israel—will complete installation of 1,369 MW of grid-scale ESS projects in 2018.

Global Semiconductor Packaging Materials Market Reaches \$16.7B

SEMI and TechSearch International reported that the global semiconductor packaging materials market reached \$16.7 billion in 2017. While slower growth of smartphones and personal computers—the industry's traditional drivers—is reducing material consumption, the slow-down was offset by strong unit growth in the cryptocurrency market in 2017 and early 2018.

Industrial 3D Printing Market to be Worth \$5.6B by 2023 ►

The industrial 3D printing market is expected to grow at a CAGR of 27.21% between 2018 and 2023, to reach \$5.66 billion by 2023 from \$1.73 billion in 2018.

Global Server Shipment Posts Slight Decline in 1018 ►

According to the latest report of DRAMeX-change, a division of TrendForce, the global server shipment experienced slight decline in 1Q18, but the demand for CPU, Server DRAM, and other related components remain flat.

Global Semiconductor Sales Up 20% Year-to-Year in 01 ►

The Semiconductor Industry Association (SIA) has announced that worldwide sales of semiconductors reached \$111.1 billion during the first quarter of 2018, an increase of 20% compared to the first quarter of 2017, but 2.5% less than the fourth quarter of 2017.

Price Decline in LCD TV Panel Market to Continue in 2018 ►

Prices of LCD TV panels of all sizes have been decreasing since the end of 2Q17, and have not shown any sign of stop so far, according to the latest report from WitsView.

Robots to Populate E-Commerce Warehouses at a High Rate ►

ABI Research estimates that shipments of global commercial and collaborative robots in e-commerce fulfillment will reach 443,000 units in 2026, twenty-fold of current shipments in 2018.



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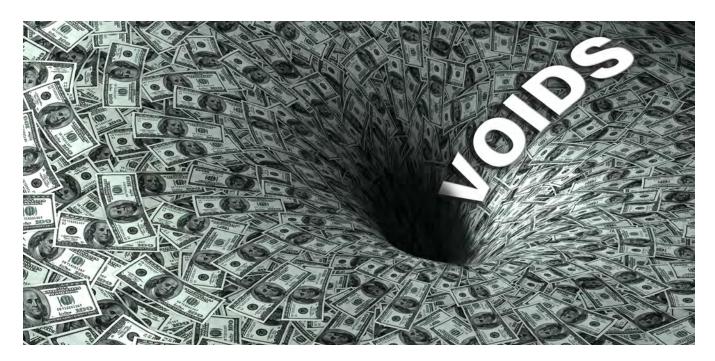
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Novel Approach to Void Reduction Using Microflux Coated Solder Preforms

Article by Anna Lifton, Paul Salerno, Jerry Sidone and Oscar Khaselev Alpha Assembly Solutions

Bottom terminated component packages, such as QFN, are becoming increasingly relevant due to their ability to carry high-power dies in a small form factor. With increasing reliability performance requirements, power management components in packages like QFNs are critical to optimizing thermal and electrical performance. Additionally, low voiding is important for decreasing the current path of the circuit to maximize high-speed and RF performances^[1]. The market demand for void reduction under thermal pads of QFN components due to shrinking package sizes and increasing power requirements has generated the need to evaluate key process factors that contribute to voiding to design an optimal solution.

The addition of a micro-fluxed preform in conjunction with a low-voiding solder paste and process knowhow is seen to create ideal solder volume with minimal voiding. As IPC 7093 specification acknowledges, one of the key concerns with bottom termination components (BTC) such as QFNs is achieving the solder volume required for a high-reliability solder joint^[2]. A multitude of processing factors such as reflow profile, reflow atmosphere, pad finish, and stencil design have been assessed in this study to develop a solution for achieving a high-reliability solder joint with low voiding for QFN packages.

Experimental Procedure

A full factorial DOE was designed based on key factors contributing to voiding under bottom termination components. The use of a solder preform was investigated compared to a solder paste only benchmark sample. The key factors in this DOE were identified and selected by subject matter experts from a leader in semi-conductor manufacturing, an OEM of specialized test and measurement equipment for radio communications, and a solder manufacturer.

A custom single layer 1.6 mm PCB test vehicle was designed specifically for this investigation that encompassed numerous variables

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Figure 1: Image of the PCB test vehicle and some of the components used in this DOE.

Type	Pin	ID	# of Comp. per TV	Exposed Ground Pad (LxW, mm)
QFN	32	QFN 32	18	3.6x3.6
QFN	20	LCS 20	18	2.1x2.1
QFN	48	LCS 48	18	5.4x5.4

Table 1: Component details.

that can contribute to voiding in bottom termination components. A single-layer PCB design (Figure 1) was chosen so that other factors (i.e., multilayer board and ground planes) would not influence the key factors being addressed in this study. QFN components of various sizes and pin configurations were among the variables addressed and further defined. In this study, only QFN components were selected (Table 1).

There were two types of test boards generated: one with an immersion tin (ImmSn) plating, which is widely used in automotive application and another with an immersion silver (ImmAg) plating, which is used in high-reliability and high-power application.

The test board also addressed via design including through hole via, no via, and plugged via configurations under the QFN and LCS components. The through hole via had a 0.3 mm diameter with and 0.5 mm diameter

ter resist on top and bottom. The plugged via maintained the same 0.3 mm diameter hole and depth of 0.4 mm with 0.7 mm diameter resist on top and bottom. Vias were configured in a pattern as indicated in Figure 2.

The investigation also addressed reflow profile and reflow atmosphere. A low voiding SAC305, type 4 solder paste was used for this study with solidus temperature of 217°C and liquidus temperature 220°C. Thermocouples were strategically placed on the QFN32, and QFN64 component locations on the test vehicle. Proven straight ramp and high soak reflow profiles were evaluated as shown in Figure 3.

The straight ramp profile increased at a rate of 1°C/s until reaching liquidus temperature of 220°C. The test vehicle was subjected to 65 seconds above liquidus (TAL) with peak temperature on the test vehicle reaching 240°C. The high-soak reflow profile increased

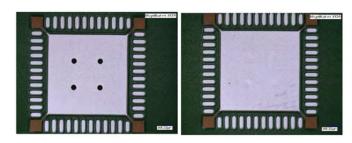
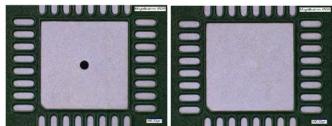
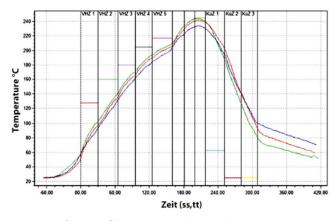


Figure 2: Via design and configuration on the test vehicle.





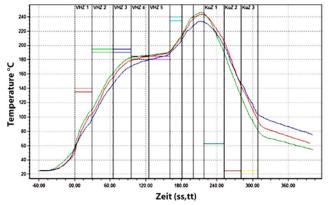


Figure 3: Reflow profiles using in this study.

temperature at a rate of 1°C/s up to 150°C before slowing to a rate of 0.5°C/s up to 200°C to allow more time for the flux to activate the surfaces.

The high-soak profile subjected the test vehicle to 50 seconds above liquidus (220°C) with a peak temperature of 240°C on the test vehicle. Finally, both air and nitrogen reflow atmospheres were evaluated in this investigation to further understand the effect of voiding under bottom termination components.

The focus of the investigation involved the use of the micro-flux coated solder preform to increase solder volume relative to fluxing agent and reduce voiding. The use of a SAC305 microflux coated solder preform in conjunction with paste was benchmarked against a solder paste only test vehicle for each of the configurations summarized in Table 2. Four replicate boards of each iteration were processed to ensure statistically viable data.

ID	PCB finish	Reflow Profile	Atmosphere
1	ImmSn	High Soak	Air
2		High Soak	Nitrogen
3		St. Ramp	Air
4		St. Ramp	Nitrogen
5	ImmAg	High Soak	Air
6		High Soak	Nitrogen
7		St. Ramp	Air
8		St. Ramp	Nitrogen

Table 2: Assemblies' configuration details.

Close to 2,000 data points were generated combining 54 components on each test vehicle and four replicates of each configuration. The solder paste only benchmark samples were printed in a window pane configuration commonly used in the industry for void reduction and shown in Figure 4.

The design of a solder preforms to allow intimate contact with the thermal pad of the component and increase solder volume played a significant role in the results presented in this investigation. Figure 5 represents an example of the use of solder paste only in window pane format on a QFN where mechanical stack-up

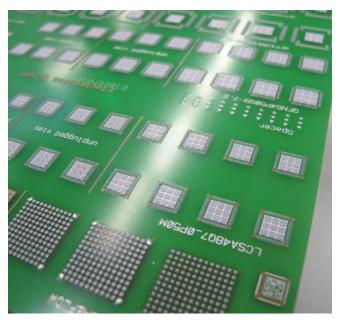


Figure 4: Solder paste print configuration. (Examples of window pane solder prints on QFN components used in benchmark samples.)

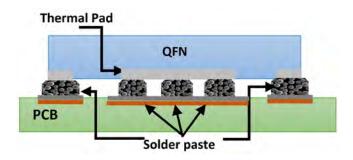


Figure 5: Solder paste print design for QFN.

issues on the component and reflow characteristics of solder paste make it difficult to achieve good voiding.

Trials were conducted using a fully automated in-line system. Use of such a worldclass facility helped to maintain control and ensure consistent process repeatability among test vehicles. A production printer was used to print 5 mil paste layouts on both the solder paste only and solder paste and preform configurations under investigation. Paste was printed at a 65° squeegee angle at a rate of 30 mm/s and 80N pressure using a 5 mil stencil. Components and solder preforms were placed from tape and reel using a production component placement machine with twin-head and 2N force. Samples were then inspected for skew prior to reflow in a production belt driven reflow oven per the reflow profiles

defined in Figure 3. Finally, upon reflow, every component was subjected to X-ray voiding analysis capturing its largest single void size and total void percent under the thermal pad.

Results and Discussion

Voiding analysis was performed on all test assemblies. Statistical software was used to compare voiding performance and processing factors to generate a main effect plot to understand QFN voiding. The plot of the main effects on the voiding of the built

assemblies are shown in Figure 6. Reviewing data, it was observed that no significant difference was observed between the two surface finishes (ImmSn and ImmAg) evaluated in this study. A very small effect of the reflow profile type was observed when all data was analyzed. As expected, the lower voiding percentage was achieved with a high soak reflow profile compare to the straight ramp. Typically, higher soak profile allows more outgassing of volatiles during reflow, which could result in lower voiding. Reflow in nitrogen atmosphere resulted in lower voiding. Higher voiding levels were observed on the larger QFN component with thermal pad 5.4 x 5.4 mm. The results for the small and medium sized LCS and QFN packages were similar even though components' thermal pads were very different (3.6 x 3.6 mm and 2.1 x 2.1 mm). Assemblies without vias and with through hole vias produced the least amount of voiding overall; whereas, plugged vias showed higher voiding level. The biggest effect contributing to the reduction in voiding was the use of the solder paste and preform (PF + paste) configuration versus solder paste only (SPO) configuration.

The solder paste only configuration was used as a benchmarking factor for the remainder of the analysis. The average voiding for the contributing factors for SPO configuration

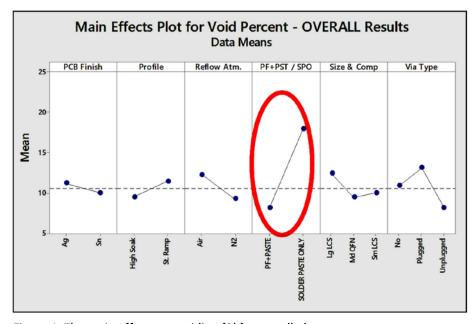


Figure 6: The main effects on voiding (%) - overall plot.

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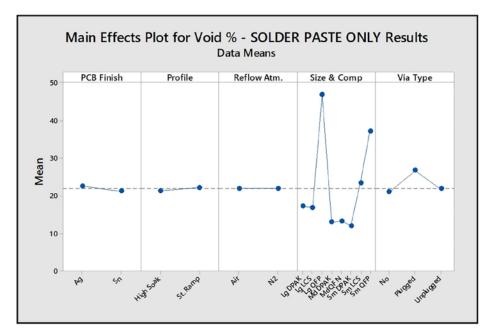


Figure 7: The main effects for SPO configuration.

shown in Figure 7. The resultant voiding was approximately in 22% average range.

ImmSn board finish and the high soak profile marginally drove to lesser voiding. Reflow atmosphere had very little impact on the voiding results overall. Unplugged vias were the most problematic of the three vias design in this study.

Focusing on the results for PF + paste configuration only, an average voiding of 9% was measured. The overall average voiding for

PF + paste configuration was more than two times lower relative to the SPO configuration. **Figure** shows the main effect of various parameters on the voiding of the PF+Paste configuration. Unlike the SPO configuration, the primary contributor to voiding in the PF+Paste configuration was reflow atmosphere. Reflow in nitrogen reduces voiding nearly to 5%. Clear correlation with component size and voiding performance was observed. Voiding levels of about 12%

were observed on the OFN component larger with thermal pad 5.4 x 5.4 mm. Reduction in the size of the thermal pad down to 3.6 x 3.6 mm reduced voiding level down to around 9%. As expected, smallest package with the thermal pad of $2.1 \times 2.1 \text{ mm}$ showed the lowest voiding level and it was about 5%. Like SPO configuration, assemblies with unplugged vias were the most problematic and produced higher voiding levels compared to another pad design.

Earlier conducted studies were undertaken to understand the effects of micro-flux coated solder preforms and voiding for bottom termination components (BTC). In the last several years a lot of advancement was achieved in flux chemistry development to improve voiding performance significantly. In the previous voiding studies^[3,4] it was identified that the higher preform-to-paste volume ratio on the pad contributed to lower voiding, specifically in nitrogen. It is evident that the increased

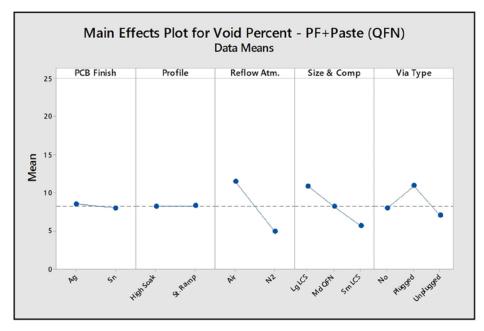
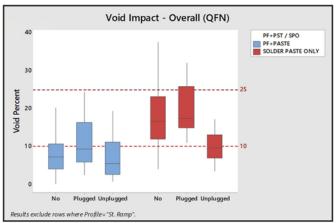


Figure 8: The main effects for PF+paste configuration.



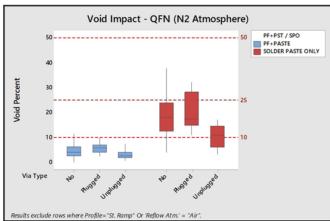


Figure 9: The overall void results of QFN packages.

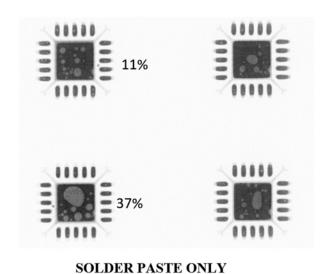
solder volume from the preforms plays a critical role in void reduction.

Voiding of QFN Packages (Small, Medium and Large Pads) Results

A QFN is a bottom termination component in which both thermal pad and signal leads terminate under the body of the component. Figure 9 summarizes the results of the voiding of those components based on the combination of PF+paste and SPO configuration as well as types of vias on the board. The PF + paste configuration with no vias or unplugged vias provide excellent voiding results below 5%. Plugged vias had slightly higher voiding but remained lower than SPO configuration. The PF + paste configuration reflowed in nitrogen environment produced the most impressive voiding results, averaging between 5–10% under all three package sizes.

It was observed during X-ray analysis that assemblies built with PF + paste configuration had a greater consistency in voiding and pad coverage from one component to another. Void distribution was much tighter for the PF + paste configurations compared to SPO configuration. Those differences could be clearly observed in Figure 10.

In the SPO example, a wider distribution of voids was present in which voiding between 11% and 37% was present on the same board for like components in similar board locations. As evident in Figure 10, a greater consistency void percent was achieved for the same situation when a micro-flux preform was used. This consistency will result in a reduction in defect



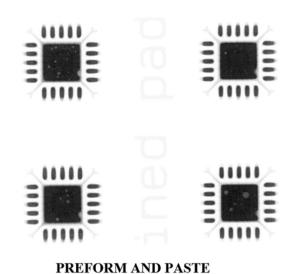


Figure 10: X-ray images of the QFN components assemblies built with different solder material configurations.

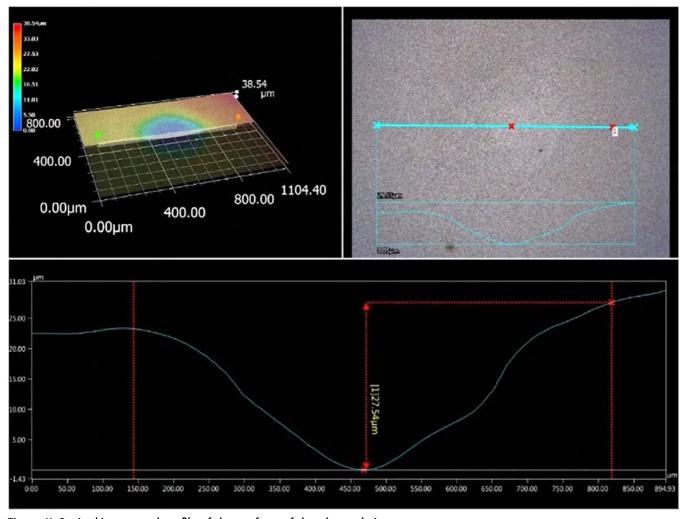


Figure 11: Optical image and profile of the surface of the plugged via.

rate and would eliminate the need for assembly rework.

Another focus of the analysis was evaluating the influence of the via design on to the void percentage. The complexity and functionality of the boards' vias in a PCB are important components. In this study two types of vias were evaluated: (1) through hole vias and (2) plugged vias. All vias were 0.3 mm diameter. Plugged vias were 0.3 mm diameter through hole vias with 0.5 mm diameter resist on top and bottom. Figure 11 shows the optical profile of the plugged via. It appears that resist had some curvature (depression), which could contribute to increased voiding due to air entrapment.

Solder material selection is an important factor when setting up a process for QFN or any other BTC. Voiding is a problem for

bottom termination components, especially for QFN packages that have a thermal pad to conduct heat away from the integrated circuit (IC). Excess voiding will increase the thermal resistance of the thermal interface. It is common practice to design pad and vias to increase propensity for volatiles to escape during reflow process to minimize voiding under the BTC. X-ray images of the assemblies built with SPO and PF + paste configurations are shown in Figure 12. Again, the same consistency between voiding of the assemblies was observed when PF+paste was examined. For plugged vias, voiding was observed around vias. As it was stated earlier, curvature in the solder resist might be contributing factor in higher voiding in the via area. Much lower and smaller voids were observed with PF + paste configuration.

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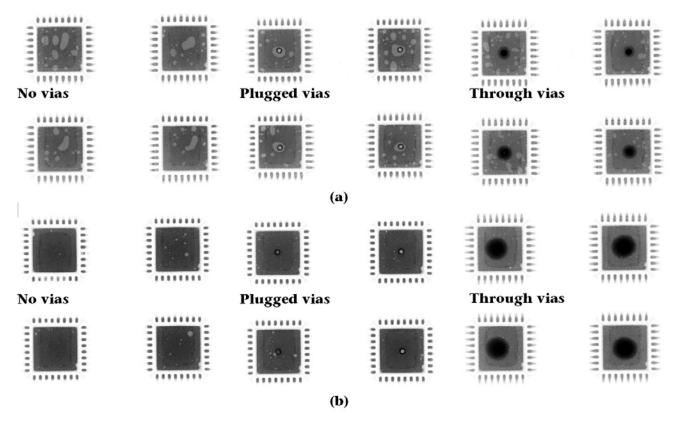


Figure 12: X-ray images of different via design the medium QFN components assemblies built with (a) SPO and (b) PF+paste with different via design.

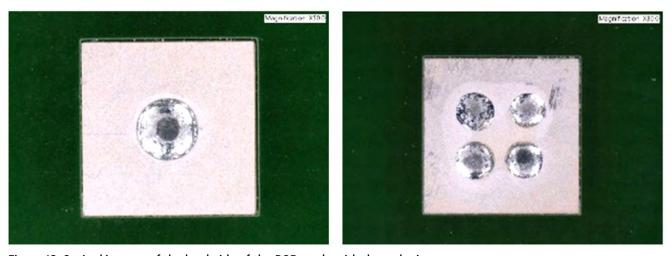


Figure 13: Optical images of the backside of the PCB, pads with through vias.

In all cases when through-hole or unplugged vias were assessed, solder overfills the hole leading to the bumps on the bottom of the board (Figure 13). This uncontrolled solder wicking could result in insufficient thermal connection between PCB and heat sink. Reduced via diameter could limit the amount of solder wicking. With smaller vias, the surface tension of the

liquid solder inside the via could oppose gravity and minimize solder wicking. However, the reduction in via diameter will result in higher overall thermal resistance, which could be one of the downsides of this approach.

In the case of the 5.4 x 5.4 mm thermal pad, 48-pin component, board was designed with four vias per pad. Results similar to the

single via design was observed (Figure 14). Most of the voids on filled via pads were on the top of the vias. Void percent in the pads with unfilled vias were lower but based on the X-ray and optical analysis, solder wicking to the bottom of the board was observed in all cases. Joints with filled vias demonstrated larger and more frequent voids.

Some of the assemblies were metallograph-

ically prepared for microstructural evaluation. Interfacial reaction between the component thermal pad and solder as well as solder and board pad were examined. Uniform and continuous intermetallic compound (IMC) layer was formed at all interfaces, acceptable solder joints were built using both configurations (SPO and PF + paste). SEM images of the cross-sectioned assemblies are shown in Figure 15.

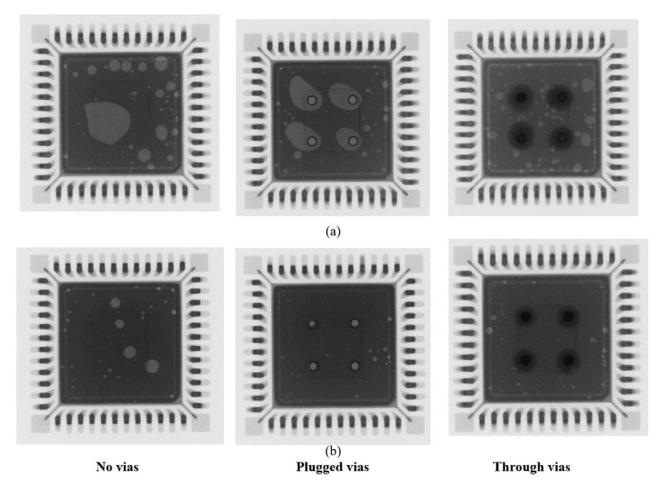


Figure 14: X-ray images of different via design the larger QFN components assemblies built with (a) solder paste only and (b) PF+paste with different via design.

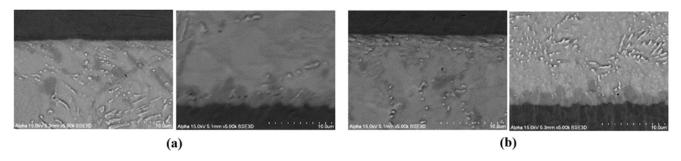


Figure 15: SEM images of the interfacial reaction of the assemblies built using (a) SPO and (b) PF+paste configuration.

Summary and Conclusions

The previous work and the work presented in this study, demonstrates the advancement of QFN and other BTC assembly using low voiding micro-flux solder preform and optimized process parameters such as stencil design, pad design and reflow parameters.

Design of the preform, selecting specific flux amount, and optimizing soldering conditions resulted in significant reduction in voiding.

Design of the preform, selecting specific flux amount, and optimizing soldering conditions resulted in significant reduction in voiding. For various component sizes, consistent sub-10% voiding was achieved. The use of preforms in conjunction with micro-flux coating technology ensures low voiding in both air and nitrogen reflow environments. Reduction in solder paste volume and controlled amount of the flux on the micro-flux preform generates low residue and ensures high electrochemical reliability of the BTC. Low voiding micro-flux technology is compatible with finishes such as immersion Sn and immersion Ag commonly used in industry. Via design is an important factor in BTC assembly. Via type and diameter could be a critical factor to achieve low voiding and reliable solder assembly. SMT007

Acknowledgement

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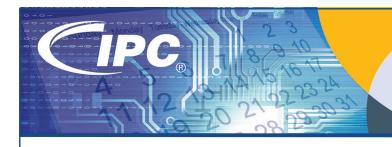


Anna Lifton is R&D manager at Alpha Assembly Solutions.



Paul Salerno is the global portfolio manager for SMT assembly solutions at Alpha Assembly Solutions.

Oscar Khaselev is the R&D director at Alpha Assembly Solutions (no image available).



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Evaluating the Impact of Powder Size and Stencils on Solder Paste Transfer Efficiency



Abstract

Building upon an earlier study which focused on solder paste powder size, room-temperature aging and PCB pad and aperture designs, this study continues to investigate powder mesh size, but also examines stencil surface treatments and stencil foil tension. The goal of the study was to identify and rank the variables that provided the most improvement in repeatability, transfer efficiency and print definition for fine pitch printing. The results showed that nanocoating, powder type and tension rank highest to lowest in terms of their effect on print quality, and that high tension should be further studied to better understand where it makes the most significant impact.

Introduction

Previous work [1] revealed that:

- a. reducing solder powder mesh size provides a modest improvement in print consistency and transfer efficiency for certain aperture designs
- b. reducing solder powder mesh size may



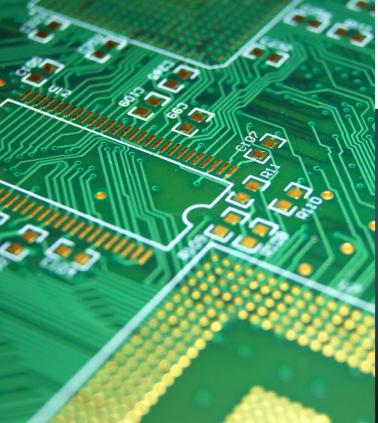
- reduce solder paste useful life and increase process variables under certain conditions
- c. pad and aperture design are the most significant variables in improving solder paste transfer efficiency when using high-quality, nanocoated stencils at standard mounting tensions

This study adds to the database the effect of nanocoating and mounting tension on print quality, bringing a new arm to the experiment by printing unaged Type 4 (T4) and Type 5 (T5) solder pastes with similar stencils; however, one stencil is coated with a commercial polymer nanocoating and the other is uncoated and mounted at high tension. For reference, "standard" mounting tension is about 35N/cm, whereas "high" tension is 50N/cm or higher. Theoretically, higher mounting tension should create Smore precise deposits because the foil will not deflect or reverberate as much during the separation phase of the printing process compared to a lower tension foil.

Experimental Method

Test Vehicle

The test vehicle (TV) selected for the print study was the Jabil Solder Paste Evaluation













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Board 2 that is commercially available from a leading dummy component and test kit supplier. The TV shown in Figure 1 provided an exceptionally thorough and detailed analysis in our earlier study and was used again in this study to provide continuity in data collection and analysis.

Features included:

- Print-to-fail (PTF) patterns with combined pad sizes ranging from 3 to 15mils with shapes including circular, square and rectangular pads, defined with both copper (NSMD) and solder mask (SMD)
- 0.4 and 0.5 mm BGA patterns.
- Markings on the PCB are etched in copper rather than silkscreened with ink to eliminate the standoff effect of PCB nomenclature

The smallest feature size printed in this study was 6 mil (150 µm) which produces an area ratio of 0.38 using a 4 mil (100 µm) stencil. The smallest feature size reported is 8 mil (200 µm), as the variation increases dramatically below this threshold, due in part to the low ARs and in part to measurement error. The TV used in this arm of testing was from the same production lot that was used in the previous study. The data was collected using a new panel for each print. No PCBs were cleaned and reprinted.

The pad and aperture sizes, area ratios and theoretical volumes are shown in Table 1.

PTF	Slump	0.4BGA 0.5BGA
	10:10:10	

Figure 1: Jabil solder paste evaluation board.

Pad size (mil)	Area	Ap Vol	Ap Vol
Pau Size (IIIII)	Ratio	Circle	Square
6	0.38	113	144
7	0.44	154	196
8	0.5	201	256
9	0.56	254	324
10	0.63	314	400
11	0.69	380	484
12	0.75	452	576
13	0.81	531	676
14	0.88	616	784
15	0.94	707	900
0.4mm BGA	0.63	(sq with rnd	383
0.5mm BGA	0.73	corners)	531

Table 1: Pad sizes, area ratios and theoretical aperture volumes for 4mil (100µm) foil.

Stencils

The stencils employed current state-of-theart technology which would typically be used for the fine feature applications that demand finer powder solder pastes. They were cut from pre-mounted name-brand stainless steel on a modern, diode laser by a high-quality, US-based stencil supplier. One stencil foil was pre-mounted at high tension; the other at standard. The stencil supplier then applied a proprietary polymer nanocoating to the standard tension stencil. The SPI results from each stencil were compared to those in the existing

> database from the previous study. All apertures were sized one to one (1:1) with the test pads, with no reductions on any apertures.

Laboratory Equipment & Print Parameters

The test equipment included a DEK Horizon screen printer, Parmi Sigma X SPI machine and ASH video microscope in the AIM Applications Laboratory located Juarez, Mexico. The test



Figure 2: AIM applications laboratory manager reviews test setup.

area is climate controlled and can be manipulated to simulate production environments around the globe. Test conditions were optimized at 25.4°C (77.4°F) at 59% RH for these tests and recorded twice daily.

The facility is staffed with full-time SMTAcertified process engineers with over 50 years of combined experience in SMT assembly processes. Figure 2 shows the laboratory manager preparing the DEK Horizon printer and Parmi Sigma X SPI machine for the test run. The print parameters were as follows:

- Squeegee: 14" (355 mm) 60° angle DEK OEM
- Squeegee speed: 40 mm/sec (~ 1.6 in/sec)
- Squeegee pressure: 10 kg (~1.5 lb./in on 14" blades)
- Separation speed: 1 mm/sec (~0.040 in/sec)
- Separation distance: 3 mm (~120 mils)
- Under wipe sequence: Wet-Vacuum-Dry (WVD), using DEK EcoRoll wiper paper and AIM DJAW-10 solvent. Stencils were automatically underwiped before the first print of each set of five.

A dedicated flat tooling support block was used to provide solid support for the PCB, and new squeegee blades were used for the tests.

Automatic Solder Paste Inspection

inspection parameters were modified to improve the accuracy of the measurements. Typically, a 30-40 um measurement threshold is used in production environments to eliminate topographical noise from PCBs' features like silkscreen markings, mask over trace, etc. Because the design of this TV limits topographical feature noise, it enabled a 15 µm measurement threshold, to improve measurement fidelity and aid in detecting subtle variations in print behavior.

Solder Paste

The solder paste tested included Types 4 and 5 in a modern, no-clean flux medium. The pastes were blended,

shipped and stored under recommended conditions. The same metal percentage was used for the T4 (88.5%) and T5 (88.3%) as in earlier tests; however, different lots of solder powder and flux medium were used in this test.

Experimental Design

Input variables in the experiment included:

- Paste Type (4, 5)
- Stencil nanocoating (Y/N)
- Foil mounting tension (std/high)
- Pause time between print tests (0, 30, 60 and 90 minutes)
- PCB pad size (6-15mil)
- PCB pad shape (circular, square, modified square with rounded corners)
- PCB pad definition (NSMD, SMD)

Output variables included:

- Deposit volume
- Deposit height
- Transfer efficiency (% volume). TE is based on theoretical aperture sizes, not measured aperture sizes. All the stencils were cut from the same material on the same cutter by the same operator, so it is assumed that any systemic error is applied equally to all stencils. Actual aperture sizes were not measured

Statistics calculated from the output readings included:

- Means (or averages)
- Standard deviations
- Coefficients of variation (CV, or the standard deviation divided by the mean and expressed as a percentage). CV is preferred over Cpk when comparing different SPI datasets because it normalizes the variation with respect to the mean without the influence of control limits
- Using generally accepted industry practices, the acceptability criterion was TE at least 80% of theoretical aperture volume and a CV of less than 10%

Stencil under wipes were performed before each set of five prints, but not between prints. SPI readings were taken immediately after each print. The full runs that included 0, 30-, 60- and 90-minute pauses took approximately four hours from start to finish.

The tests were nested as follows:

Time 0

- 1. Install stencil and squeegees
- 2. Stir solder paste and apply to stencil
- 3. Print 5 boards
- 4. Start timer for 30 minutes
- 5. Remove stencil and squeegees, leave paste on stencil

Tension	Refriger- ation	Powder Size	Time	Board #	Board Label	SPI File Name
		Type 4	0	1	SF4-T0-#21	
				2	SF4-T0-#22	
چ				3	SF4-T0-#23	SF4-T0-bd 1-5
es				4	SF4-T0-#24	
Ĕ				5	SF4-T0-#25	
			30	1	SF4-T30-#26	
<u> </u>	Fresh			2	SF4-T30-#27	
\mathbf{a}				3	SF4-T30-#28	SF4-T30-bd 6-10
				4	SF4-T30-#29	
Ę				5	SF4-T30-#30	
.∺			60	1	SF4-T60-#31	
Z Z				2	SF4-T60-#32	
O				3	SF4-T60-#33	SF4-T60-bd 11-15
<u> </u>				4	SF4-T60-#34	
<u></u>				5	SF4-T60-#35	
Normal Tension (Poly mesh)			90	1	SF4-T90-#36	
Z				2	SF4-T90-#37	
ž				3	SF4-T90-#38	SF4-T90-bd 16-20
				4	SF4-T90-#39	
				5	SF4-T90-#40	

Table 2: Data management spreadsheet.

At 30-minute mark on timer run WVD wipe

- 1. Print 5 boards
- 2. Start timer for 60 minutes
- 3. Remove stencil and squeegees, install stencil and squeegees
- 4. At 30-minute mark on timer, run WVD
- 5. Print 5 boards

At 60-minute mark run WVD wipe

- 1. Print 5 boards
- 2. Start timer for 90 minutes
- 3. Remove stencil and squeegees, install "A" stencil and squeegees
- 4. At 60-minute mark on timer run WVD wipe
- 5. Print 5 boards

At 90-minute mark on timer "F" run WVD wipe

- 1. Print 5 boards
- 2. Start timer for 120 minutes
- 3. Remove stencil and squeegees, install stencil and squeegees
- 4. At 90-minute mark on timer, run WVD wipe
- 5. Print 5 boards
- 6. Remove stencil and squeegees

Table 2 shows the data management worksheet that indicates variable, run order, board labeling and SPI file tracking information.

Results and Discussion

There is myriad facets to consider when analyzing the collected data. To streamline the analysis:

- 1. data has been compartmentalized by component type or padstack
- 2. only best- and worst-case scenarios are reviewed
- 3. paste transfer quality is interpreted with respect to the main input variables of nanocoating, paste particle size, and foil tensioning

BGAs

0.4 and 0.5 mm BGA apertures are the first features considered, as these devices are becom-

Paste Transfer - 0.5mm BGA

Types 4 and 5 Powder

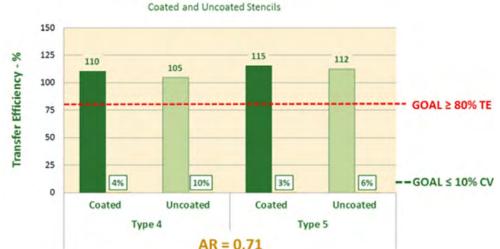


Figure 3: Print performance of Types 4 and 5 powder with 0.5 mm BGA.

Paste Transfer - 0.4mm BGA

Types 4 and 5 Powder Coated and Uncoated Stencils 150 125 Transfer Efficiency - % 110 111 109 97 100 GOAL ≥ 80% TE 75 50 25 5% 10% 4% 7% -GOAL ≤ 10% CV

Coated

Type 5

Uncoated

Figure 4: Print performance of Types 4 and 5 powder with 0.4 mm BGA.

AR = 0.62

Uncoated

ing common to the industry and are a frequent print challenge for mainstream PBC assemblers. The test vehicle's area ratios are 0.71 for 0.5 mm BGA and 0.62 for 0.4 mm BGA. These are at either side of the threshold of recommended guidelines of 0.66 AR, which has historically been cited as the lowest AR that should be considered when printing T3 solder paste. T3 was not included in this test because T4 is quickly becoming the industry standard it is usually readily available. T5 was also tested, as it is often requested by assemblers who

0

Coated

Type 4

perceive smaller powder size as a fast and easy improvement to a fine pitch printing process. T5 paste indeed brings some print advantages, but also carries with it some inherent disadvantages. Procuring T5 paste can present supply chain challenges and it can increase variability in paste print and reflow performance over time due to the higher surface area: volume ratio.

Figures 3 and 4 shows the Transfer Efficiency (TE), or the percentage of theoretical aperture volume that was deposited and the associated Coefficients of Variation (CVs) for the

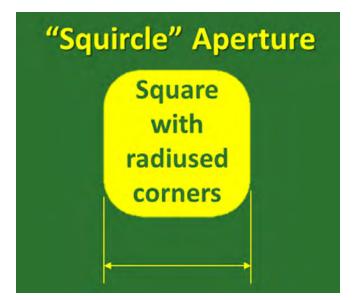


Figure 5: "Squircle" aperture design for BGAs offers optimized solder paste release by minimizing paste sticking in corners.

0.5 mm and 0.4 mm BGAs. Each data point on the 0.5 mm chart represents the average of 3780 deposit readings—84 I/Os per device, 3 devices per board, three boards per panel and five panels per test. Each data point on the 0.4 mm BGA chart represents 16,200 measurements, as the same number of devices have 360 I/Os each. This quantity of data generates high confidence in the results.

Notice the TEs are all slightly higher than 100%. This is not uncommon and can be due to numerous factors relating to gasketing breaches and/or paste pump out due to the 1:1 aperture:pad ratio and the combination of round pad with squircle aperture (Figure 5) [3]. The pads on this device are NSMD (labeled "copper" in our study), and, given this method of definition, shape differences naturally lend themselves to gasketing issues, and the 1:1 aperture:pad ratio in general is highly susceptible to positional errors in the stencil or PCB, alignment error in the printer, or slightly undersized pads or oversized apertures.

Figures 3 and 4 show that that all the print results were within our prescribed limits of ≥80% TE and ≤10% CV for both T4 and T5 pastes and coated and uncoated stencils. Comparing the results of T4 and T5, T5 gives very little advantage over T4, with the one

slight exception being uncoated stencils on 0.4 mm BGAs with an AR of 0.62.

More striking than the powder size comparison is the impact of coated stencils on print consistency. In every case, the coated stencil deposited similar or greater amounts of solder paste with half the variation. Cutting CV by half is a profound improvement in process control.

To the printing specialist, this data should facilitate the decision between finer powder and nanocoating as means to improve release and the overall solder paste printing process. Nanocoating has a significantly more positive effect on both increasing TE and, most importantly, reducing CV.

Print-To-Fail

The next area of focus is the TV 'Print to Fail' (PTF) patterns. The PTF patterns combine pad sizes ranging from 6 to 15 mils with shapes including circular, square and rectangular pads, defined with both copper (SMD) and solder mask (NSMD). Each data point represents 480 measurements for each PTF configuration. Figure 6 illustrates the advantage of SMD defined pads towards improving print



Figures 6a and b: SMD pads (top) produce more consistent prints than NSMD pads (bottom).

Paste Transfer - Best Case Scenario

Square, Mask Defined Pads and Apertures

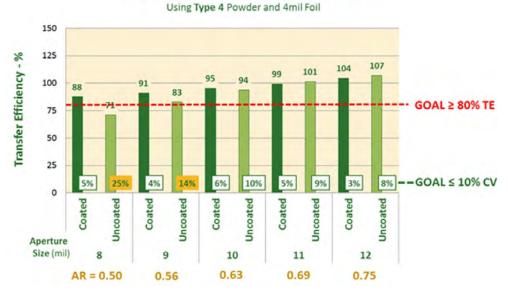


Figure 7: Print performance of Type 4 powder with best-case scenario pad design.

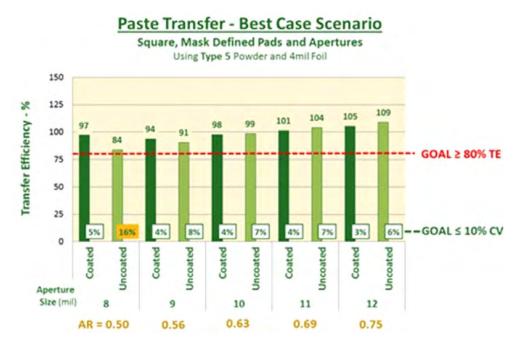


Figure 8: Print performance of Type 5 powder with best-case scenario pad design.

consistency and reducing the coefficient of variation.

The data generated in this arm of the study echoes the findings of the previous DOE in that that best quality prints were produced on square and solder mask-defined pads, whereas the worst prints were produced on circular, non-solder mask-defined pads (aka copper defined pads). In between the extremes

are mask-defined circular pads and copperdefined square pads. For the sake of brevity, the two middling conditions are not reported; rather, the best-case scenarios are presented, and the worst-case scenarios are explored in greater depth.

Figures 7 and 8 represent the best-case scenario for achieving quality print results. It combines SMD test pads with square apertures with a coated and uncoated stencil using T4 solder paste at Time 0.

Figure 7 shows that once the area ratios drop below 0.63 the limitations of the uncoated stencil are apparent as the CV falls below the prescribed 10% and TE is only border line at 0.56 AR. However, the nanocoated stencil exceeds the benchmark as low as an AR of 0.50, or an 8mil aperture in a 4mil foil. These figures represent a very robust and repeatable print process.

Figure 8 shows the test results for the T5 solder paste, using the same best-case scenario of square, mask defined pads at Time 0. The trends established by the nanocoated stencil are repeated with the T5 paste in that it meets the acceptability criteria all the way down to the 0.5 AR. On the uncoated stencil, the T5 paste does offer some improvements in overall transfer efficiency and on coefficient of variation on AR of less than 0.63, but only meets the acceptability criteria at 0.56 AR. In other words, the T5 paste can bring some process improvement, but not at the same level as the nanocoating.

It is noteworthy that the measurement threshold on the SPI equipment was lowered to 15 μ m in the laboratory, rather than 40 μ m, which is the typical threshold in production

environments. The process improvements documented within this study may not be as perceptible when testing using production inspection parameters.

Figures 9 and 10 represent the worst-case scenario—circular, copper-defined pads—at Time 0 with Type 4 and Type 5 pastes, respectively. As detailed in the previous study, circular apertures have lower volume as opposed to square apertures and generally poorer release characteristics. It is believed that the circular apertures exhibit inferior release characteristics due to equal surface tension of the solder paste around the apertures' periphery. Square apertures have unequal forces acting on the solder paste/stencil wall interface, which helps facilitate paste release.

As is plainly demonstrated in Figure 9 the release characteristics of an uncoated stencil with sub-optimal conditions are simply unacceptable. An AR of 0.69, which is considered easily accomplished, cannot be repeatedly printed with an uncoated stencil in this scenario. It is important to emphasize that the apertures are 1:1 with specified pad size, and small pad sizes are commonly over-etched, resulting in smaller pads and poor gasketing. The nanocoated stencil, however, again produced acceptable prints all the way down to the 0.56 AR.



Figure 9: Print performance of Type 4 powder with worst-case scenario pad design.



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Paste Transfer - Worst Case Scenario

Circular, Copper Defined Pads and Apertures
Using Type 5 Powder and 4mil Foil



Figure 10: Print performance of Type 5 powder with worst-case scenario pad design.

In Figure 10, T5 solder paste is replaced by T4 and again, the trend continues, but demonstrates a more considerable impact of the reduced powder size. On an uncoated stencil the T5 solder paste produced acceptable volumes but unacceptable variation at 0.56 AR, and acceptable volumes and CVs obtained at 0.63 AR. The nanocoated stencil, however, produced acceptable prints with the T5 paste with AR as low as 0.50 even in the worst-case scenario of circular, copperdefined pads.

It should be noted that the metal percentage by weight was lowered slightly from 88.5% in the T4 to 88.3% in the T5 to minimize solder powder "packing" during print, resulting in slightly lower viscosity paste. It is possible that the advantage of T5 was a combined effect of both the reduction in mesh size and formulation modifications.

Peaking

Peaking, or the tendency of the solder paste to stretch and snap during release, creates pointed deposits rather than flat top deposits Figure 12. Pointed deposits are undesirable because they can be the root cause of solder bridging. To check the stencil-solder paste release relationship, the heights of the rectangular PTH patterns were analyzed. Rectangles were chosen because they offer two opportunities per deposit to peak, or "dog ear," and the effect of peaking would be more pronounced in the SPI readings than similar measurements on square or circular pads with only one opportunity.

Figure 11 shows the average measured height of the mask-defined rectangles for the various pad widths. In this case, with T4 solder paste, the average heights of the deposits are 0.6-0.7 mils higher than those of the coated stencils. T5 paste showed somewhat less peaking, partially closing the gap between coated and uncoated stencils with differentials between 0.4 and 0.5 mils. Copper-defined pads showed even less peaking, with T4 showing a range of 0.3 to 0.4 mils, and the T5 showing a range of 0.2-0.3 mils. The trend was consistent for all pad and powder type combinations: uncoated stencils created greater peaks and dog ears than the coated stencils.

In addition to the lower peaking, coated stencils also showed less variation in height than uncoated, cutting it by half or more, and

Effect of Nanocoating on Peaking

Average Heights of Mask-Defined Rectangles Using Type 4 Paste and 4mil foil



Figure 11: Average heights of rectangular deposits.

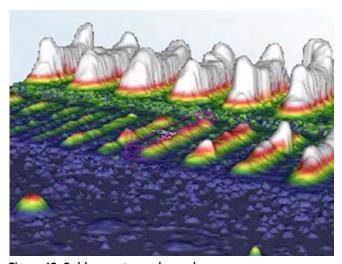


Figure 12: Solder paste peaks or dog ears.

indicating more consistent release and better process control.

Figure 12 shows an example of dog ears from the SPI machine.

Foil Mounting Tension

The final variable analyzed is one of the latest stencil innovations that promise to help improve print quality: the tension of the foil mounted in the frame. As previously mentioned, standard stencil tension is typically 35-40 N/cm and high tension $\sim 50 + \text{N/cm}$.

The concept is that when mounted with higher tension, the foil will provide a more stable print platform with less deflection or reverberation and produce better results. High tension foils require reinforced mesh and frames to withstand in increased forces and justify a cost premium. This experiment tested uncoated stencils at standard and high tensions, with both T4 and T5 solder pastes. Uncoated stencils were used to isolate the effect of tensioning. The stencils were tensioned as foils premounted on their frames before cutting.

The 0.5 and 0.4 mm BGAs were analyzed first. The performance of both stencils, including pause times of 0, 30, 60 and 90 minutes, met the goals of ≥80% TE and ≤10% CV, for both BGAs and both paste sizes. The TEs and CVs were similar for both the high and standard tension foils. Given the unremarkable nature of the BGA tests, the data was further mined to investigate differences for smaller apertures or pause times. In the best-case scenario of square, mask-defined pads, the higher tension demonstrated no distinct advantages, shown in Figure 13. Both tensions printed well down to a 0.62 AR, but just missed the acceptance criteria at 0.56. Type 5 paste opened the window slightly by enabling a 0.56 AR (Figure

Paste Transfer - Standard vs High Tension

Square, Mask-Defined Pads and Apertures (Best Case)

Type 4 solder paste with uncoated stencils

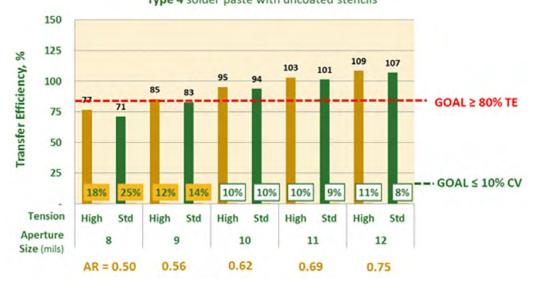


Figure 13: Comparison of effect of foil mounting tension on print quality with Type 4 solder paste and best-case scenario pad design.

Paste Transfer - Standard vs High Tension Square, Mask-Defined Pads and Apertures (Best Case) Type 5 solder paste with uncoated stencils



Figure 14: Comparison of effect of foil mounting tension on print quality with Type 5 solder paste and best-case scenario pad design.

14) and producing borderline results at 0.50, but still showed no considerable difference in TE or CV between the two mounting tensions.

To drill down the absolute worst-case scenarios looking for advantages of higher tension, the T4 and T5 prints on circular, copperdefined pads were examined at Time 0, and T4 prints after the 90-minute pause.

As expected, this combination of variables produced the most unacceptable results. What was somewhat unexpected was the degree of failure as even at an AR of 0.69 (Figure 15), where deposit inconsistency with a standard tension foil was deemed unacceptable.

In Figure 16, T5 powder again helped bring deposit characteristics that were on the border-

Paste Transfer - Standard vs High Tension

Circular, Copper-Defined Pads and Apertures (Worst Case) Type 4 solder paste with uncoated stencils

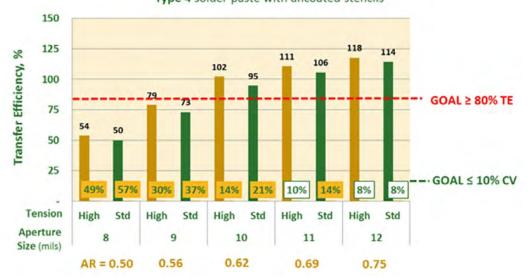
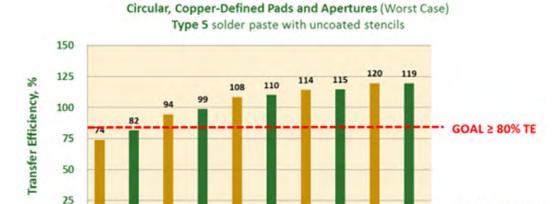


Figure 15: Comparison of effect of foil mounting tension on print quality with Type 4 solder paste and worst-case scenario pad design.



10%

5td

10

0.62

9%

High

8%

Std

11

0.69

7%

High

Std

12

0.75

Paste Transfer - Standard vs High Tension

Figure 16: Comparison of effect of foil mounting tension on print quality with Type 5 solder paste and worst-case scenario pad design.

10%

High

line with T4 paste into compliance with the benchmark for ARs of 0.69 and 0.62, but again, showed very little difference in TE and CV between the standard and high-tension mountings.

38%

High

Std

AR = 0.50

Tension

Aperture

Size (mils)

19%

High

0.56

18%

Std

Finally, going for the absolute worst-case scenario possible—circular, copper-defined pads, with T4 paste after a 90-minute pause—

all the trends remained constant. As seen in Figure 17, the paste release was extremely similar to that of Time 0, with the higher tension stencil showing a very slight potential advantage in TE, and little effect on CV.

Comparing the effects of nanocoating to the effects of high tension, these tests indicate that nanocoating offers far greater benefit than

GOAL ≤ 10% CV

Paste Transfer - Standard vs High Tension

Circular, Copper-Defined Pads and Apertures (Worst Case) - with 90 minute

Type 4 solder paste with uncoated stencils

pause

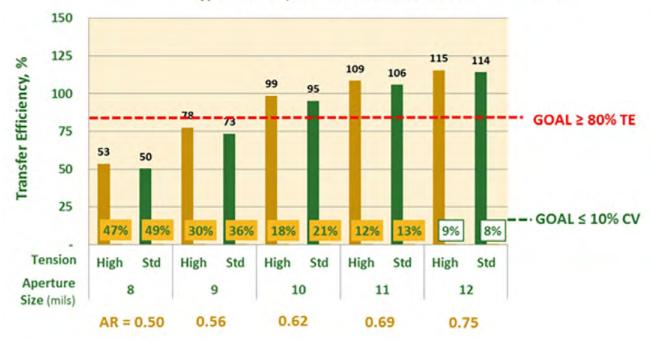


Figure 17: Comparison of effect of foil mounting tension on print quality with Type 4 solder paste and worst-case scenario pad design after 90-minute pause.

high tension. Use of nanocoating also appears to outweigh the effective benefit of using T5 to T4 solder paste, which in turn, appears to have a greater effect than the tension. Therefore, the effects of the studied variables on overall print quality can be ranked from highest to lowest as: nanocoating, powder mesh size, and tension.

It should be noted that, although high tension foil mounting did not show a considerable impact on this test, the test vehicle itself does not have a high aperture density, and the foil is a 4 mil-thick, hard stainless steel. Stencils with higher aperture densities, or thinner or more ductile foils may realize measurable benefit from higher mounting tensions.

It should also be noted that the combination of high tension and nanocoating was not tested. Based on the results of this study, the combination may be tested for statistical analysis, but it is anticipated that the effect of nanocoating will far outweigh the effect of foil mounting tension on this test vehicle.

Conclusions

The solder paste printing process represents the greatest opportunity to introduce defects into the SMT assembly process. Therefore, any technology that can reduce the risk is always worth investigating.

This study demonstrated that the most significant advantages in both transfer efficiency and volume consistency were realized by using nanocoated stencils, particularly as aperture ratios shrink below 0.62. It should be noted that AIM has no commercial interest in stencil or coating technologies; AIM's purpose in investigating the effect of the coatings is simply to provide users with the best possible process recommendations. In most cases, moving from T4 to T5 provided print quality improvements in both transfer and consistency, but the gain was minimal compared to that of the nanocoating.

Nanocoating provided a wider process window than T5 solder paste. Additionally, finer mesh solder powder, such as T5, have

been known to introduce variability to both the print and reflow process due to the increased interaction between the flux medium and solder powder, and smaller mesh sizes often pose increased material cost and availability issues. Therefore, it is recommended that users facing fine pitch printing issues first check their basic process setup, then investigate nanocoating prior to trying T5 solder paste.

The benefit of high tension stencil foil mounting is less clear than the benefits of nanocoating or finer mesh size. Varying performance improvements were witnessed with higher tension, but they were slight and inconsistent. Users of high-aperture density stencils report incremental improvements in print quality in production settings; however, that was not consistently reproduced in this laboratory test.

The benefit of high tension stencil foil mounting is less clear than the benefits of nanocoating or finer mesh size.

The benefit of high tensioning may be better realized with a different stencil design, as the test stencil had relatively low aperture density. Similarly, the test stencil was 4 mil (100µm) thick, whereas a thinner stencil—which would be more prone to deflection—may show more benefit from increased foil tension.

Finally, it should be noted that the data analyzed in this study was produced in a highly controlled laboratory environment, by professional process engineers, using high-resolution measurement techniques. Similar results should not be anticipated in production environments with typical noise and standard SPI measurement techniques. It would be reasonable to expect similar trends in production, but with somewhat lower TEs and somewhat higher CVs. Therefore, the data should not be interpreted as a direct recommendation of print capability

on an assembly line; however, it serves as an excellent basis on which to propose the following guidelines:

- Nano-coated stencils should be used whenever area ratios are lower than 0.66
- T4 mesh powder is well suited to print area ratios as low as 0.50 when nano coating is applied
- High-tension foils may offer slight benefits, but more study needs to be performed

A representative subset of the data is provided within the paper; more details of the extensive analysis are available upon request. SMT007

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Editor's Note: This article was originally published in the proceedings of SMTA International.



Tim O'Neill is the technical marketing manager at AIM Solder.



Carlos Tafoya is the international technical support manager at AIM Solder.

Gustavo Ramirez is a process application manager at AIM Solder (no image available).



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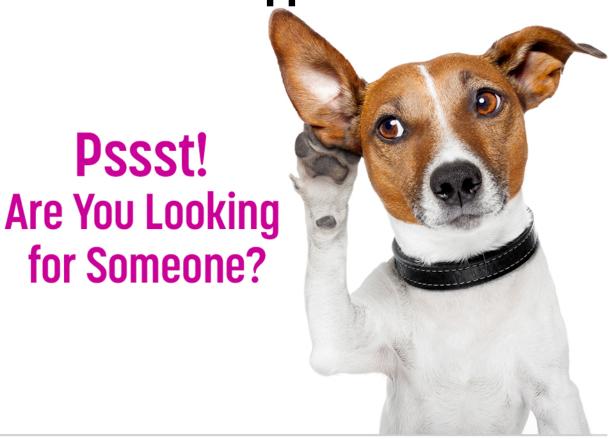
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