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August 2013

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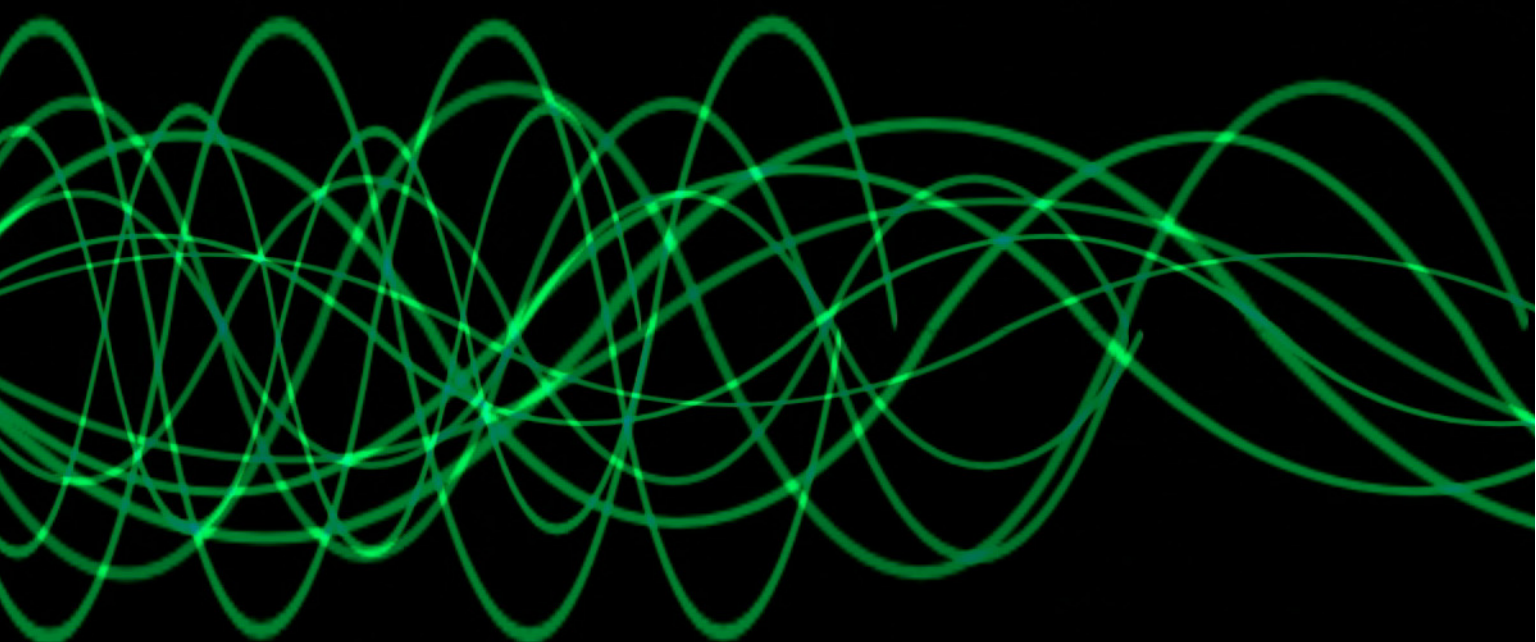
SIGNAL INTEGRITY



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Feature Article of the Month

Differential Signal Design (Part 1)

by Lee Ritchey

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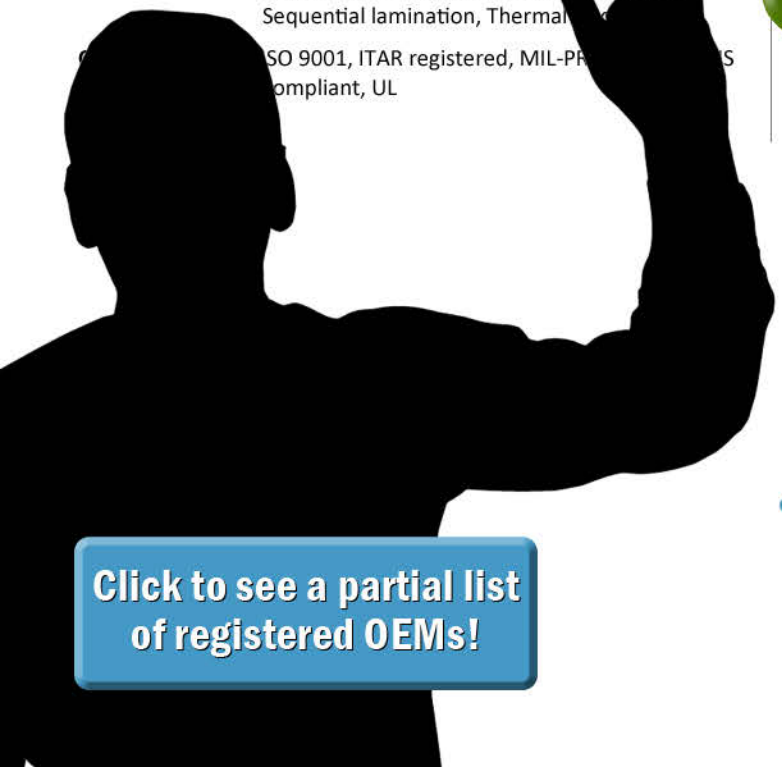

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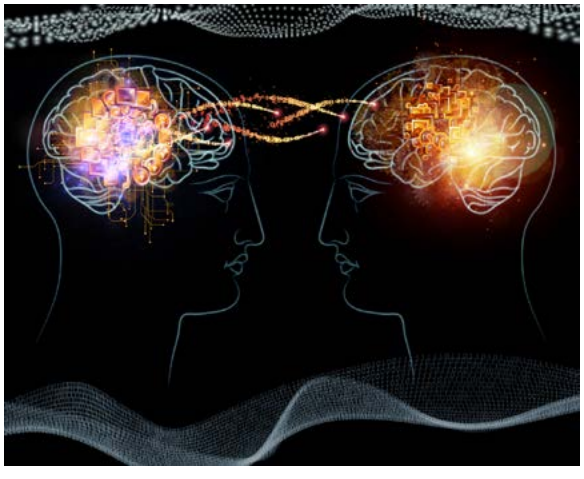
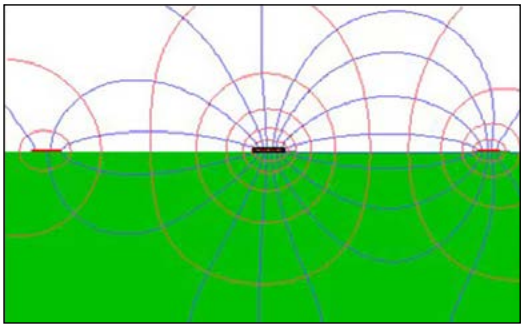
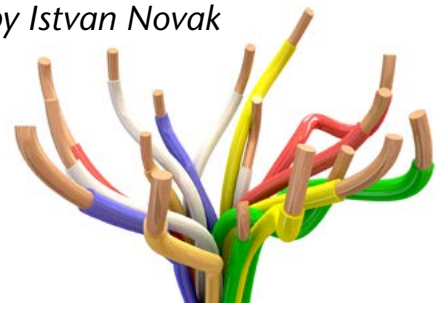
This Issue: SIGNAL INTEGRITY

FEATURED CONTENT

It's not a question of whether you'll encounter signal integrity problems. It's a question of when. In this issue, the industry's top SI experts weigh in with the latest tips, tricks and techniques for achieving signal integrity.







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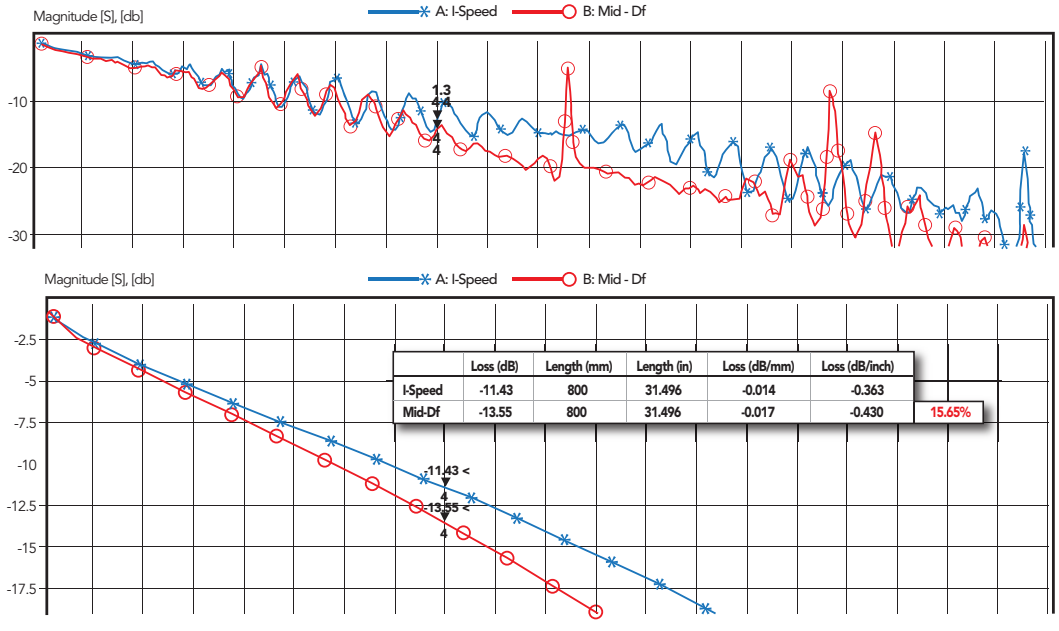

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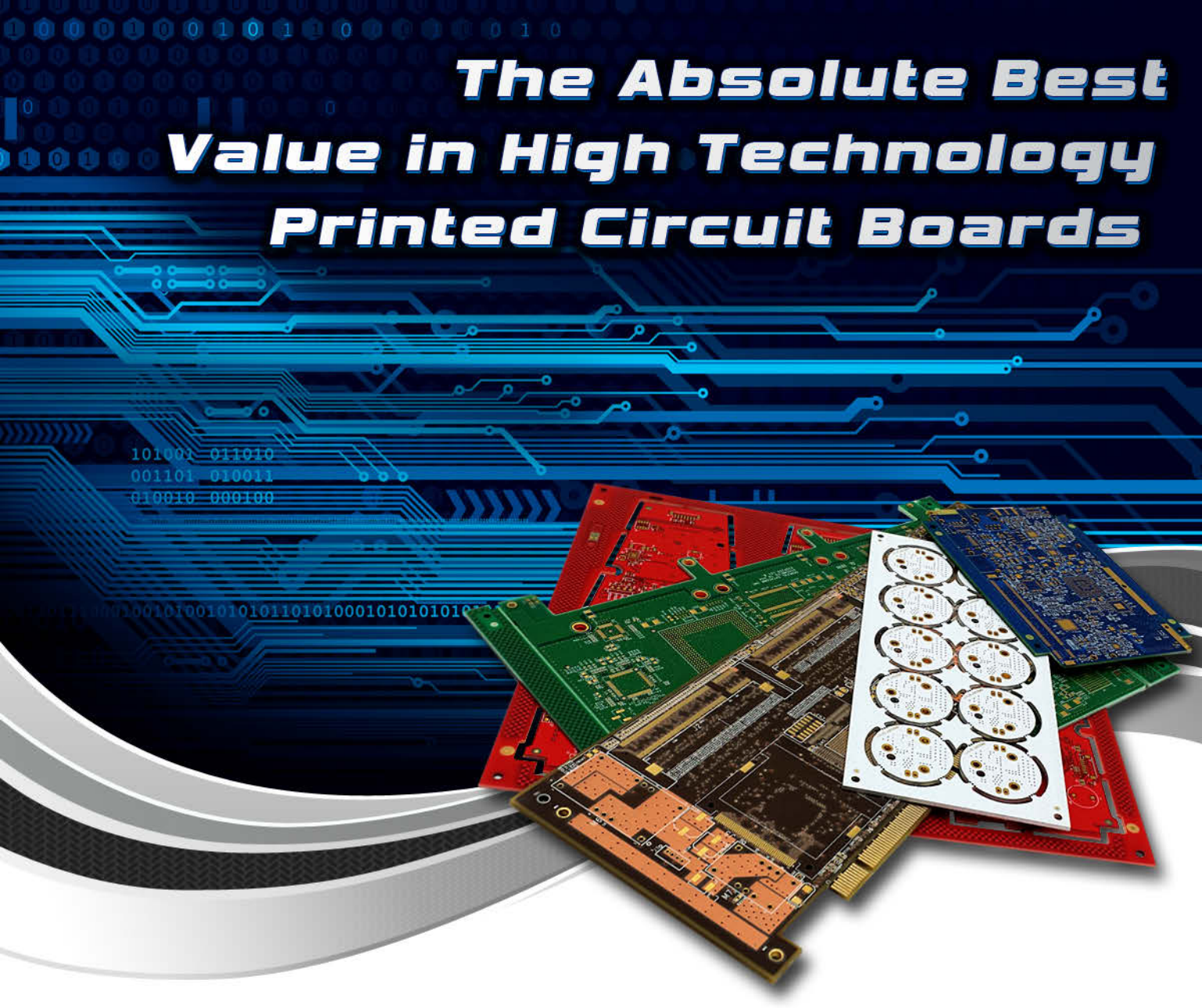

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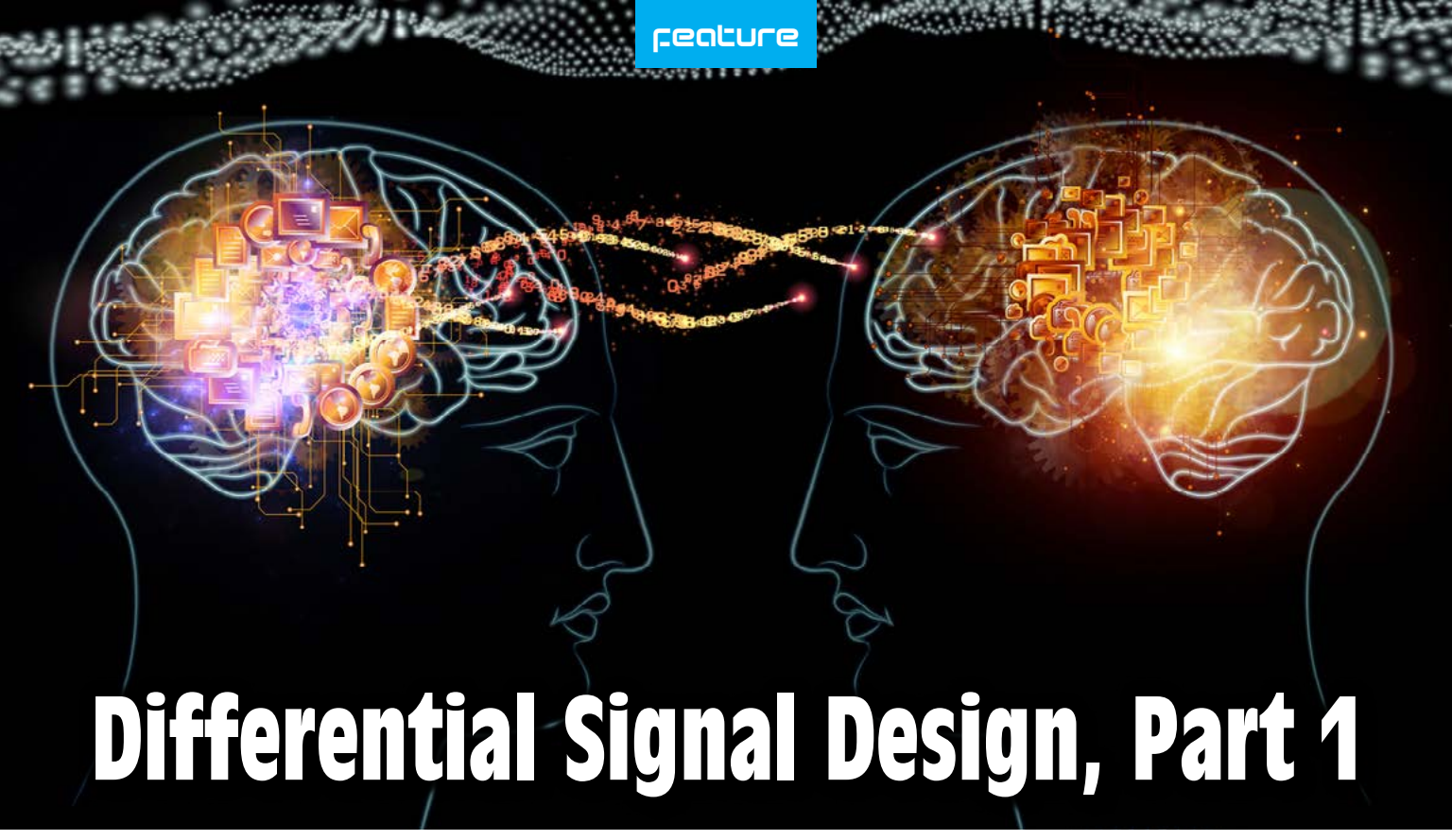

Differential Signal Design, Part 1

by Lee W. Ritchey
SPEEDING EDGE

SUMMARY: In its most basic form, a differential pair is made up of two transmission lines that have equal and opposite polarity signals traveling on them. But engineers and PCB designers have been flooded with misinformation about differential signal design. Lee Ritchey breaks down diff pair design and design rules in this two-part series.

Introduction

Differential signaling has evolved into the signaling protocol of choice for nearly all emerging designs. Over the years I have written articles covering specific questions on the subject and have devoted chapters to it in Volumes 1 and 2 of my book series, *Right the First Time, A Practical Handbook on High-Speed PCB and System Design,* as well as articles in our newsletters.

Along with all of this, there has been a flood of both misinformation and accurate information in magazine articles, applications notes and design guides. Some of this misinformation makes PCB layout more complex than it needs to be and some of it actually introduces potential malfunctions.

In order to help make the design task a little easier and sort through the misinformation, I decided it would be a good idea to pull all of this information together in a single place. This document is devoted to this topic in the hope that it will make it easier for engineers to get up to speed on this subject.

Throughout this article, I will use actual test data to determine where the limits are. At the end, there will be a list of design rules that apply to all differential pairs, along with a list of rules that should not be used as a starting point for creating a full rule set for a PCB or system.

This discussion focuses on differential pairs that are routed over planes as is common in PCBs. Differential pairs that travel on wires, such as UTP, are treated in my aforementioned books.

What is a differential pair and how does it work?

In its most basic form, a differential pair is made up of two transmission lines that have equal and opposite polarity signals traveling on them. The property that these two signals have in common is that they are equal and opposite and they are tightly timed to each other. Beyond these two characteristics there are no other properties that matter when a design uses

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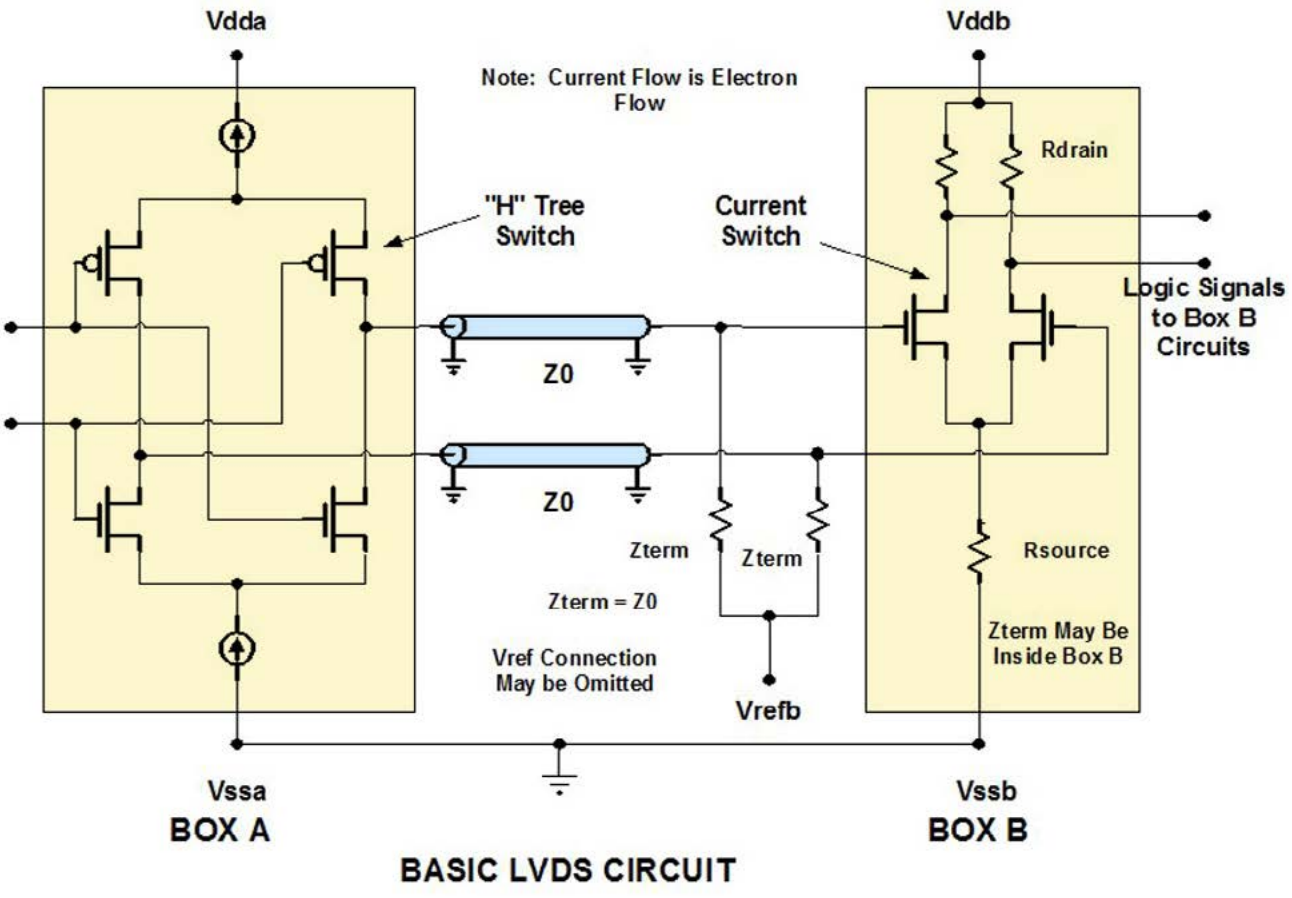

Figure 1: A typical CMOS differential signaling circuit.

differential pairs. Maintaining the equal and opposite amplitude and timing relationship is the guiding concept when using differential pairs.

Figure 1 is a typical CMOS differential pair driver and receiver pair. It is the usual circuit used in LVDS (low voltage differential signaling) type signaling protocols.

As can be seen from Figure 1, there are two independent transmission lines of characteristic impedance, Z_0, connecting the drivers and receivers. Each of these is terminated with a parallel termination of value Z_0 to V_{ref} in or at the receiver. Figure 2 shows the current flow in the two signal paths when the circuit is in one of its two logic states. In the other logic state the currents reverse direction. (The two lines do not have to be the same impedance for the circuit to function properly.)

As can be seen, the current flows out of the current source in Box A through the upper transmission line and into V_{refb}. A different current flows out of V_{refb}, up through a terminating resistor, through the lower transmission line and into the upper current source. When all of the impedances in the path are of equal magnitude, the two currents are equal and opposite flowing into and out of V_{refb} so the net current into or out of V_{refb} is zero. When this is the case, it is convenient to leave off the V_{refb} connection and place a single resistor of 2 times Z_0 across the two ends of the pair. When the impedance of the two lines is 50 ohms each, this results in a single resistor of 100 ohms. As a result, those who don't understand how this circuit works mistakenly conclude that a 100-ohm differential impedance is required, when, in fact, what is needed is two 50-ohm transmission lines each terminated in 50 ohms. More about this later.

The receiver responds only to the difference in voltage between the ends of the two trans-

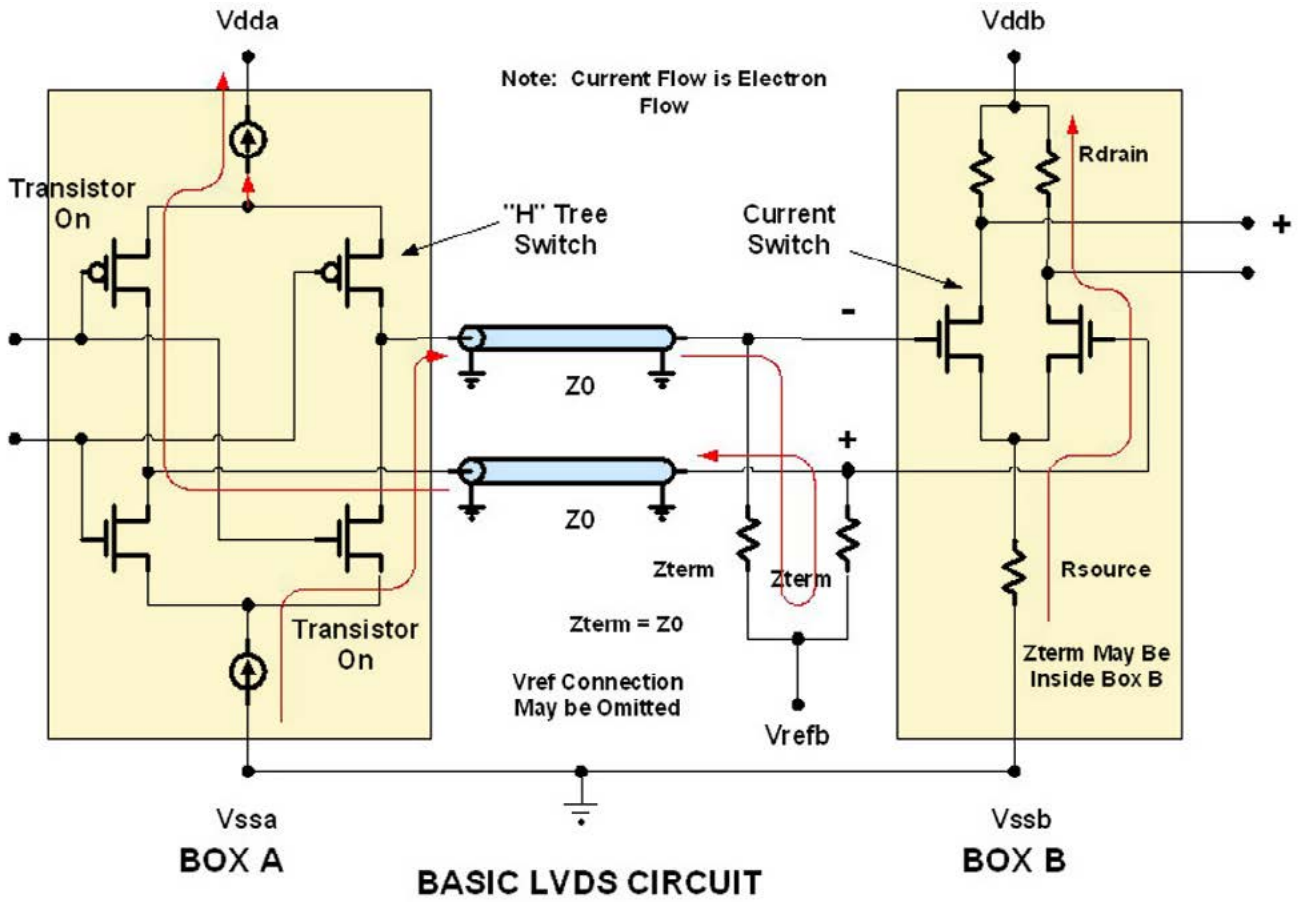

Figure 2: CMOS differential signaling circuit showing current flow.

mission lines and makes a decision as to whether a "1" or a "0" is present. When the polarity reverses, a logic state change is detected and sent on to circuits in the receiver box. It is at the moment of crossing that the logic state change is sensed. It is for this reason that minimizing jitter is so important. The receiver is a crossing detector so preserving the integrity of the crossing is essential. It is the primary concern when designing a differential pair. I'll come back to this later.

Why use differential pairs?

There are three reasons to use differential pairs in a digital or analog signal path. The most important one is that the ground connection between the two ends of the signal path can be very poor and data quality will not be compromised. Compare this to a single-ended signal path such as LVCMOS, where the signal arriving at the receiver is compared to a reference level in the receiver. If the grounds between the two ends are offset, the logic levels will be offset and one or the other of the two logic levels is compromised. This ability to "ignore" ground offsets has been the backbone of the wired Internet from the onset. In the case of Ethernet, the two ends of these links are transformer coupled. (I have seen examples of Ethernet links where the ground offset voltage was more than 6.5VAC, which would destroy the receiver if the circuit were DC coupled.)

In the case of the CMOS circuit shown in Figure 1, the driver transistor set (the H tree switch) is connected to V_{dd} and V_{ss} through two current sources. The switch is free to "float" with the circuits in the receiver circuit up or down as the ground offset between the two boxes changes. In some cases, the offset voltage can be as large as V_{dd}. As a result, the difference

voltage seen at the receiver is not affected by the offset. In some cases, the receiver circuit is connected with current sources instead of the driver circuit. ECL and most of the high-speed links with pre-emphasis or de-emphasis circuits in the drivers are examples of this. LVDS is an example of a link with the current sources in the driver.

A second reason to use differential signaling is that the link can suffer substantial attenuation of the signal and still function properly. In the case of the old ECL differential signaling circuit (the original differential protocol after which all later differential logic has been patterned), the signal leaving the driver is roughly 1000 mV. It only requires 20 mV for the receiver to successfully respond, so the signal could be attenuated as much as 24 db. In the case of many of the gigabit and higher differential signaling protocols currently in use, the signals can be attenuated as much as 20 db and the link still functions correctly.

A third reason to use differential pairs is for data paths with very high data rates such as gigabit and higher links. It is possible to drive differential paths at rates as high as 10 Gb/S over copper traces in standard PCB materials. This is impossible to do with single-ended logic paths.

When are differential pairs needed?

The usual conditions where differential pairs are needed can be determined from the characteristics discussed above. These are:

- Where the ground connections between the ends of the signal path are poor
- Where there is significant attenuation along the signal path
- When very high data rates are required

The first area where differential signaling was employed was the data paths between the various chassis in early mainframe computer systems. The protocol used was ECL differential signaling. Next, differential signaling was used for slow speed data links where the environment contained large amounts of electrical noise such as a factory floor. The usual protocol was RS-422 with very large signal swings.

Single-ended logic was successfully employed in almost all TTL and CMOS digital applications with wide parallel data buses until laptop computers came onto the scene with a large graphics data stream that had to pass from the motherboard through the hinge to the graphics display. When parallel data paths were used, two problems crept in: The wire bundle associated with the wide parallel data bus did not fit well into the hinge, and the ground connection was not satisfactory for single-ended operation as the simultaneous switching noise (SSN) was excessive. The solution was to switch to a serial data stream using differential signaling and call the protocol LVDS.

Since then, this protocol has been used in an increasingly wider array of products, giving rise to the following protocols. All of the following protocols share the same characteristics and can use the same design rules:

- Infiniband
- Ethernet
- Hyper Transport
- PCI Express
- Fiberchannel
- XAUI
- Rocket I/O
- Firewire
- IEEE 1394
- Universal Serial Bus (USB)
- SSCSI (serial SCSI)
- SATA (serial ATA)
- SIDE (serial IDE)

Why aren't differential pairs used for all digital signal paths?

Knowing all of the advantages of differential signaling, we may ask, "Why hasn't it been adopted for every data path?" The reason is that most data streams are parallel bus organized, as used by CPUs and memory systems. In order to use a differential data link, which is usually serial, the parallel data stream must be first converted to a serial data stream as it enters the differential pair and then reconverted to a parallel data stream at the receiving end. This is accomplished with serializer/deserializer (serdes). The logic circuits required to do this are relatively complex and, until recently, were costly to im-

plement. As a result, this cost was only justified where no other method of communicating the data was successful.

There are examples of single data path signals that require differential signaling even when both ends of the path are on the same PCB. The clocks on DDR2 memory systems are examples of this. The SSN associated with large data buses switching causes clocking problems with single-ended clocks, so these clocks are differential pairs.

With the advent of very large scale integration and the shrinking of features on ICs, it has become possible to manufacture these serdes as part of a large IC at very little cost. This has made it possible to employ serial differential signaling on virtually any product including disc drives (SATA, SIDE and SSCSI), video games, PCs, and peripherals (USB).

"The primary consideration in length matching is keeping jitter to a minimum. Jitter is the movement in time of the crossing or data transition from bit to bit with respect to the clock that is part of the data path."

How is length matching tolerance determined?

At the beginning of this document, I mentioned that one of the most important design considerations when using differential signaling is making sure that the lengths of the two transmission lines are the same within some limit set by the characteristics of the circuit. A simple solution to the problem is to require that the two paths be length matched "as close as possible" or adhere to some other very tight specification. This solves the problem, but it may result in difficult or impossible routing of the PCB. Designability must also be taken into account in order to arrive at a design that is both routable and functional.

A better solution is to understand how length matching affects performance and calculate a length matching tolerance that is, on the one hand, tight enough to guarantee proper performance and on the other hand loose enough to be routable with reasonable effort. There is a straightforward way to do this. Figure 3 depicts an example of routing a differential pair using routing vias to change signal layers. It would be good if this technique could be used without requiring length be added to the shorter side of the pair. A similar condition often exists when entering or exiting connectors. Two examples of signals crossing are illustrated, the upper one with perfect matching and the lower one with the two waveforms skewed.

The primary consideration in length matching is keeping jitter to a minimum. Jitter is the movement in time of the crossing or data transition from bit to bit with respect to the clock that is part of the data path. Jitter is at its lowest when the two signals cross in the "straight" parts of the rising and falling edges. The circuit still detects crossings when the waveforms cross as shown in the lower case in Figure 3, but, from cycle to cycle, the crossing will move around in time with respect to the clock due to the uncertainty associated with the low slope of the two waveforms. Crossings will also be detected when the waveforms are skewed even farther than that shown in the lower waveform pair. Because the slope of the waveforms is very near zero, jitter will be very bad and may render the circuit unusable.

Knowing this, it is possible to calculate the degree of mismatch that a given circuit can tolerate. This will allow specifying a matching tolerance that balances the demands of performance against ease of layout. The tick marks on the perfectly aligned set of waveforms mark the bounds of the "straight" portion of the switching waveforms. Jitter will stay at its minimum so long as the two edges cross within this time frame. All that is needed is to know the fastest rise and fall times of these waveforms as they arrive at the receiver to perform the necessary calculation. Once this time interval is known, multiplying it by the velocity of the waveforms on the transmission line (usually around 166 psec per inch in most PCB dielectrics) yields the length tolerance.

A couple of examples will illustrate this. LVDS is specified as working properly with length mismatches of 400 psec. Converting this

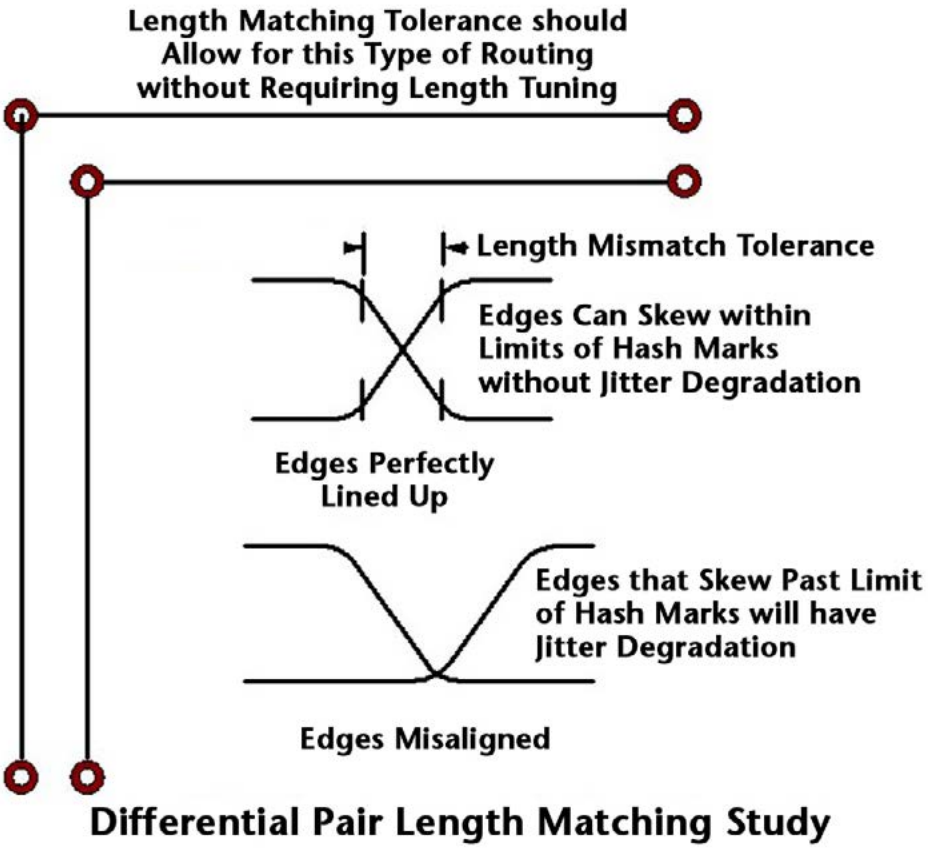

Figure 3: Example showing differential pair routing and length matching.

to a length results in a tolerance of approximately ±1200 mils or ±1.2 inches. Clearly, imposing a length-matching requirement of ±10 mils is excessively tight.

Another example is a 2.4 Gb/S serial link often used in high performance products such as routers, switches and servers. The fastest slope at the receiver is 60 psec in most systems. This results in a length matching tolerance of ±150 mils- enough to allow routing as illustrated in Figure 3 without requiring special length matching. This will result in reduced layout time and congestion of the routing surface that results from the zigzag add length routine usually used for this purpose.

Are there any undesirable side effects of length mismatching, even when within tolerance?

When the two edges are not aligned so that they don't cross exactly halfway from one voltage level to the other, as is the misaligned case in Figure 3, there is a short interval of time when current must flow into or out of the V_{ref} terminal. If a single 100 ohm resistor is used instead of two 50 ohm resistors to V_{ref} there is no connection. In this case, current is not available, so one of the edges will be slowed down. For low data rate protocols such as LVDS, this edge degradation is of little consequence.

When data rates are high and bit intervals are short, this degradation can have an adverse effect on bit error rate. This is certainly true for 2.4 Gb/S and higher signaling. To solve this problem, a path for the current must be provided. There are several methods for accomplishing this. One is to use a Thevenin termination on the end of each transmission line. This has the unwanted side effect of increasing power consumption and using excessive real estate when done on die. An alternative is to provide the two 50-ohm terminating resistors and connecting their common pins through a very small capacitor to ground. The size of this capacitor need only be on the order of 10 pF for 2.4 Gb/S and higher data rates. This is a practical solution when done on die. (At gigabit and higher data rates, it is necessary to locate the terminations on die in order to preserve signal integrity.)

Choosing terminating resistor values

Often, terminator values of 110 ohms are used when the specified differential impedance is 100 ohms. This looks like an error, but it is done on purpose. The reason for the higher value is as follows: Differential signal amplitudes are small, often leaving the driver at 400 mV

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peak to peak. As a result, there isn't much noise margin. In order to preserve as much noise margin as possible, it is advisable to make sure that there are no reflections at the receiver from mismatches between the terminator and the line impedance. One way to help this is to use terminator resistor values that are ±1 %. This helps, but the line impedance can vary ±10 % as a normal part of the PCB fabrication process.

Figure 4 is the waveform observed at the driver end of a 50-ohm parallel terminated transmission line with a perfect termination and terminations that are mismatched. Notice that when the terminator value is higher than line impedance, in this case 70 ohms, the reflection is in the same direction as the original signal or adds to the incident signal. This is often called overshoot. If there is a reflection, overshoot is the one to have, as it does not degrade the signal level. When the terminator value is less than the line impedance, in this case 30 ohms, the reflection is in the opposite direction as the incident waveform or takes away from the incident signal. This is often called undershoot. It is desirable to design the circuit so undershoot does not occur at any time.

Since the usual impedance of transmission lines in PCBs is 50 ohms and the tolerance is ±10%, it would be wise to choose a terminator value that is 10% higher than 50 ohms, or 55 ohms. Similarly, for 100-ohm differential impedance, an impedance of 110 ohms would be chosen. In this case, the mismatches will result only in overshoot with an amplitude low enough that it will not cause over-voltage conditions. As can be seen, the 110-ohm value was not an error, rather it was good engineering.

As the operating voltages of DDR memory ICs have dropped, the same situation exists. The built in terminations for many of the newer

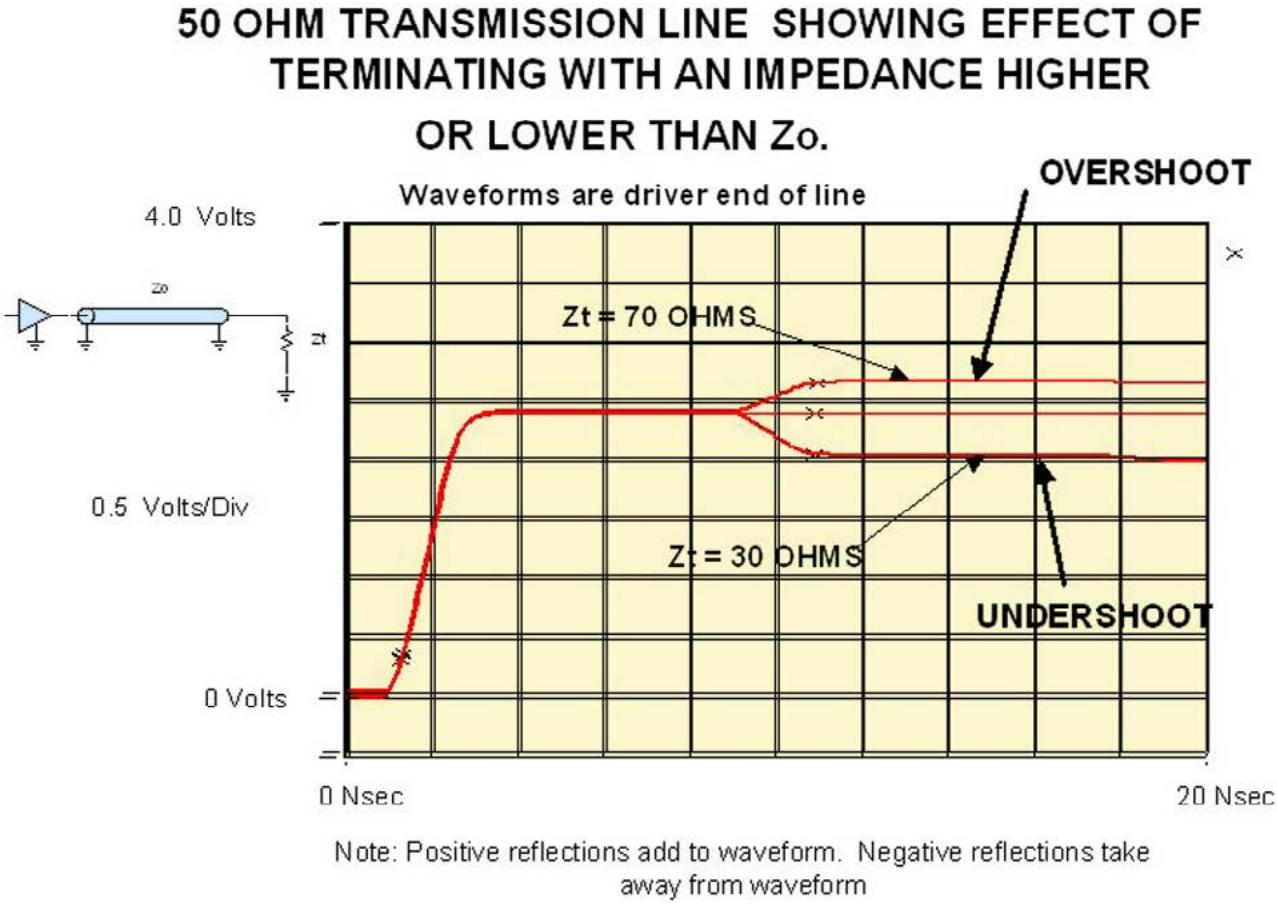

Figure 4: Overshoot and undershoot.

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memory ICs is higher than 50 ohms, often 75 ohms. This has been done for the same reason. The number is higher than ±10% due to the fact that resistor tolerances on ICs are often ±20%.

What do AC coupling capacitors do, and when are they needed?

AC coupling capacitors are inserted in series with each leg of a differential pair to provide DC isolation between the two ends of the data path. The usual reason for doing this is that the ground offsets between the two ends of the data path are too large for the built-in current sources in the driver or receiver to deal with. The most common situation where this is likely to occur is when signals travel between boxes or between cards in a large card cage. Many applications notes spell out AC coupling capacitors in paths that begin and end on the same PCB when both ends of the path are the same logic type. This is not necessary and should be avoided.

Another example of using AC coupling capacitors is when the two ends of the differential signaling path are of different technologies. The most common of these is when LVPECL (low voltage positive emitter coupled logic) is interfaced with LVDS (low voltage differential signaling).

Sizing the AC coupling capacitors is done by calculating their capacitive reactance at the lowest frequency data stream that will travel down the path. The capacitive reactance at that frequency needs to be a small fraction of the transmission line impedance to avoid excessive attenuation and signal distortion. For random data patterns, the lowest frequency may be at or near DC, in which case the capacitors will have to have very large values. Luckily, most of the data paths that use differential signaling employ an encoding scheme that makes sure the data stream never drops below some "idling" frequency. This idling frequency is used to recover the clock from the data stream at the receiver end. In this case, the capacitor value can be relatively small.

Where should AC coupling capacitors be placed? Do they cause signal degradation?

Usually, the transmission lines that are connected to AC coupling capacitors are located on internal layers on the PCB. In order to connect the terminals of the capacitors to the transmission lines, a via is required at each end of the capacitor. These vias are almost always through-hole vias with a drill diameter of 12 mils. In a 100-mil thick PCB, the parasitic capacitance of each via is approximately 0.4 pF. There is concern that this added parasitic capacitance along with the parasitic capacitance of the capacitor mounting structure might adversely affect the performance of the transmission line. Much has been written about this possibility and much speculation has been done about how severe the effect will be.

Similar speculation takes place about where the capacitors should be located. Should they be placed near the driver? Should they be placed midway between the driver and receiver? Should they be placed near the receiver?

Simulations conducted in an effort to determine the effect of adding AC coupling capacitors have yielded few, if any, real conclusions. A direct approach might be to build identical transmission lines with and without the capacitors and measure the loss vs. frequency of the two paths to determine if there is any difference. This is exactly what we have done to resolve this confusion. Figure 5 is a photograph of a pair of test PCBs used to make these measurements, along with others discussed later in this document.

Figure 6 depicts the loss vs. frequency for the two paths from 100 KHz to 6 GHz. This is equivalent to 200 Kb/S to 12 Gb/S. The red curve is the path with no AC coupling capacitors and the blue curve is the path with AC coupling capacitors. Each AC coupling capacitor is 0.1 uF in a 0402 package connected to the transmission line on each side of the mounting pads with 12 mil drilled vias.

Notice that there are very small differences between the two curves, but nothing that would significantly affect signals out as far as 12 Gb/S. While this test does not actually change the locations of the capacitors along the length of the transmission line, it is reasonable to conclude that since the effect of the capacitor is very small at all frequencies of interest its location along the length of the trace will also not matter. If one considers that this is a linear

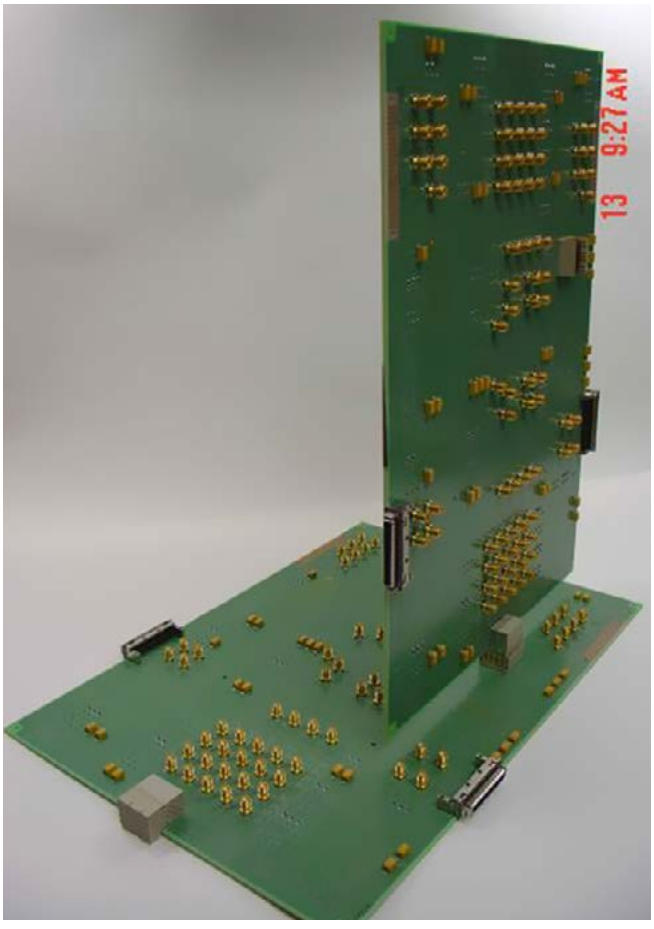

Figure 5: Test PCB used to measure actual path losses.

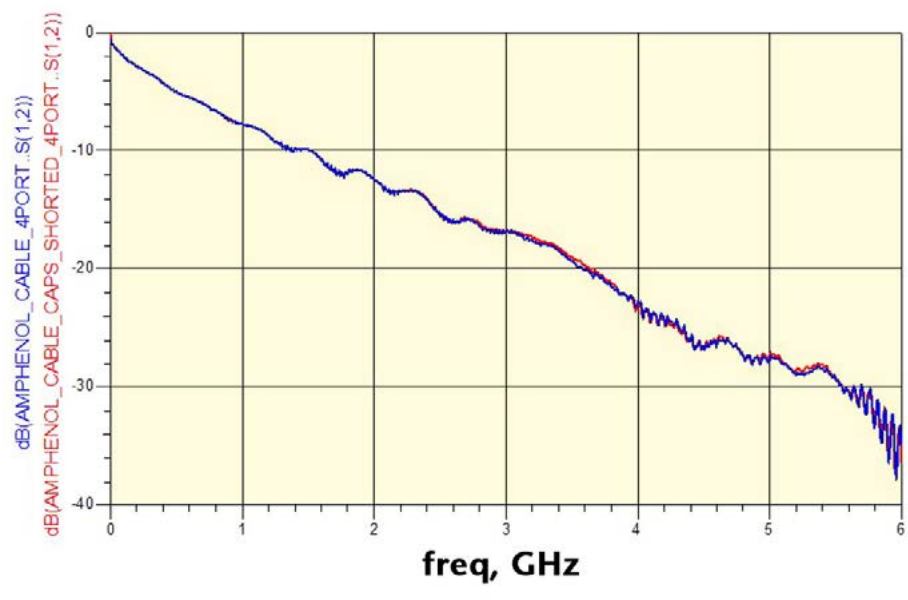

Figure 6: Loss vs. frequency for data paths with and without AC coupling capacitors.

circuit, the location of the capacitors along the path will not change the overall behavior of the path.

Any downsides to adding AC coupling capacitors to a differential pair?

An obvious downside to adding AC coupling capacitors to a differential pair is the need to find room for the capacitors, their connecting vias and their mounting pads, as well as the added parts on the bill of material. A not-so-obvious downside is that the receiver side of the path will suffer a DC offset or drift if the data pattern traveling on the path is not symmetrical. There are two solutions to this problem. One solution is to encode the data in such a way that the data is symmetrical. This is what the 8b/10B encoding does. A second and more general solution is to add a resistive network on the receiver side of the AC coupling capacitor that "biases" the input such that the DC component of a nonsymmetrical of the waveform is eliminated.

Is tight coupling of a differential pair a good idea?

There is the notion that tight coupling between differential pairs is a good idea. There is even one industry "guru" who is known to say "everybody knows tight coupling is a good idea," as if anyone who does not know this must be incompetent. In some cases, the reason given is that it reduces unwanted coupling from other signals. This will be discussed later in its own section. Another reason given is that the "return currents" from one member of the pair will travel better on the other member when tight coupling is done.

Figure 7 shows an example of a differential pair tightly routed (5 mil lines and 5 mil spaces with a height above the plane of 10 mils). Figure 8 shows the same differential pair routed with 10

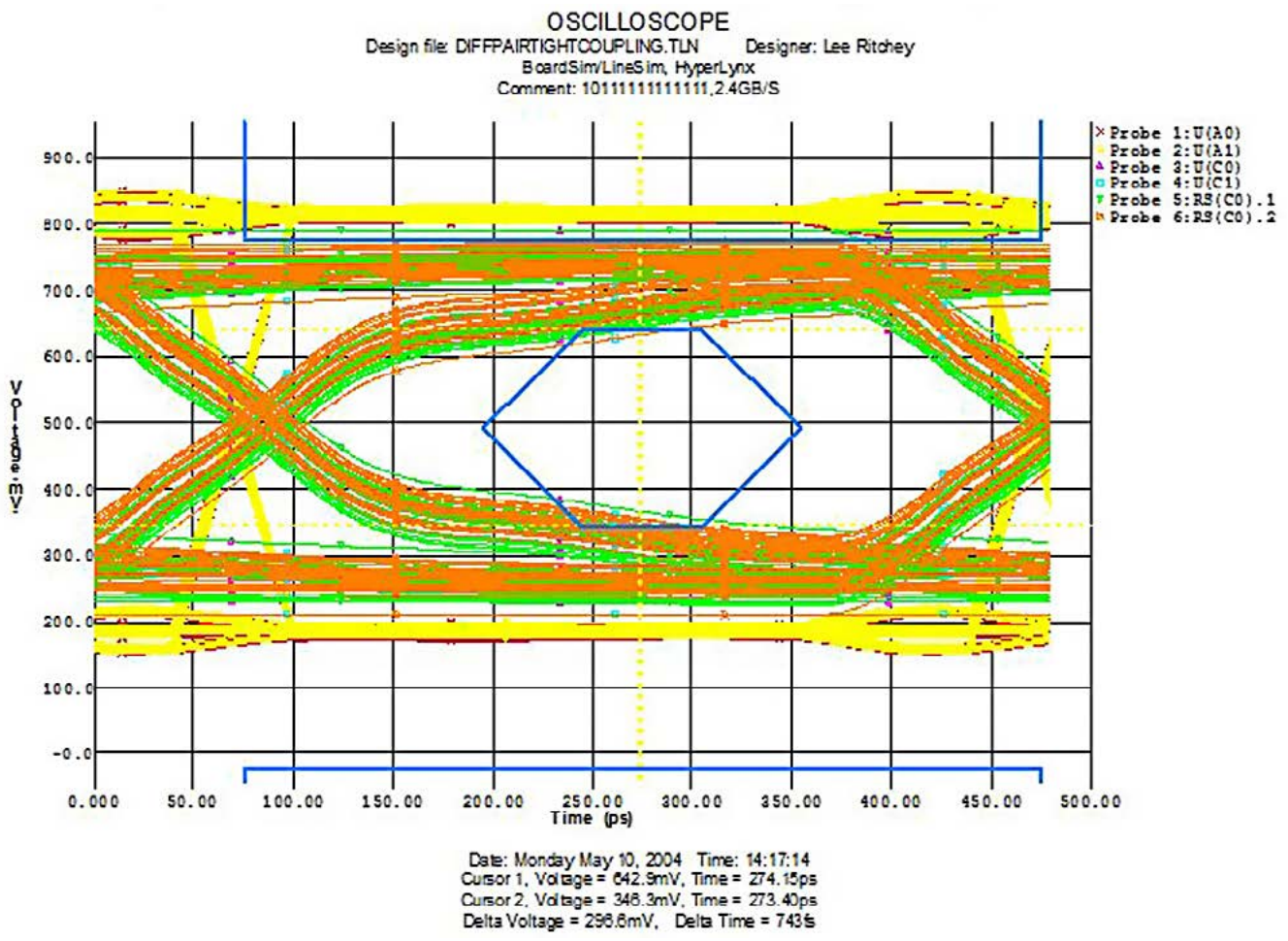

Figure 7: Tightly coupled differential pair.

mil spacing. In order to achieve the same "100 ohm" differential impedance, the trace width was increased to 10 mils in the second case. The reason for this will be explained later. Both data paths are running at 3.125 Gb/S and are 30 inches long with copper thickness of ½ ounce or 0.7 mils (18 microns).

This method of viewing signal quality is called an eye diagram. It is created by setting up a storage oscilloscope so that one bit period is visible on the screen, and then the data path is exercised with thousands of randomly generated data bits. Eventually, the worst-case bit pattern will be captured, allowing assessment of the quality of the data path.

Notice that the signal amplitude or the eye opening is larger in the loosely coupled case than in the tightly coupled one. The reason for this is higher skin effect loss with the 5-mil trace used in the tightly coupled case. A consequence of crowding traces close to each other is that each trace drives the impedance of the other down due to added parasitic capacitance. Higher parasitic capacitance on a transmission line always drives impedance down. In order to get back to the 50 ohms needed on each trace to meet the 100-ohm differential impedance requirement, the trace must be narrowed resulting in higher skin effect loss. Jitter is also higher in the tightly coupled case.

As noted above, one consequence of tight coupling is higher skin effect loss. A second, and more consequence is that the two traces must always be kept tightly coupled along their entire length. Figure 9 illustrates what happens to the differential impedance when each of

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DIFFERENTIAL SIGNAL DESIGN, PART 1 *continues*

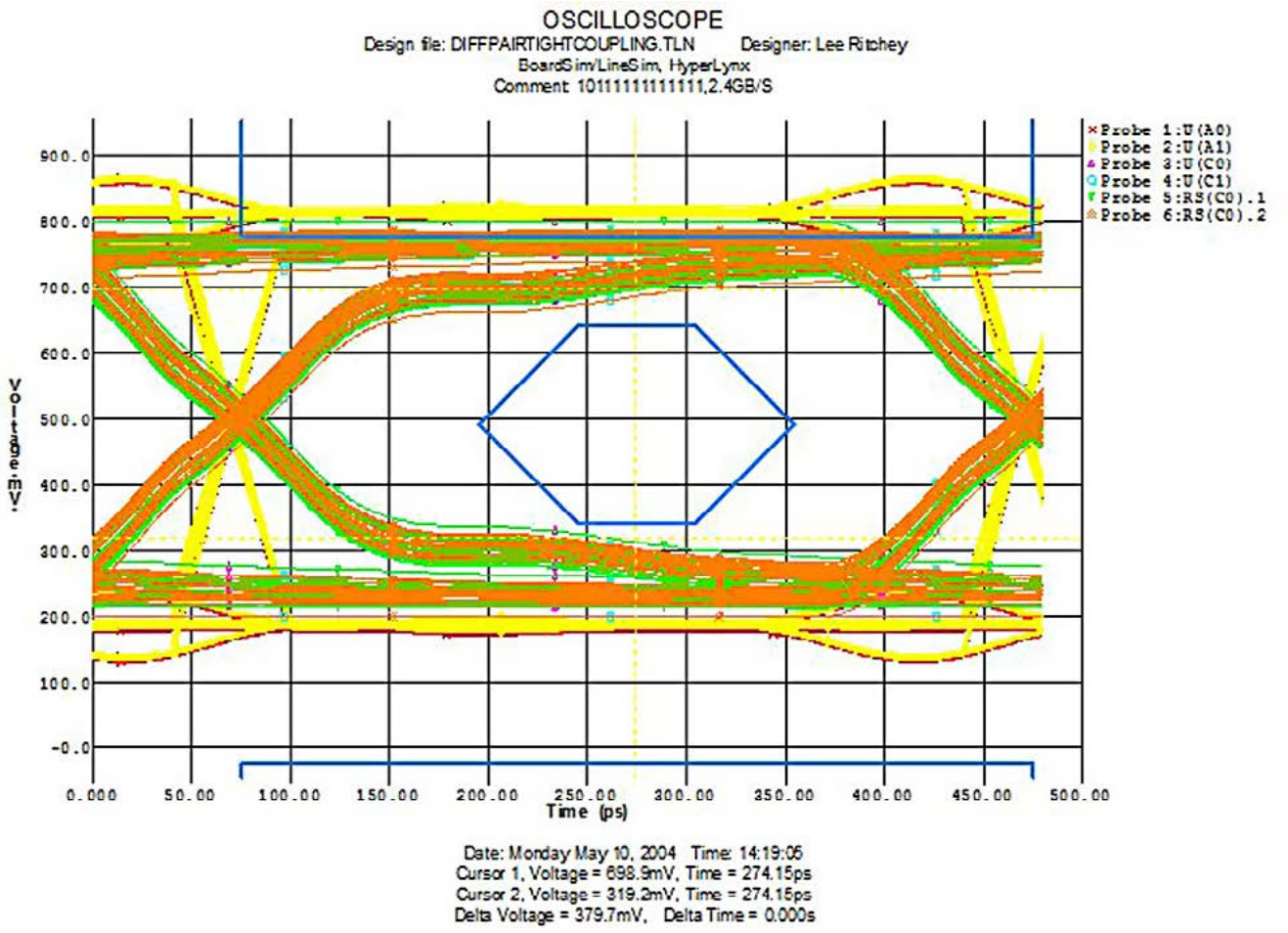

Figure 8: Loosely coupled differential pair.

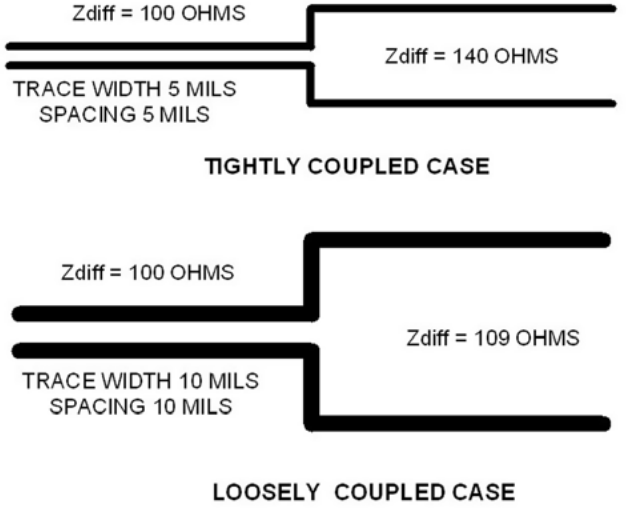

Figure 9: Tightly spaced and loosely spaced differential pair.

the two pairs in Figures 7 and 8 is separated to weave through a 1 mm pitch BGA or other pin field where it is not possible to maintain the tight spacing.

Both differential pairs are spaced 10 mils above the plane over which they are routed. Trace and spacing for Figure 7 is 5 mil lines and 5 mil spaces. Trace and spacing in Figure 8 is 10 mil lines and 10 mil spaces.

Notice that the differential impedance of the tightly coupled pair increases to 140 ohms when the traces are separated. Said another way, the individual impedance of one trace when separated from its partner is 70 ohms while the loosely coupled pair changes to 109 ohms or a single-ended impedance of 54.5 ohms.

The reason the single-ended impedance of the tightly coupled pair is so high when the traces are separated is that introducing any metal, whether a trace or a plane fill, close to a transmission line adds parasitic capacitance resulting in a lowering of the impedance. In order to bring the impedance back to the desired 50 ohms, the trace must be made narrower, in this case to 5 mils. When the metal is removed from the near field, this added parasitic capacitance goes away and the single-ended impedance of the trace returns to 70 ohms.

As long as skin effect loss is not an issue, tightly coupled traces work fine. However, it is necessary to maintain the tight coupling along the entire length in order to avoid reflection problems. In many cases this is a severe routing handicap. A restriction that comes to mind is that it will not be possible to route differential pairs through the pin field of a high pin count 1 mm BGA. **PCBDESIGN**

Part 2 will continue in the September issue of The PCB Design Magazine.

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Lee Ritchey is founder and president of Speeding Edge. A longtime PCB design instructor and consultant, Ritchey is the author of *Right the First Time: A Practical Handbook of High-Speed PCB and System Design.*

How Electromagnetic Fields Determine Impedance, Part 1

Douglas Brooks, Ph.D.
ULTRACAD DESIGN

We talk a lot about trace dimensions and relationships when discussing signal integrity issues. In particular, we like to talk about how close traces are to underlying planes and how close traces are to each other. But there is another way to think about things that is sometimes much more practical and intuitive, and that is by thinking about the electromagnetic field *around* the trace(s) we are considering. The position and shape of the electromagnetic field can tell us a lot about trace impedance, EMI and crosstalk coupling, and signal propagation speed.

When a current flows down a conductor (Figure 1) an electric field and a magnetic field radiates away from that conductor. Collectively, this is called the electromagnetic field. What is important to note is that this field *always* exists. Furthermore, the electromagnetic field and the current are inseparable. That is: (a) the electric field can't move ahead of the magnetic field; (b) the magnetic field can't move ahead of the electric field; and (c) neither field can get ahead of or fall behind the current itself. They all have to move together along the conductor.

Another point that should be intuitive needs to be said anyway. It is that important. If a current causes an electromagnetic field to exist around a conductor, then a changing current causes a changing electromagnetic field to exist around the conductor.

A changing current in a conductor induces a current in an adjacent conductor (Figure 2). This is related to Faraday's Law of Magnetic Induction and is also the principle behind a generator, a transformer, EMI, and crosstalk.

Some signal integrity simulators allow us to visualize the electromagnetic field

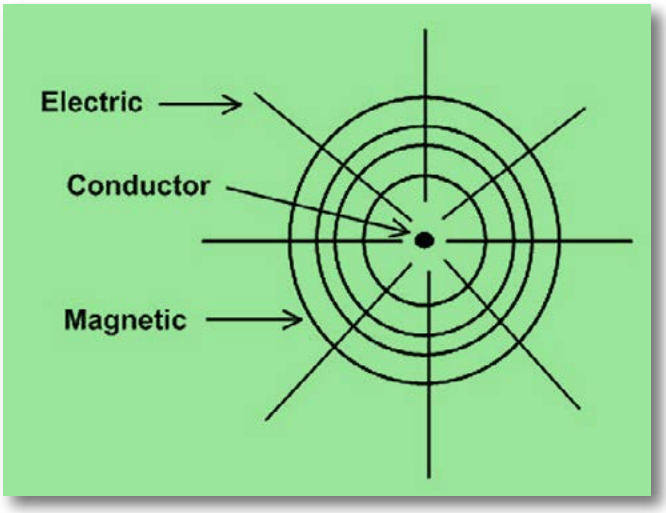

Figure 1: The electromagnetic field around a conductor when current flows.

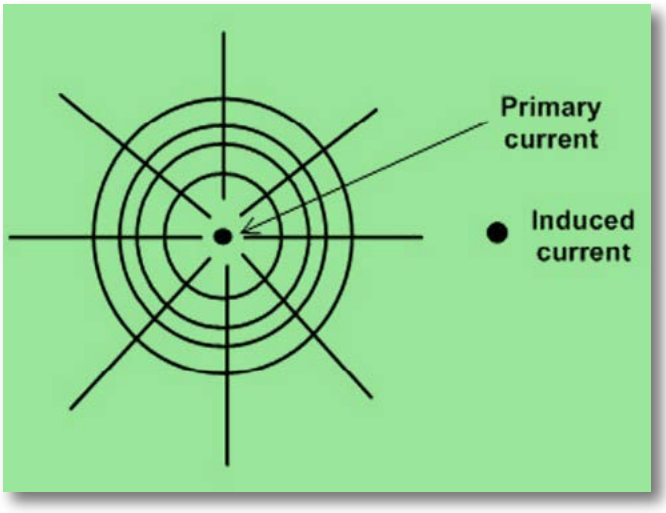

Figure 2: A changing primary current in a conductor induces a current in a nearby conductor.

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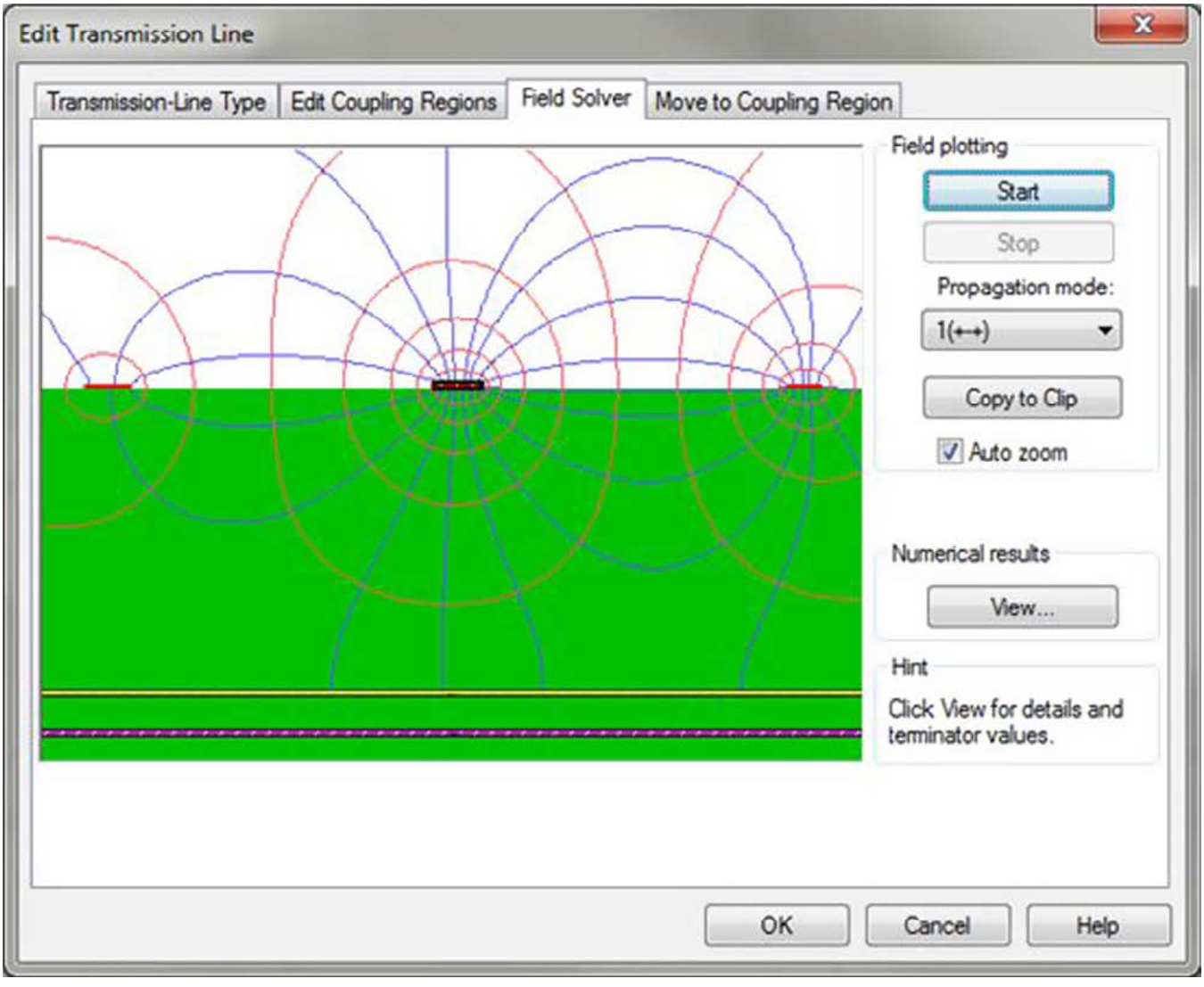

Figure 3: Electromagnetic field illustration shown in HyperLynx.

around a PCB trace. The Mentor Graphics HyperLynx tool is one of them. Figure 3 is an image of the Field Solver screen under the Edit Transmission Line menu. The blue lines radiating away from the trace are the electric field lines, and the orange lines circling around the trace are the magnetic field lines. We can infer several things from thinking about and visualizing the electromagnetic field. This column addresses what the field can tell us about the impedance of the trace.

Figure 4 illustrates the electromagnetic field around an 8 mil wide, 0.5 oz. trace, 6 mils above the underlying plane. The trace is part of a differential pair. The second trace separation is 20 mils from the first. The single-ended characteristic impedance of each trace is given by the model as 59.6 ohms. (This results in a Zdiff of 114.9 ohms.)

Figure 5 shows the field patterns for a pair of 16 mil traces, 12 mils above the plane, and 1.0 oz. in thickness, separated by 40 mils. It looks much like Figure 4. In fact, it almost looks like we have repeated Figure 4 by mistake. But we haven't! The field patterns look identical. In fact, the field

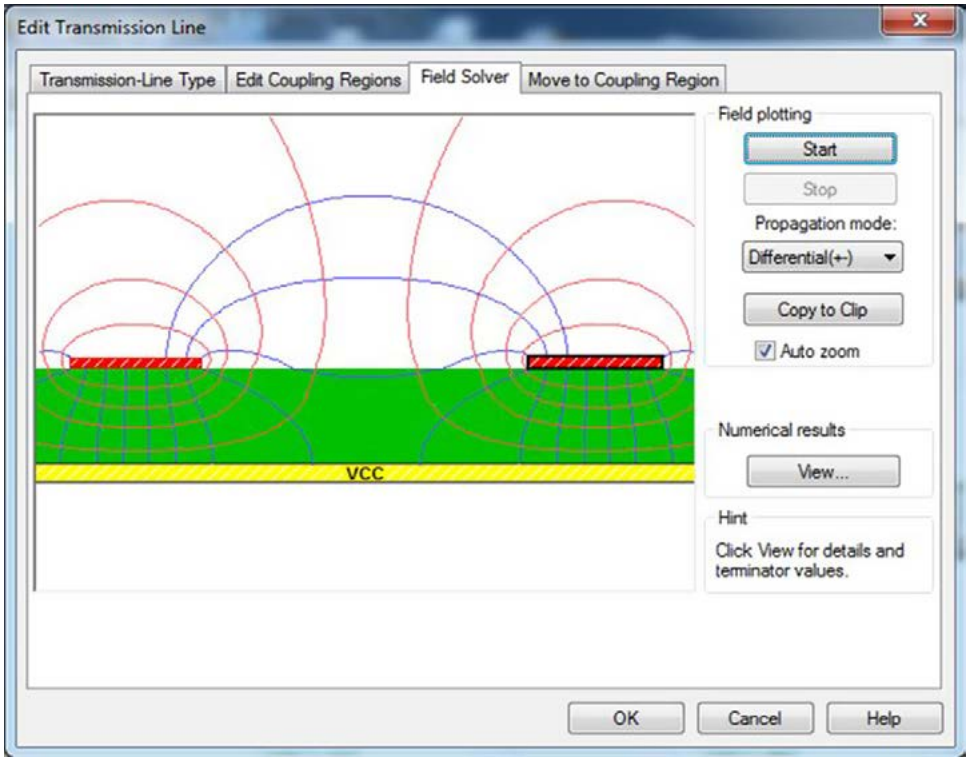

Figure 4: An 8 mil trace, 20 mil separation, 6 mil above plane, 0.5 oz. thick.

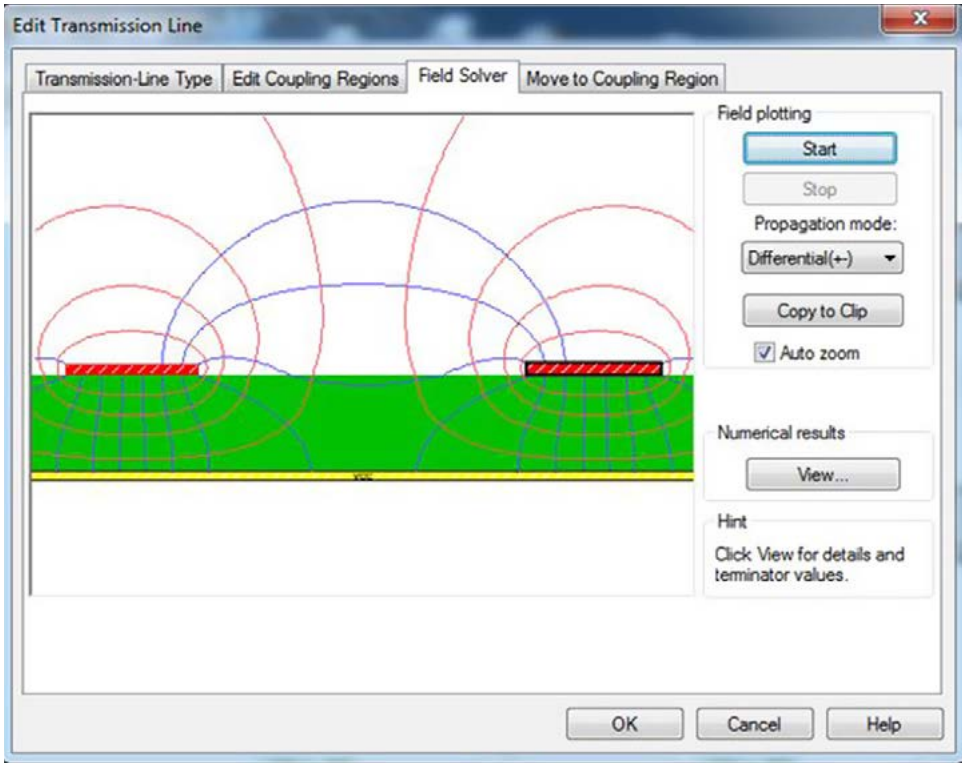

Figure 5: A 16 mil trace, 40 mil separation, 12 mil above plane, 1.0 oz. thick.

patterns are identical! And the single-ended characteristic impedance is identical at 59.6 ohms. (And the Zdiff is also identical at 114.9 ohms.) In fact, *everything is identical; it's just scaled.*

This illustrates a very important point. The impedance is not necessarily determined by the stackup dimensions. Several different combinations of stackup dimensions will lead to the same characteristic impedance. *The impedance of the trace is determined by the electromagnetic field distribution.* If we scale the dimensions, we don't change the electromagnetic field pattern, and therefore we don't change the impedance.

This illustrates one example of how visualizing the electromagnetic field pattern (or in this case the difference in the pattern between two different stackups) can help us visualize some of the parameters related to the traces. To illustrate this point another way, consider Figure 6. This is the same stackup as Figure 4, but with a trace separation from the plane of only 3 mils. Looking at the figure, we see that more of the

HOW ELECTROMAGNETIC FIELDS DETERMINE IMPEDANCE, PART 1 *continues*

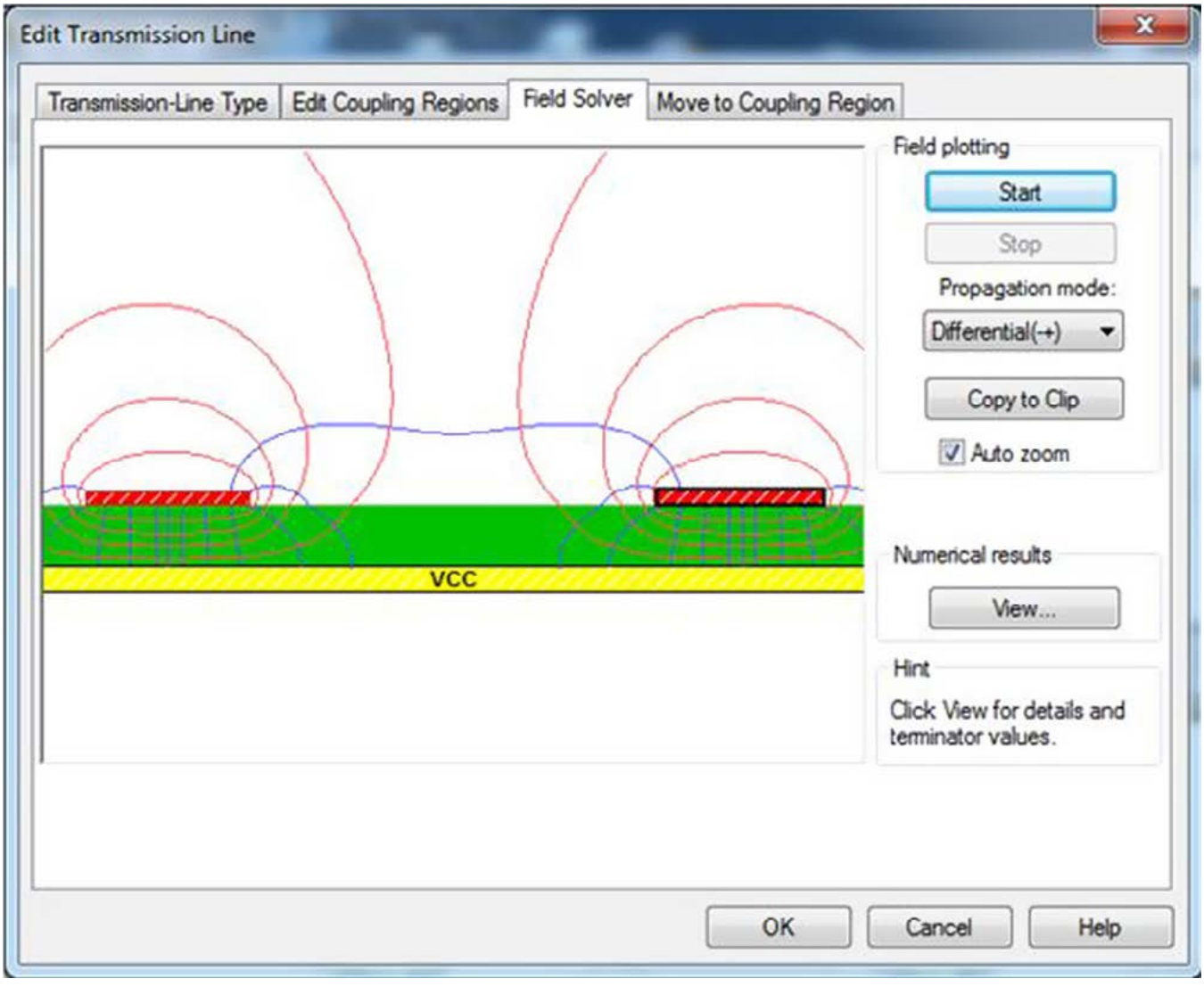

Figure 6: 8 mil trace, 20 mil separation, 3 mil above plane, 0.5 oz. thick.

field is captured between the trace(s) and the plane. This would imply that the capacitance between the trace and the plane is greater (than in Figure 4), and that therefore the characteristic impedance would have gone down. In fact, the model gives the impedance as 39.5 ohms.

When thinking about signal integrity issues, train yourself to think in terms of what the electromagnetic field might look like, or what it might look like if some change were made. This can result in some quick and intuitive insights about what will happen on your boards. **PCBDESIGN**

Douglas Brooks, Ph.D., is the founder of UltraCAD Design Inc. He has written numerous articles in several disciplines and held signal integrity seminars around the world. He has spent most of his career in the electronics industry in positions of engineering, marketing, management, and as CEO of several companies. Prentice Hall recently published Brooks' latest book, PCB Currents: How They Flow, How They React. Visit his website at www.ultracad.com.

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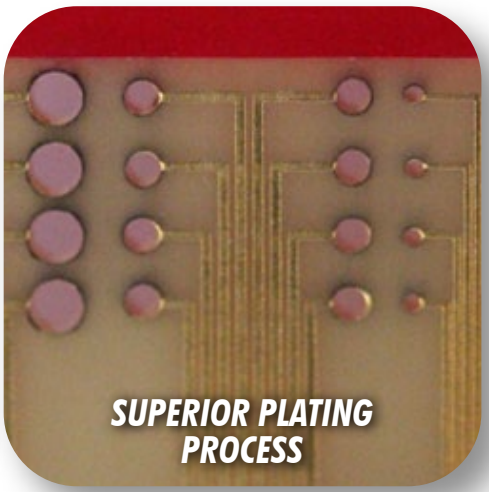

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PCB007 News Highlights

PragoBoard Joins FabStream's Network of PCB Makers

FabStream, the integrated PCB design and manufacturing solution developed by DownStream Technologies and targeted at the DIY electronics market, has announced that PragoBoard has become the sixth PCB manufacturer to join the FabStream network of global PCB manufacturers.

Graphic Plc Acquires Flex PCB Maker Calflex

Graphic Plc. has acquired the assets of California-based Calflex, a flex PCB specialist with 30 years experience in supplying military, aerospace, and medical industries. The Graphic Group now has a real world presence of PCB manufacturing with specialist IMS plants in the UK, the U.S., Europe, and Asia.

Endicott Interconnect Files for Chapter 11 Protection

Endicott Interconnect Technologies filed for Chapter 11 protection in U.S. Bankruptcy Court on July 10. According to court documents, the New York-based company owes between $50 and $100 million; former parent company IBM is EI's largest creditor, with $5.5 million in unsecured debt.

IPC APEX EXPO 2014: 95% of Booth Space Sold

The show sold out of exhibitor space last year and 2014 is promising to sell out as well. "Our number one priority is to give our exhibitors and attendees the best return on their investments, giving them an opportunity to grow their businesses and increase revenue," said Alicia Balonek, senior director of trade shows and events.

German PCB Market on the Rise

Sales of PCBs in Germany were up by 5.7% in April, year-on-year, according to the Central Association of PCB and Electronic Systems. This is the third consecutive month of growth in 2013.

Gorilla Circuits Lands Zeta Certificate

Integral Technology, Inc. has announced that PCB manufacturer Gorilla Circuits is the next PCB fabricator certified to produce circuit boards using Integral's revolutionary Zeta® glass-free laminate and film solutions for rigid PCB applications. "Gorilla Circuits is a shining example of how entrepreneurial vision can guide a company to success even in a down economy," stated Integral President Ken Parent. "Gorilla's commitment to engineering quality and reliability makes them a valued member of the Zeta® team."

Multek: New Interconnect Technology Center In Silicon Valley

"Our Interconnect Technology Center will focus on future technologies for the printed circuit board industry with the understanding that critical decisions are made specific to connections within the board and the device as a whole," said Franck Lize, president.

N.A. May PCB Shipments Down 4.4%, Bookings Up 8.3%

"PCB sales and orders have been below last year's levels for most months of the past year, but they have been improving in recent months," said Sharon Starr, IPC director of market research. "Order growth rates have improved faster than sales growth rates, which accounts for the positive book-to-bill ratios of past five months," she explained.

Maskless Completes Series D Financing; Collaborates with CBT

Bill Elder, president and CEO of MLI said, "I am very pleased to have closed this round of financing that will enable MLI to continue its rapid growth into the global PCB market. In addition to the new funding, as part of the collaboration between MLI and CBT, MLI will be able to integrate its existing direct imaging technology into CBT's vast array of lithography products, all focused on the PCB industry."

Epec, Suncoast Digital Technology Join Forces

Ed McMahon, CEO of Epec, commented, "We are very excited to welcome Suncoast Digital into the growing Epec family. Paul Knupke, Joe Frangione, and their dedicated team have built a tremendous reputation that seamlessly fits into Epec's proven business model, focusing on providing customers with high-level engineered solutions."

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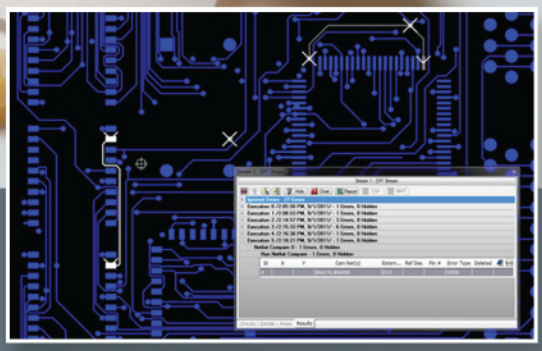

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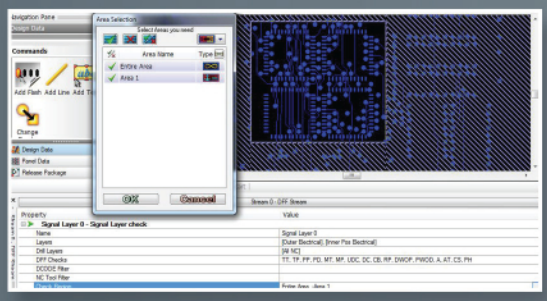


Define DFM checks by area so components such as BGAs can be verified with unique rules different from rest of design

DownStream Technologies

Don't Forget to Terminate Cables

by Istvan Novak
ORACLE

We know that in high-speed signal integrity measurements, one of the first rules is to properly terminate traces and cables. However, many of our PDN measurements may be limited to lower frequencies, such as measuring the switching ripple of a DC-DC converter. Do we really need to terminate our measurement cables if the signal we want to measure is the switching ripple of a converter running at 1 MHz? We may think that termination is not needed or does not matter in this case, but we may be in for some surprises!

Let us look at the output ripple of the LTM4604 converter[1], which was our device under test in an earlier column[2]. The converter is powered from a 4.5V battery pack, and its output voltage is set to 1.2V. An approximate 1A DC load is created by a small incandescent bulb. The output ripple is measured by a Tektronix TDS540B oscilloscope that I recently bought on eBay. The 1 GS/s maximum real-time sampling rate and 500 MHz analog bandwidth, together with a maximum 1 mV/div vertical sensitivity makes this category of oscilloscopes very useful for many PDN measurements even today. The setup is shown in Figure 1.

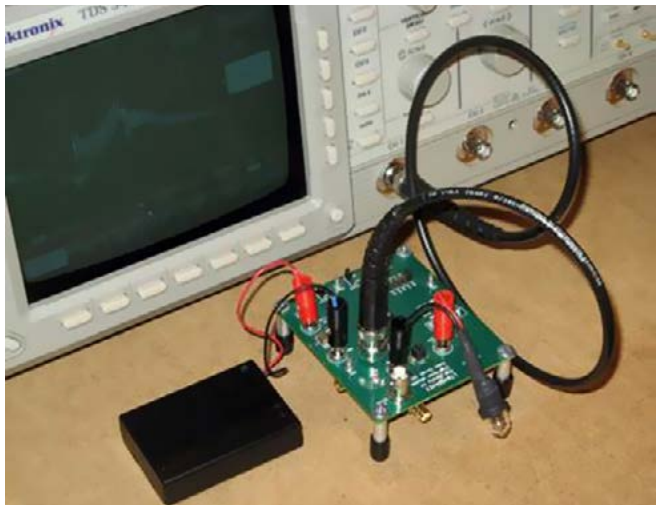
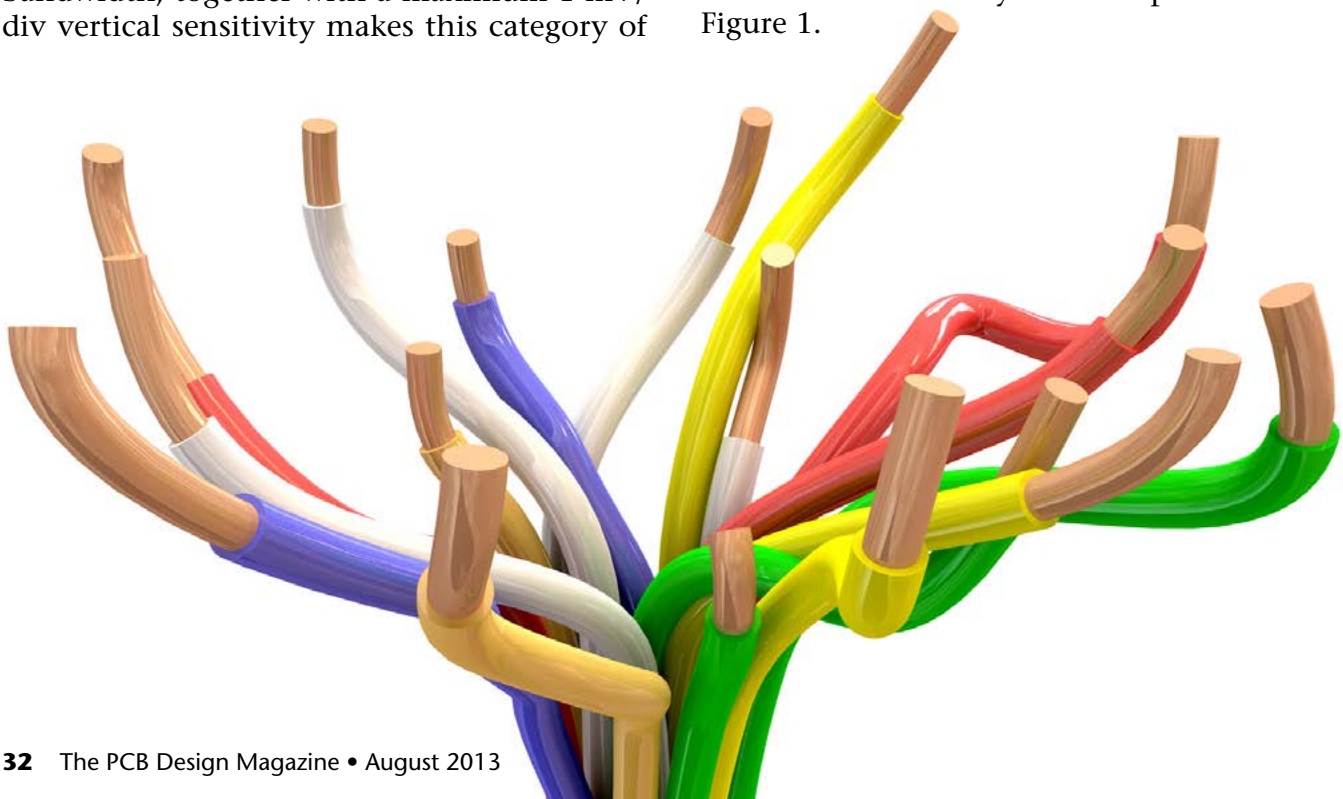


Figure 1: LTM4604AEV DC-DC converter evaluation module (courtesy of Linear Technologies), connected to CH1 of a Tektronix TDS540B oscilloscope through a coaxial cable.



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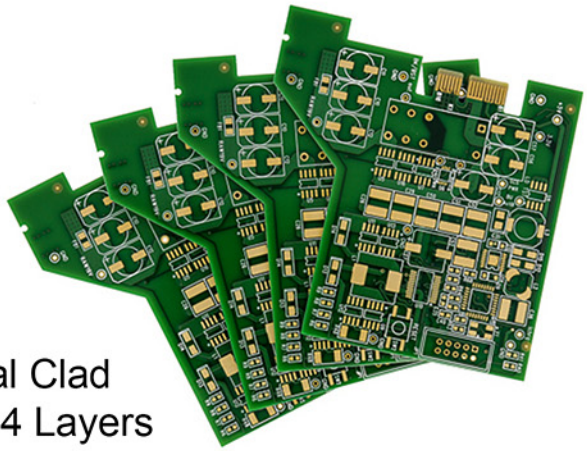

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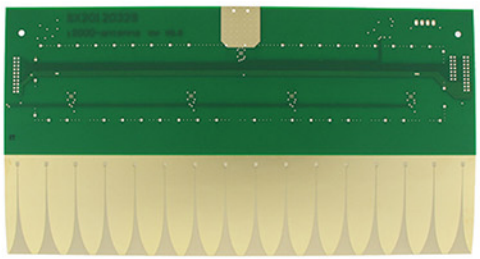

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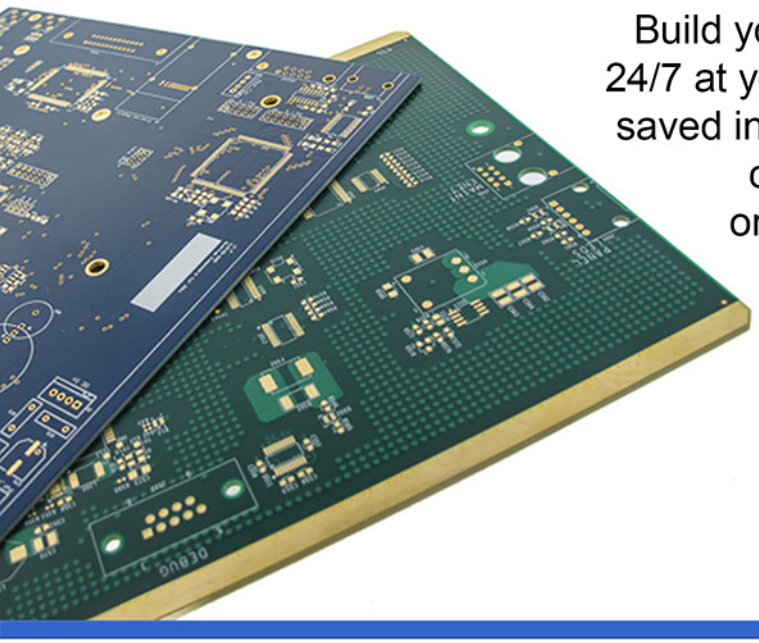

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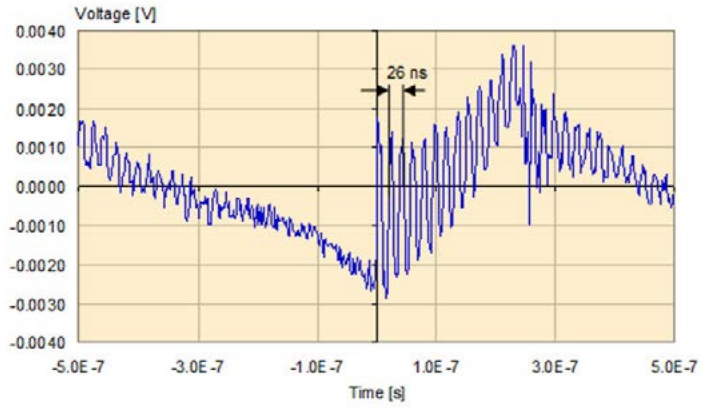

Figure 2: Output ripple of the DC-DC converter shown in Figure 1.

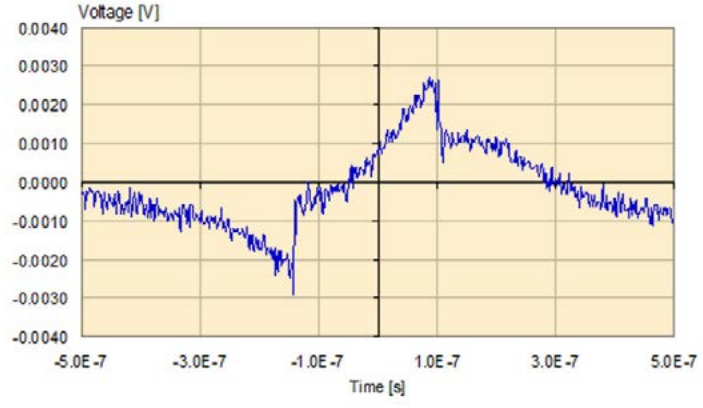

Figure 3: Output switching ripple measured with 50 ohm termination at the oscilloscope input.

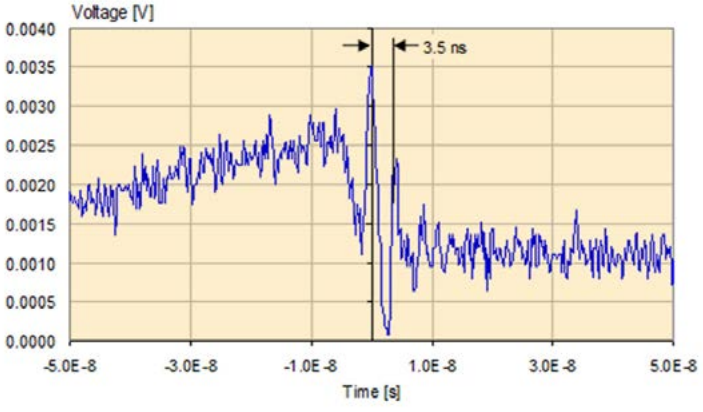

Figure 4: Same waveform as in Figure 3, except zoomed in around the end of the ON period.

When we connect the output BNC socket to CH1 of the oscilloscope with a coaxial cable, we get a waveform shown in Figure 2.

Figure 2 shows approximately one full cycle of the converter, with the trigger point aligned to time zero. The ON time, shown by the positive ramp, is approximately 0.3 ms. The peak-to-peak ripple is below 10 mV, so everything makes sense, except we see a strong oscillation during the ON time with a 26 ns period. When we check the oscilloscope settings, we notice that, in order to show the small AC contents on top of the 1.2V DC, the autoscale feature uses AC coupling on the oscilloscope input. Checking further, we will notice that the input impedance is set to 1 MOhm. This 38 MHz ringing is caused by the reflections on the one-meter Belden RG 58C/U coaxial connecting cable. The coaxial cable has almost full reflections at both ends: an approximately +1 voltage reflection coefficient at the oscilloscope input and an approximately -1 voltage reflection coefficient at the DC-DC converter output. These conditions create a quarter-wave resonator with a resonance period of four times the one-way propagation delay. The unloaded propagation delay is 5.1 ns/m; with the load reactances at the input and output of the cable we may get a delay of 6.5ns, which results in a 38 MHz ringing frequency. We will notice by using different cables that the ringing frequency changes proportionally with the cable delay.

Unfortunately, the 38 MHz ringing frequency is not high enough so that we could count on eliminating it by switching on the customary 20 MHz BW limit option. The proper way to eliminate this ringing is to use a 50 ohm termination at the oscilloscope input. We can use either an external 50 ohm termination at the end of the cable and then we can keep the 1 MOhm input setting on the oscilloscope, or switch the oscilloscope input to 50 ohms. When we switch the oscilloscope input to 50 ohms (and leave the AC

coupling setting), we get a warning reminding us that the 50 ohm input impedance together with the series capacitor providing the AC coupling will result in an increased high-pass cut-off frequency. Since in this case our lowest frequency component of interest is the 1MHz fundamental wave of the switching ripple, this will not degrade our measurement.

Using the 50 ohm termination setting on CH1 input, we get a ringing-free switching waveform as shown in Figure 3.

This waveform is much cleaner and it now allows us to hunt for finer details. For instance, as shown in Figure 4, if we zoom in on a switching transition, we will notice a high-frequency ringing; this time, on the other hand, the ringing is "real," generated by the DUT.

This high-frequency ringing now has a 3.5 ns period, corresponding to a 286 MHz frequency. As opposed to the 38 MHz ringing we had before, this ringing does not change as we change cables. By looking at the switch-node waveform, we can convince ourselves that this ringing is the parasitic ringing originated inside the DC-DC converter module and is the result of the fast switching edge exciting the parasitic inductances and capacitances associated with the switching elements. **PCBDESIGN**

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Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To contact Novak, click here.

Practical Signal Integrity

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

"There are two types of designers: Those that have signal integrity problems and those that will." —Sun Microsystems.

If you are a digital designer, you will eventually have SI problems whether you like it or not. But all is not lost. If you learn to work with these issues, then you will soon become proficient with high-speed design.

Advances in semiconductor lithography enable IC manufacturers to ship smaller and smaller dies. However, Moore's law (1965) is still in effect: The number of transistors on ICs doubles every two years and will continue for at least 10 years. Arguably, the predictions about the law were short-sighted, and the paradigm will continue to apply as chip sizes continue to scale down. But keeping up with it is becoming more challenging. Intel for instance, changed transistor structure into 3D form, by placing transistors on top of each other, on the latest 22 nm process to enable them to continue shrinking silicon.

Each new generation of semiconductor process technology delivers greater levels of integration, higher performance and lower cost. However, these benefits are offset by increases in power consumption that seem to unavoidably accompany each reduction in feature size. In order to reduce power consumption, IC manufacturers have moved to lower core voltages and higher operating frequencies which of course mean high current requirements and faster edge rates.

Faster edge rates mean reflections and signal quality problems. So even when the package and your clock speed haven't changed, a problem may exist for legacy designs. The enhancements in driver edge rates have a significant impact on signal quality, crosstalk, timing and EMI. So whether you like it or not, welcome to the domain of high-speed design.

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Impedance Control

Impedance is the key factor that controls the stability of a design—it is the core issue of signal integrity methodology. At low frequencies, a PCB trace is almost an ideal circuit with little resistance, and without capacitance or inductance. Current follows the path of least resistance. But at high frequencies, alternating current circuit characteristics dominate, causing impedances, inductances and capacitances to become prevalent. Current then follows the path of least inductance. The impedance of an ideal lossless transmission line is related to the capacitance and inductance:

$$Zo = \sqrt{L/C} \qquad \text{Equation 1}$$

But this is very simplistic and the impedance should be simulated by a field solver (Figure 1) to obtain accurate values of impedance for each signal layer of the substrate. The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a reduction in quality of the signal and possibly radiation of noise. For perfect transfer of energy, the impedance at the source must equal the impedance at the load. However, this is not usually the case and terminations are generally required at fast edge rates to limit ringing.

Figure 2 shows a typical scenario where there is a Virtex-4 driving into a 1.5" transmission line and then to the DDR2 receiver. The impedance of the driver is 20 ohms—its value is embedded in the devices IBIS model. Now, obviously, a 20 ohm driver does not match a 52.4 ohm transmission line.

The red waveform in Figure 3 shows the ringing of the un-terminated trace. However, once a 33 ohm series terminator is placed close to the driver, the impedances are matched resulting in the blue waveform. Notice that the rise time is slower now. There are, of course, different types of termination strategies but series is the best for point-to-point terminations because it slows down the edge rate without drawing extra current. Parallel terminations are typically used as end terminators on the address busses pulling the signal up to VTT.

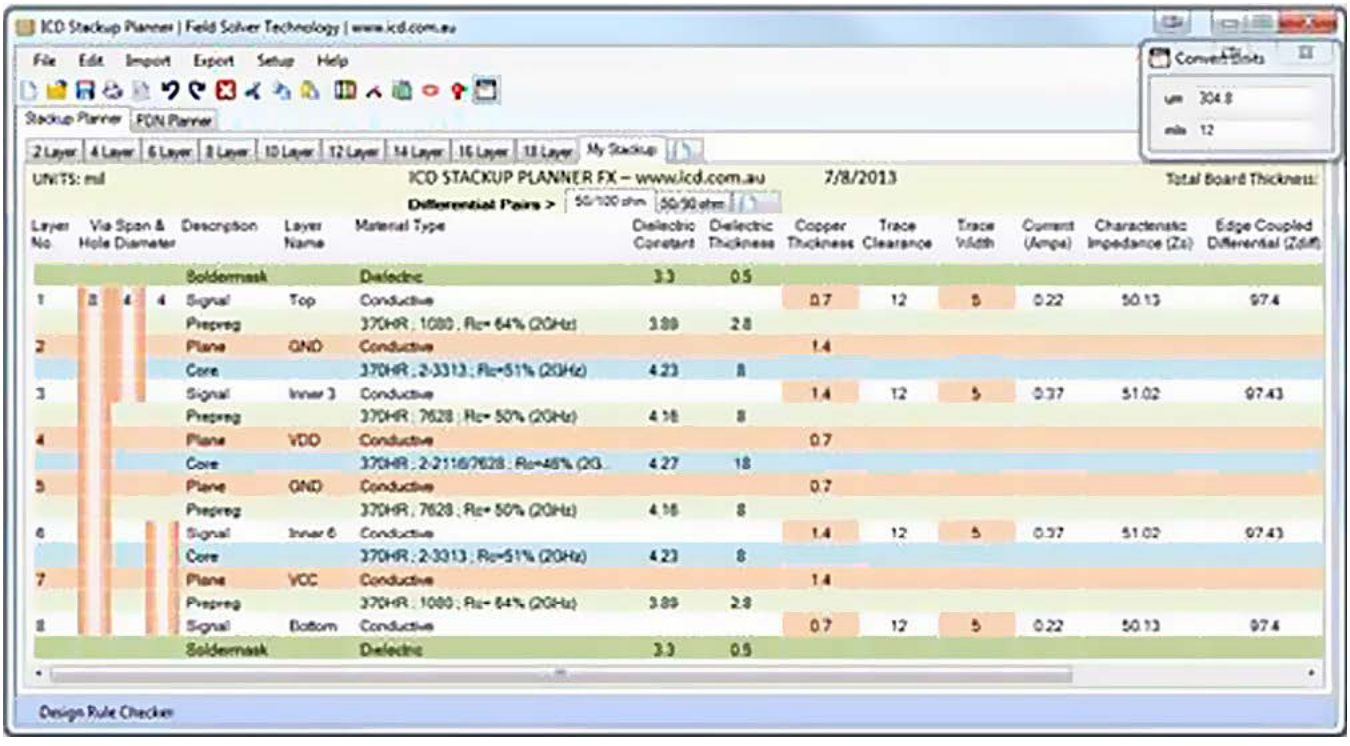

Figure 1: Impedance of the transmission lines simulated by a BEM field solver.

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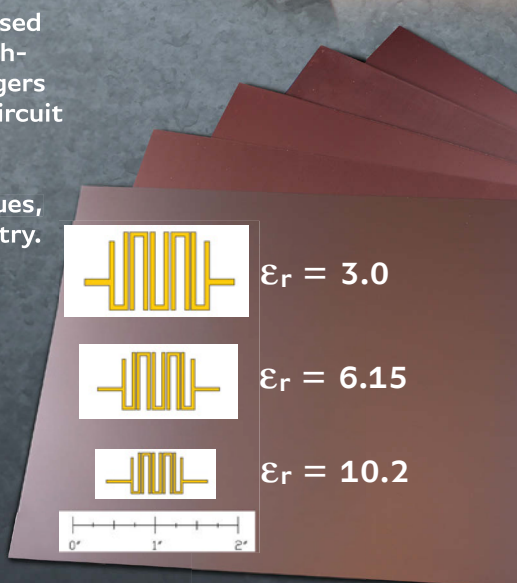

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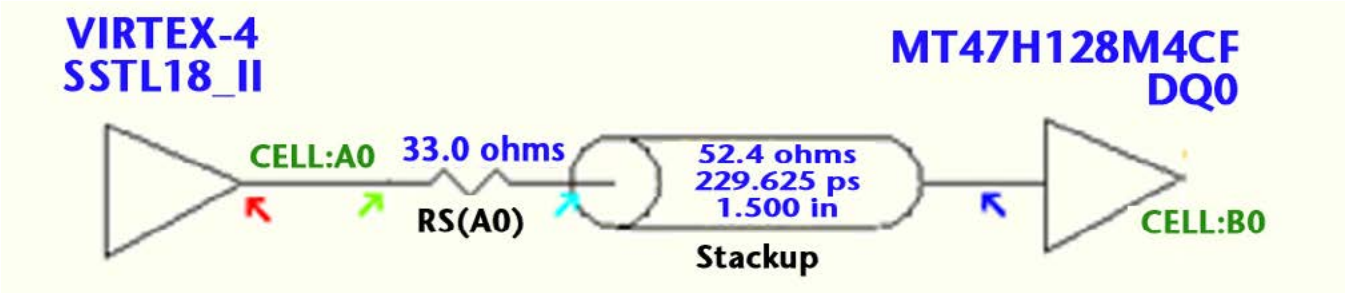

Figure 2: Model of a Virtex-4 driver, a 1.5" transmission line and a DDR2 receiver.

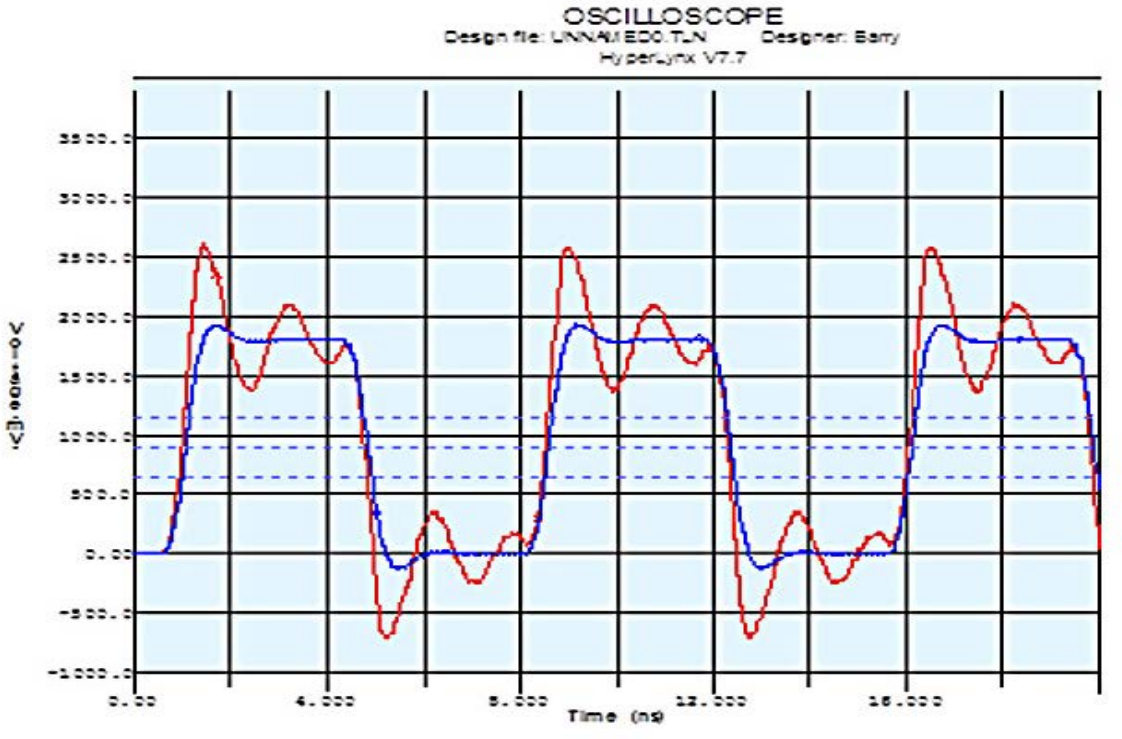

Figure 3: Comparison of an unterminated (red) and a terminated (blue) trace.

In this case, the rise time of the unterminated signal is 235 ps whereas it is slowed down to just 350 ps once terminated. It is the rise time rather than the frequency that is of concern.

Rule of Thumb: All drivers whose trace length (in inches) is equal to or greater than the rise time (in ns) must have provision for termination.

Crosstalk

Crosstalk is the unintentional electromagnetic coupling between traces on a PCB. But crosstalk can also be induced in the return path—which often gets overlooked. The insidious little creature pictured in Figure 4 is the crosstalk associated with two parallel trace segments on the outer (microstrip) layer of a PCB.

The red lines represent the magnetic field that couples voltage inductively to the nearby trace and also radiates electromagnetic emissions. The blue lines are electric fields that capacitively couple current into the nearby trace and are somewhat absorbed by the plane but still tend to radiate noise outward.

Crosstalk is caused by capacitive and inductive coupling:

- Capacitive coupling causes signal voltages to couple current into nearby nets. This is also referred to as forward or far end crosstalk (FEXT)
- Inductive coupling causes signal currents to couple voltage into nearby nets. This is also referred to as backward or near end crosstalk (NEXT)

In the case of inductive coupling, return currents can overlap, also causing ground bounce to occur. The return currents follow the path of least inductance with the streams of electrons crossing over each other. Although this is probably immeasurable, one would assume that there would be some sort of detrimental interaction (crosstalk) between these streams. When the stackup is planned, be aware of which plane(s)—either power or ground—will be the return path for the critical signals and make sure there is an unobstructed return path.

Crosstalk can be coupled trace-to-trace, on the same layer, or can be broadside coupled by traces on adjacent layers. The coupling is three-dimensional. Broadside coupling is difficult to spot, as generally we look for trace clearances when evaluating crosstalk; a simulator will pick this up. Traces routed in parallel and broadside cause greater amounts of crosstalk than those routed side by side. This is due to the width of the trace being much larger that the thickness, so more coupling occurs in the broadside configuration. It is therefore good practice to route adjacent signal layers in the stackup orthogonally to each other to minimize the coupling region. A better solution is to only have one signal layer between two planes to totally avoid broadside coupling altogether.

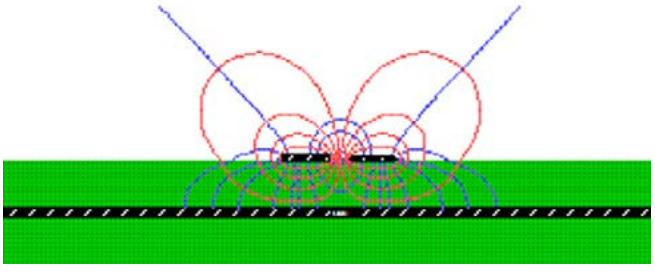

Figure 4: Crosstalk on the outer (microstrip) layer.

Since crosstalk is induced by one or more aggressors onto a victim trace, it is obvious that the higher the aggressor voltage the more crosstalk will be induced. It is therefore best to segregate groups of nets according to their signal amplitude. This strategy prevents larger voltage nets (3.3 V) from affecting smaller voltage nets (1.5 V).

Crosstalk is defined by:

$$Xtalk = \frac{1}{1 + (\frac{D}{H})^2}$$ Equation 2

The above equation clearly shows that in order to reduce crosstalk, we need to minimize H (height above the plane) and maximize D (distance between traces). The easiest way to reduce crosstalk, from a nearby aggressor signal, is of course by increasing the spacing between the signals in question. Crosstalk falls off very rapidly with distance. Crosstalk plummets roughly quadratically with increased separation. Doubling the spacing cuts the crosstalk to roughly a quarter of its original level.

Rule of Thumb: Gap = 3X trace width.

However, in today's complex, dense designs, it is not always possible to use up valuable real estate to satisfy the above. An alternative is to set up parallel segment rules to prevent traces running in parallel for more than 500mils. Also, the effect of dielectric height above a reference plane on trace-to-trace coupling plays an important role in reducing the crosstalk. A 3 mil thickness dielectric material reduces the crosstalk by approximately a quarter compared to the 6mil given the same trace spacing.

Rule of Thumb: Couple the signal traces closely to the plane.

Rail Collapse in the Power Distribution Network

Now that the quality of signal paths is sorted out, we need to look at other sources

of noise. In order to reduce power consumption, IC manufacturers have moved to lower core voltages and higher operating frequencies. But as the voltage drops, the current increases; and as the frequency increases, more energy is required, more often. Then, if a 64-bit wide bus is switching simultaneously, one hell of a lot of current is required—up to 10A—instantaneously. This tends to collapse the power supply rails creating further SI and also EMI problems. The power distribution network (PDN) must be designed to maintain constant voltage levels under maximum switching load.

The goal of PDN analysis is to maintain low AC impedance, on the supply voltage planes, from DC to the maximum required frequency. Excessive electromagnetic radiation typically occurs where there is a peak in the AC impedance. This maximum frequency or bandwidth should also take into consideration the odd harmonics of the clock. The bandwidth increases as the rise time gets faster. For DDR2 memory running at 400 MHz, the fifth harmonic is 2 GHz. So what was assumed to be just a 400 MHz design now has to be stable up to 2 GHz. (On second thought, maybe you should leave this to the experts?) Actually, it is quite simple if you have the right tools.

In Figure 5, the plane data has been extracted from the ICD stackup planner into the ICD PDN planner, and the AC impedance of a 1.8 V DDR2 supply is analyzed up to 10GHz. The AC impedance is below the target impedance of 60 mΩ up to 400 MHz—the fundamental frequency—and plane resonance is clear at the 5th harmonic of 2GHz.

Timing and Skew

Skew refers to the time difference between any two single-ended signals. For instance, if a clock signal arrives at the receiver before an address signal then the skew may cause false triggering. Clock signals should always have the

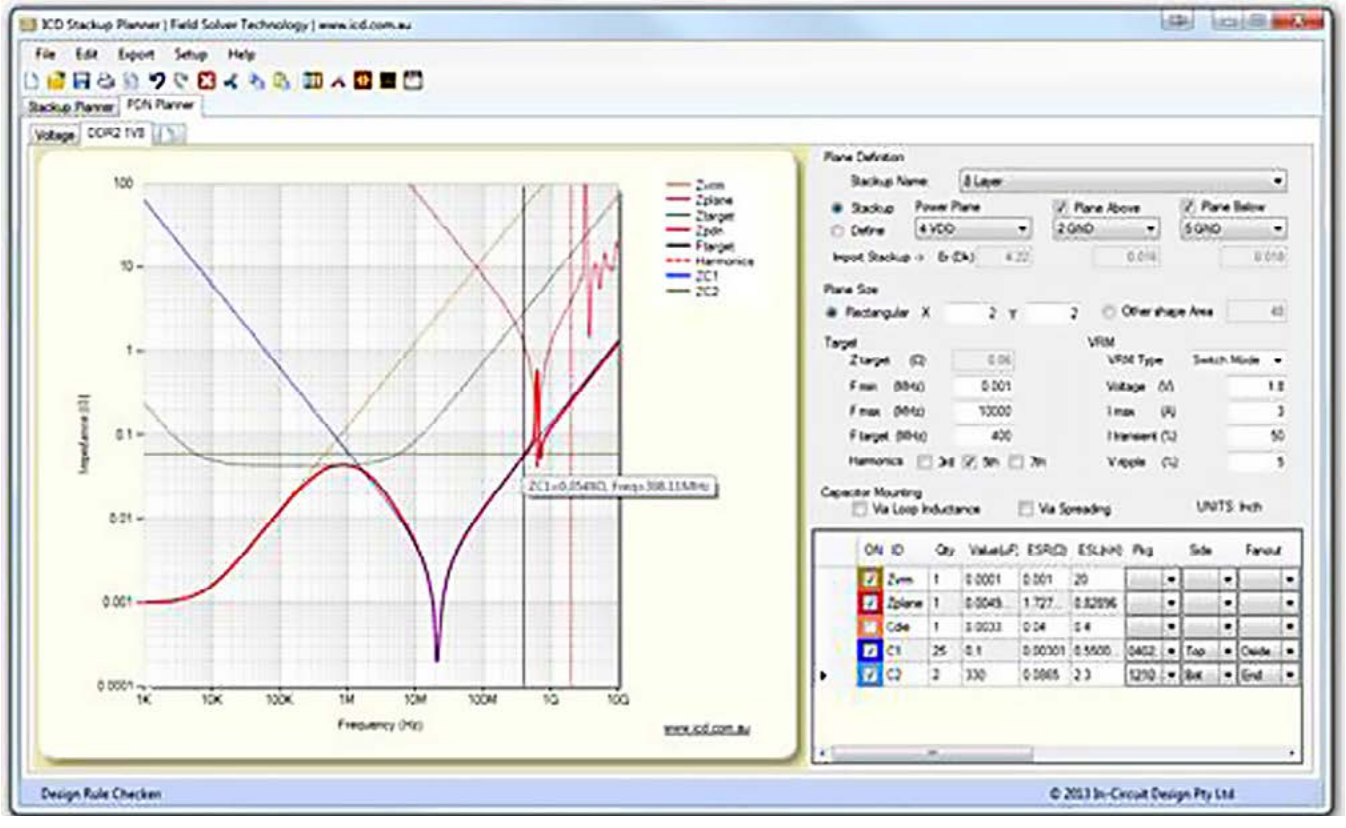

Figure 5: The 1.8V power distribution network of a DDR2 memory.

longest delay of the group, as the data, address, control and command signals need to settle down before the clock arrives at the chip sampling the bus.

Skew can also be the time difference of the two signals in a differential pair. Any mismatch in delay will result in changing part of the differential signal power into common-mode power. While skew is a timing problem, it is often caused by mismatched interconnects.

Ideally, the delay should be confirmed by simulation rather than by matched length. The length of the signal is not necessarily directly proportional to the delay. For instance for serpentine traces, forward crosstalk can increase the signal propagation even if the lengths are matched.

There are many other factors that can influence SI, but basically the stackup planning and the PDN analysis of a PCB are the two main factors that control the stability of a design. Getting these two factors right helps ensure the long-term reliability and performance of any high-speed digital design.

Points to remember:

- "There are two types of designers: Those that have signal integrity problems and those that will." —Sun Microsystems
- In order to reduce power consumption, IC manufacturers have moved to lower core voltages and higher operating frequencies, which of course mean high current requirements and faster edge rates. Faster edge rates mean reflections and signal quality problems
- The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a reduction in quality of the signal and possibly radiation of noise
- Rule of thumb: All drivers whose trace length (in inches) is equal to or greater than the rise time (in nanoseconds) must have provision for termination. It is the rise time rather than the frequency that is of concern
- Crosstalk can be coupled trace-to-trace on the same layer or can be broadside coupled by traces on adjacent layers. The coupling is three dimensional
- It is best to segregate groups of nets according to their signal amplitude to reduce crosstalk
- Rule of thumb: Gap = 3X trace width. Crosstalk plummets roughly quadratically with increased separation
- Set up parallel segment rules to prevent traces running in parallel for more than 500 mils
- Rule of thumb: Couple the signal traces closely to the plane. A 3mil thickness dielectric material reduces the crosstalk by approximately a quarter compared to the 6mil given the same trace spacing
- The goal of PDN analysis is to maintain low AC impedance, on the supply voltage planes, from DC to the maximum required frequency, including harmonics
- Clock signals should always have the longest delay of the group, as the data, address, control and command signals need to settle down before the clock arrives at the chip sampling the bus **PCBDESIGN**

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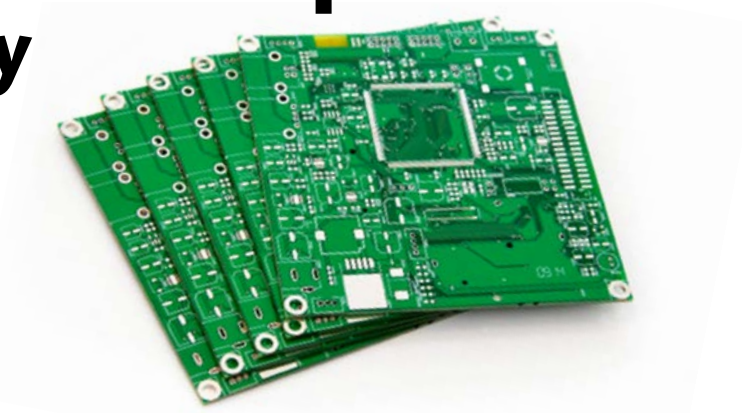
   – Beyond Design: Controlling the Beast
   – Beyond Design: Power Distribution Network Planning
   – Beyond Design: Skewed Again
   – The ICD Stackup and PDN Planner

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. ICD is a PCB design service bureau and specializing in board-level simulation. The company developed the ICD Stackup Planner and the ICD PDN Planner software. To read past columns or contact Olney, click here.

PCB Materials that Empower Signal Integrity



by John Coonrod
Rogers Corporation,
Advanced Circuit Materials Division

Signal integrity is a broad study of issues related to electrical performance. It can be associated with RF applications; however, it is more commonly related to high-speed digital concerns. Several attributes associated with circuit materials can contribute to good signal integrity.

Impedance control for PCBs is typically a concern when considering signal integrity. The factors impacting impedance control are circuit thickness, conductor width and spacing, copper thickness and the dielectric constant (Dk) of the material. There are interactions between these variables, but one point to consider is that the thickness of the circuit has much to do with how sensitive the other factors are to affecting impedance changes. A simple example is to consider a double-sided microstrip 50 ohm transmission line at two different thicknesses. Using a circuit with 10 mil thick material and a Dk of about 3.9, a conductor width change of 1 mil will cause about a 2.8% change in impedance. For a thinner circuit using the same material 4 mils thick, a conductor width change of 1 mil results in an impedance change of 6.8%.

Also considering the same example, the Dk control of the material is less sensitive to impedance change regardless of the circuit thickness. A difference of 0.1 for the Dk in the previous example will yield a difference in impedance of 1.1% for the 10 mil circuit and also 1.1% for the 4 mil circuit.

For circuits requiring a tight impedance tolerance, all aspects that can affect impedance should be considered. Even though Dk appears to be a relatively low concern, if a circuit has a tight impedance tolerance such as ± 5%, then obviously Dk control is worth considering. The laminates used in the high-frequency segment are formulated for tightly controlled Dk tolerance and should be used for applications where the impedance tolerance has a narrow specification.

Circuit thickness is a driving factor for many variables associated with impedance change and given this consideration, the best circuit fabrication process should be used to have good thickness control. Most digital PCBs are multilayers, and with regard to the previous microstrip example, that circuit would be on the outer two copper layers of the PCB. These layers could be created by a foil lamination using prepreg or a core lamination using a laminate. Most high-frequency laminates have a tightly controlled thickness tolerance. It generally makes more sense to use the core lamination process with one of these laminates as opposed to the foil lamination in order to get a circuit with better thickness control.

Over the past few years, more attention has been placed on insertion loss for digital PCBs. One of several reasons for this is signal integrity. A circuit with higher insertion loss will cause a digital signal to lose amplitude, which will affect the integrity of the pulse shape. Additionally, all circuit materials have an increase in dissipation factor with an increase in frequency, which generally means that the insertion loss will be worse for higher frequencies.

Digital pulses are formulated from multiple RF waveforms at different frequencies. High speed digital signals are formulated by using a fundamental frequency, combined with multiples (harmonics) of that frequency. Generally speaking, a digital signal at a rate of 1 Gbit/s will use multiple analog waves. The fundamental analog frequency will be 0.5 GHz and multiples of

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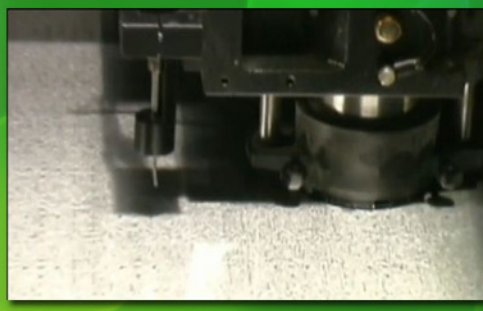

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this frequency are 1.5 GHz, 2.5 GHz, etc. If the material dissipation factor changes significantly from 0.5 GHz to 2.5 GHz, that will impact the formation of the digital signal and can be an issue for signal integrity. Many PCB materials do not have a significant difference in dissipation factor across this range of frequencies. However, this issue can be a very different concern for rates that are much faster.

There are now many high-speed digital applications at 10 Gbit/s and higher. These applications use a fundamental frequency of 5 GHz and harmonics of 15 GHz, 25 GHz, etc. In this range of frequencies, most common PCB materials will have a very significant difference in dissipation factor and cause serious signal integrity issues. This is one reason high-speed digital PCBs are using special circuit materials that are formulated for high-frequency applications. These materials are formulated for having a low dissipation factor with minimal change across a wide range of frequencies. The materials have been used historically in high frequency RF applications and even now used in applications of 77 GHz and higher. Besides the dissipation factor improvement, the materials are formulated for tight thickness control and Dk control, both being beneficial to signal integrity.

Signal integrity issues continue to become more complex as speeds increase. Understanding the attributes of high-frequency circuit materials can be very advantageous in minimizing signal integrity issues. When dealing with signal integrity issues, your material supplier can help you choose the appropriate circuit material to achieve the best performance from your particular technology. **PCBDESIGN**

John Coonrod is a market development engineer for Rogers Corporation, Advance Circuit Materials Division. To contact Coonrod, click here.

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Micro-Waves, Macro-Challenges

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John Coonrod talks to Guest Editor Kelly Dack about Rogers Corporation's high-frequency laminates and his paper about the topic of insertion loss and how Rogers materials, combined with prudent design and manufacturing methods, are solving the industries most challenging microwave challenges.

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CONNECTING THE DOTS

The CAD Library, Part 2

by Jack Olson, CID+
PADSTACKS

When we left off last month, we were using the simple example of a capacitor connected to vias, which are the plated holes that connect conductive layers together. Let's take a quick look at plated holes, because they can also be stored as library parts.

Holes of various diameters will be needed for vias. Vias will be used for circuit board mounting holes, for leaded components and for SMT components that require holes for alignment pins or for additional mechanical support.

The elements for a plated hole are created using the same method as the surface mount capacitor in the previous example, with the addition of a drilled-hole definition. We won't need anything on the silkscreen layers, but we will need an opening in the top and bottom solder mask layers. We also need a conductive shape for the surface layers, usually round instead of rectangular, and we may also need round pads on the internal signal layers.

You may prefer different diameters on different layers, an approach that most CAD systems support. Plane layers are treated differently than signal layers, because if the plated hole is connected to the plane we will often use a shape that will provide thermal relief (we'll cover thermal relief later), but if it is not connected to the plane we need to add a clearance diameter. As vias or other plated hole types are used in the design, the CAD software will assign connection or clearance shapes automatically, as needed.

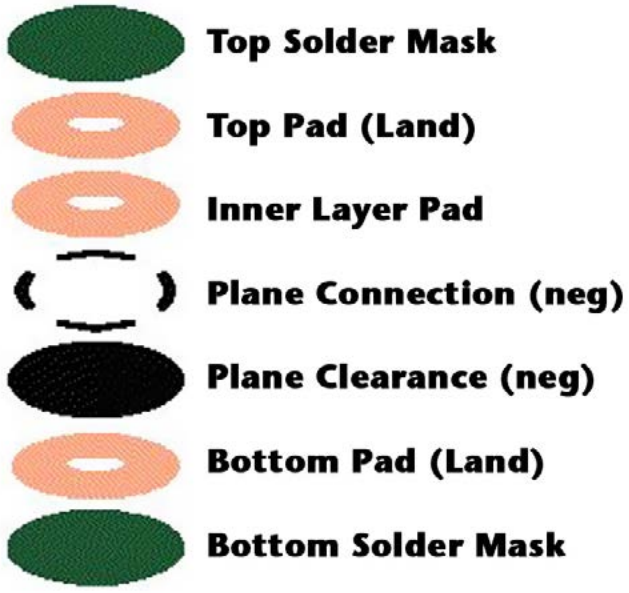
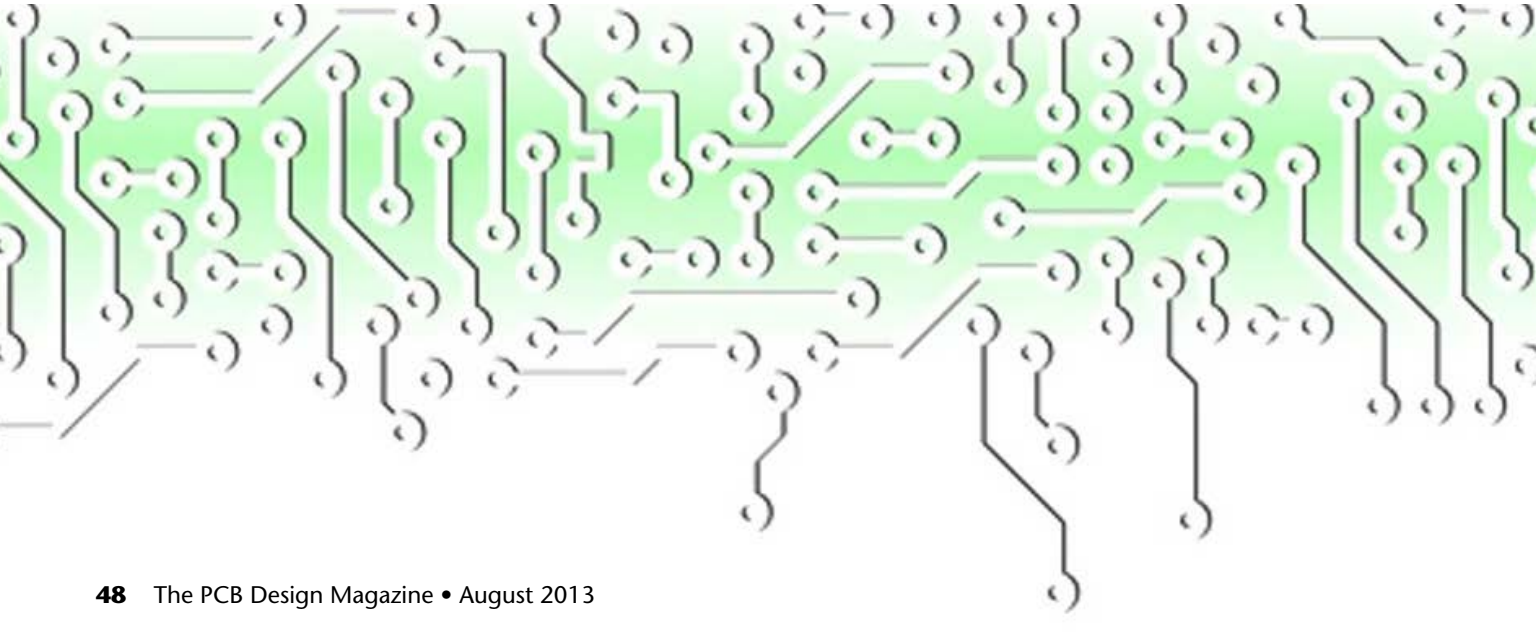


Figure 1: Padstack for a plated hole.



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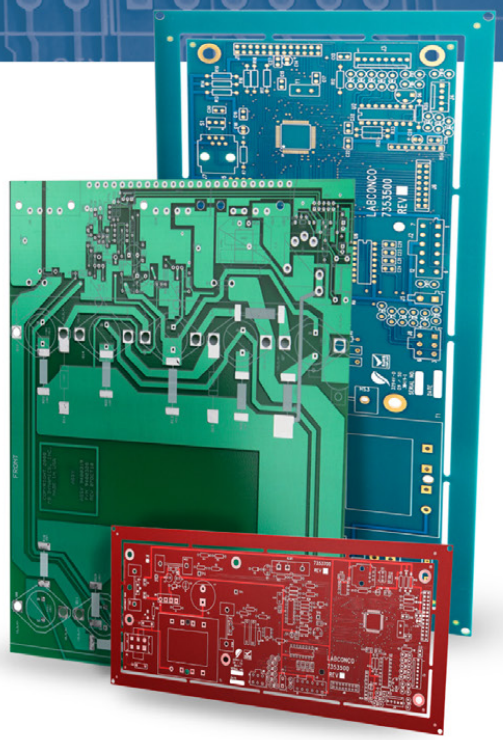

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THE CAD LIBRARY, PART 2 *continues*

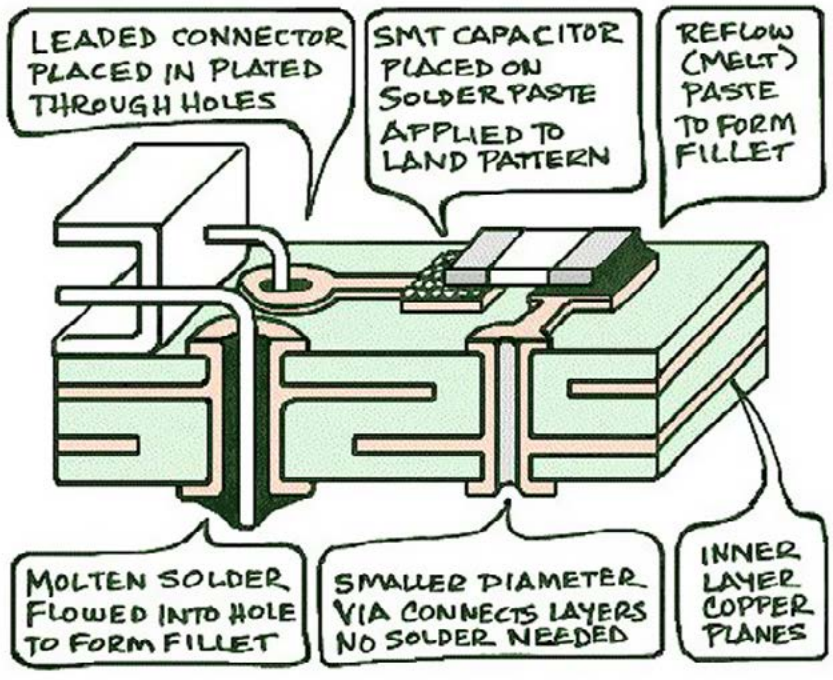

Figure 2: Electronic assembly.

As you can see in Figure 2, the end-result will be a stack of various diameter pads, which is where the term "padstack" comes from. And now that I'm on the subject of terminology, let me introduce another term you should know: annular ring. When the pads are drilled to make a hole through the center of the padstack, the result is that the pads look more like donuts than circles. The remaining amount of copper is called the annular ring. Minimum annular ring size is an important concept that we will look at later.

Additional Library Features

Eventually, you will develop a working library that will contain reusable footprints or land patterns for all of the components in your designs, and also padstacks of various hole diameters that you will use for different via sizes, component lead diameters, and mounting hardware.

So far, we have only described the features of a library component that are required for manufacturing the circuit board itself. Bare board fabrication data include the required finished diameters of holes, the conductive land pattern for soldering component leads or terminations, silkscreen graphics that might include component outlines in addition to the reference designator, and soldermask clearances. All of these features are built into the library for each component, but there are additional features that can be stored as part of the library definition that can aid in maintaining minimum spacing between components during the component placement phase of the circuit board layout process, and features that will be helpful for electronic assembly and documentation.

The first of these additional features is the definition of paste mask for surface mount components. Figure 2 might help to illustrate the concept of paste mask graphics.

There is much to learn about electronics manufacturing, but briefly, the surface mount components are usually soldered using a different process than the through-hole components. Solder paste is applied to the conductive lands using a stainless steel paste screen, and then the components are placed on the paste. The whole assembly is then heated in an oven until the solder melts, attaching the component to the board. This establishes the electrical connection and also provides the mechanical attachment.

That's as far as we're going to go on the subject of assembly right now, but the intention is to illustrate that most modern designs require an additional layer of artwork to describe the paste mask. You wouldn't want to manually design a paste screen for each circuit board. It is far more effective to include the paste area on a separate CAD layer in the library for the surface mounted components. Unless you are working very closely with your assembly partner and know their particular paste screen preferences, it is best to make the paste screen area exactly the same size as the land area. The paste screen manufacturer will make adjustments to these sizes as needed for their process requirements.

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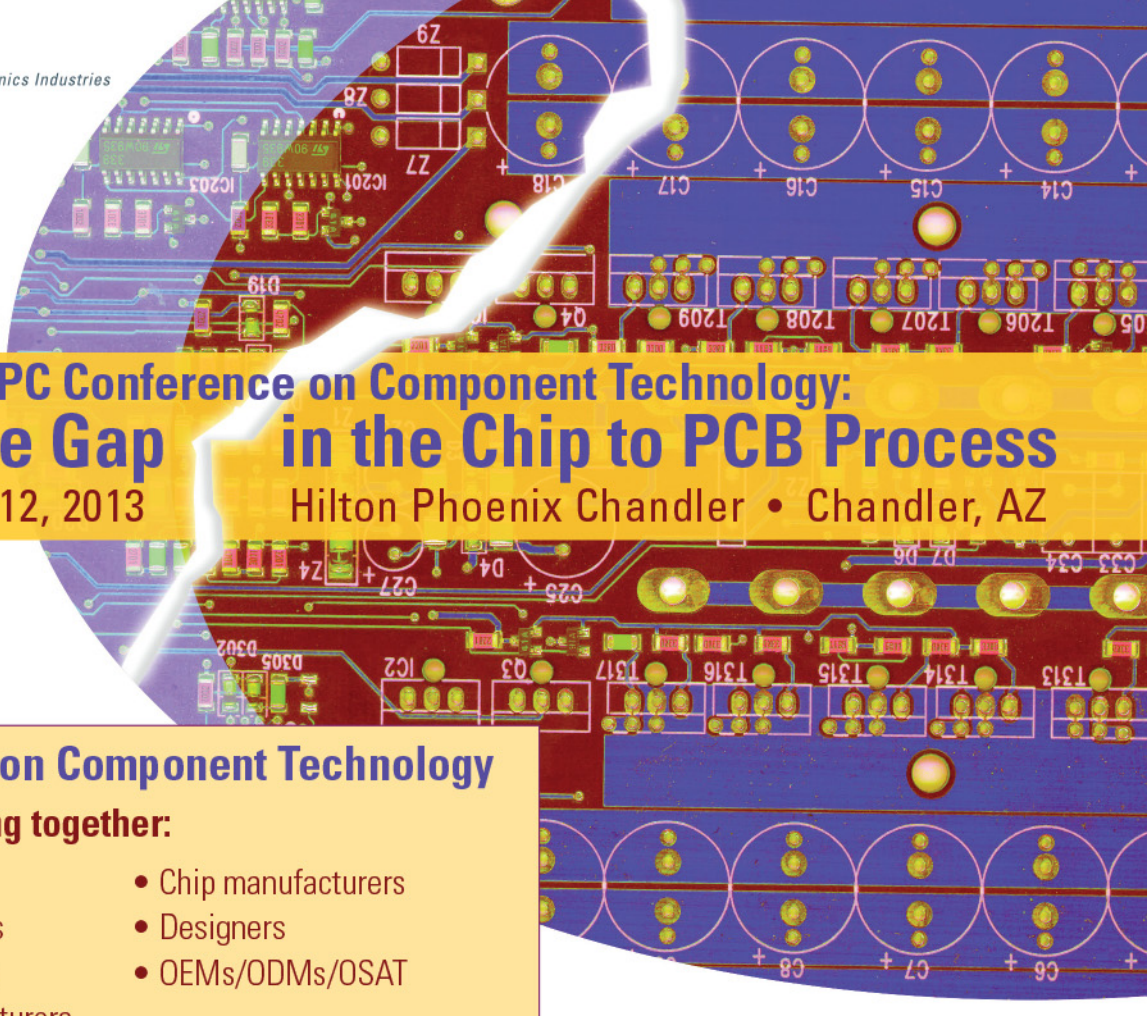

IPC Conference on Component Technology:

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This event will bring together:

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The path to successful IC-to-package-to-board-level-interconnect encounters many obstacles along the way. Finding the right materials, equipment and processes is critical. IPC, with event host Amkor Technology, is presenting the ***IPC Conference on Component Technology: Closing the Gap in the Chip to PCB Process*** to help the PCB supply chain and chip manufacturers address the many technology challenges in IC-to-board-level interconnections.

With an emphasis on design and manufacturing of component technology to interconnection solutions, the event will tackle the latest advancements and discoveries. Don't miss this opportunity to learn from the experts!

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THE CAD LIBRARY, PART 2 *continues*

The second point I'd like to make is that most CAD systems support the concept of "keepout areas." You may decide that for a particular component, you don't want any vias or routed traces underneath, or maybe you want to control planes or copper fills around or underneath a component. Some software packages support all three of those separately, and you can define routing keepouts, via keepouts and area fill cutouts. You may be able to define a placement border a specific distance away from the component body, which will automatically maintain a minimum distance between components during the placement phase of the design.

There might also be a separate layer for assembly documentation. On dense designs it is sometimes difficult to add meaningful graphics and nomenclature to the silkscreen layers, but you might be able to turn on a different layer when creating the assembly drawing to show the components more realistically. There are advantages to reducing the silkscreen graphics on the bare board itself, especially for high volume products. Some designers are starting to remove everything except the "pin one" indicator or a polarity mark on the board to show the proper orientation of the component, and then using a more descriptive graphic on the drawings.

The implementation of the features mentioned here might vary depending on the particular brand of CAD software you are using, but I strongly encourage you to learn the capabilities of your software, and try to take full advantage of the features it provides for library management. Build as much intelligence into your library as possible.

OK, I have two more quick notes related to assembly that I need to squeeze in before we move on. The first is another new term, the "fiducial." A fiducial is an optical target placed on the circuit board that the assembly equipment can use as a reference point. Your library may already have one available for you to use, but if it doesn't, create a component that is simply a 1 mm round dot on the surface copper layer, and create a solder mask opening that is 3 mm diameter. If you can, create a 3 mm placement keepout, too. You want to keep everything away from the fiducial so the assembly camera doesn't get confused. It is best to place three fiducials orthogonally on the outside edges of the board or array (as far apart as possible), and make sure you put them on the back too, if you have SMT parts on both sides.

Finally, it will be helpful to the assembler if you create your library components using the same orientation as they are packaged by the component manufacturer. For example, polarized capacitors are packaged horizontally with the polarity mark on the left. The assembly equipment considers this to be "zero degree rotation" for that type of part. When you package a schematic, the components will be loaded into your design in what the CAD system thinks is zero-degree rotation, which will be the orientation of the components the way you built it in the library. Just as a simple thought experiment, imagine that you were able to place all of your parts and complete the design without ever manually rotating a part. When you create the assembly placement data, all of your components will be listed as "rotation 0." But will your zero rotations match the assembler's zero rotations?

If not, they will have to make adjustments to your data. If you built your polarized capacitor vertically instead of horizontally in your library, your rotation will always be at least 90 degrees different than theirs. I just wanted to mention that, but don't worry too much if you don't know what the orientation will be from the manufacturer. The industry does not always agree on the proper orientation for some types of components, but the assembler will adjust your data to match their equipment. If you have a choice, build your library parts in the same orientation as the component data sheet shows. **PCBDESIGN**

Jack Olson, CID+, has been designing circuit boards full-time for over 20 years. He would again like to thank Tom Hausherr of PCB Libraries for his continuing efforts to systemize and standardize CAD library development.
To contact Olson click here.

Mil/Aero007 News Highlights

FTG, TPC Form JV to Supply PCBs to Aerospace Market

The joint venture will build on the strong customer base FTG has in the aerospace market as well as FTG's knowledge and expertise of aerospace technical and quality requirements; this will be combined with TPC's established manufacturing facilities in Tianjin, China.

Westak Awarded MIL-PRF-31032 Certification

Westak has successfully achieved certification and qualification to MIL-PRF-31032 for its Forest Grove, Oregon manufacturing facility. The certification was awarded in recognition of the company's advanced quality management system and production processes that meet the stringent requirements of the standard.

FTG Circuits Segment Sales Down $1.4M or 13% in Q2

"The second quarter of 2013 saw a return to profitability for FTG while we continued to invest in technology and facilities across the corporation. Obviously, the joint venture we announced with TPC is an important strategic investment and will provide an exciting new solution for our customers," stated Brad Bourne, president and CEO.

Commercial Aero Revenue Up 16.2%; Defense Down 1.3%

The study found that in 2012, commercial aerospace revenues significantly increased and more than made up for declines in the defense segment. Commercial aircraft segment revenues increased 16.2% or US $38.4 billion in 2012, while defense segment revenues decreased 1.3%, for a combined increase of 5.9%, up from a 1.6% increase in 2011.

Global UAV Market to Reach $89B in Next 10 Years

"The UAV market is evolving, it is becoming an increasingly international market as it grows," said Philip Finnegan, Teal Group's director of corporate analysis and an author of the study. "UAVs have proved their value in Iraq and Afghanistan and are being sought by a growing number of militaries worldwide."

Asia's Defence Budgets to Outpace North America's by 2021

Asia Pacific budgets are set to outstrip the U.S. and Canada by 2021, fuelled by an explosion in global arms trade that threatens the competitive edge and dominance of the U.S., the UK, and European defence trade according to the biggest budget and export study since the economic downturn.

Report: U.S. Electronic Security Industry Outlook to 2017

The U.S. has been the largest market for the electronic security products worldwide for several past years. The demand for the electronic security systems continues to be driven by a high perceived risk of crime, despite a long-term trend of falling crime rates.

Business & Commercial Aircraft Market Forecast Released

As the business and commercial aircraft markets continue to recover from the industry downturn, signs of forward momentum are beginning to emerge. Demand for new aircraft orders will continue to come from established and developed markets, and the growth potential in emerging markets such as China, India, Russia, and Latin America is predicted to play an increasingly important role in the global aviation marketplace.

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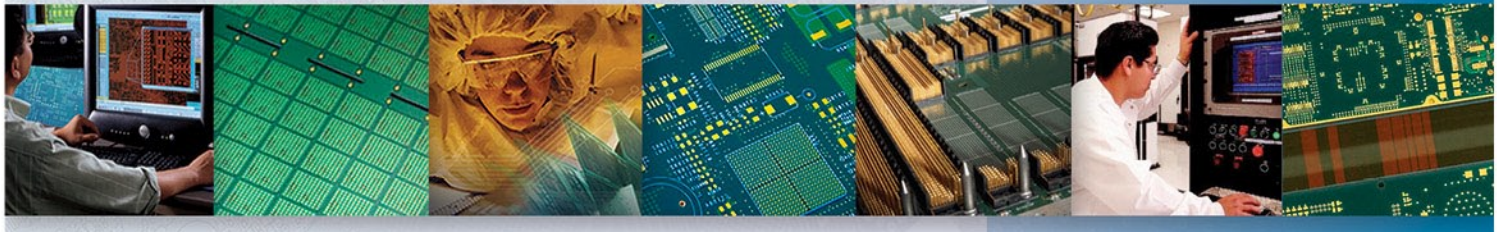

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New Material May Transfer Heat More Effectively

A team of physicists at the U.S. Naval Research Laboratory (NRL) and Boston College has identified cubic boron arsenide as a material with an extraordinarily high thermal conductivity and the potential to transfer heat more effectively from electronic devices than diamond. This work provides new insight into the nature of thermal transport at a quantitative level and predicts a new material, with ultra-high thermal conductivity, of potential interest for passive cooling applications.

Calculating the thermal conductivity of cubic III-V boron compounds using a predictive first principles approach, the team has found boron arsenide to have a remarkable room temperature thermal conductivity, greater than 2,000 watts per meter per degree Kelvin (>2000 $Wm^{-1}K^{-1}$). This is comparable to those in diamond and graphite, which are the highest bulk values known.

Unlike metals, where the electrons carry the heat, diamond and boron arsenide are electrical insulators. For the latter type of materials heat is carried by vibrational waves (phonons) of the constituent atoms, and intrinsic resistance to heat flow results from these waves scattering from one another. Diamond is of interest for cooling applications but it is scarce and its synthetic fabrication suffers from slow growth rates, high costs and low quality. However, little progress has been made to date in identifying new high thermally conductive materials.

This research, supported in part by the Office of Naval Research (ONR) and the Defense Advanced Research Projects Agency (DARPA), gives important new insight into the physics of thermal transport in materials, and it illustrates the power of modern computational techniques in making quantitative predictions for materials whose properties have yet to be measured.

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TOP TEN

News Highlights from PCBDesign007 this Month

① Mentor PCB Forum Arrives in U.S., Canada

The Mentor PCB Forum, a series of Mentor Graphics seminars that attracted hundreds of users in Europe earlier this year, is now coming to the United States and Canada.

② EMA Enhances CircuitSpace

"CircuitSpace enables engineers to expedite the PCB design requirements with a higher level of quality and reproducibility from the placement phase of the design cycle through design review and verification," said Manny Marcano, president and CEO. "We strive to continue to innovate with our technology to make life easier for PCB designers."

③ FabStream Releases SoloPCB Design Software V1.1

"The market reaction and response to FabStream and SoloPCB has been very positive," said Rick Almeida, managing director of FabStream. "The feedback we've received during the beta pilot phase has strengthened an already powerful design alternative for DIY engineers who need access to quality PCB design software and manufacturing.

④ ODB++ Solutions Alliance Launches New Video

Visit the ODB++ Solutions Alliance Resources page to see a new video presentation titled "How to Implement ODB++." This informative real-world presentation will guide you through the process of creating and using an ODB++ file, and how to best use it to improve your NPI process.

5 ICD Stackup Planner Incorporates Via Span Definitions

The Via Span Definitions enhance and clarify the graphics display and provide the automatically generated fabrication drawing with the additional information required to build an HDI board," said Managing Director Barry Olney. "With this release, we have also incorporated over 2,000 new materials into the Dielectric Materials Library, bringing the total count to over 5,650."

6 IPC, JPCA: New Design Guidelines for Printed Electronics

"IPC will continue its work on the design guidelines, in collaboration with JPCA, to secure additional companies' experiences. We encourage companies with expertise in this area to help by participating in the continuing international consensus-building committee process," says IPC Director of Technology Transfer Marc Carter.

7 Cadence Reports Revenue of $362 Million in Q2

Cadence reported second quarter 2013 revenue of $362 million, compared to revenue of $326 million reported for the same period in 2012. "Integration of our recent acquisitions is going smoothly as we continue to execute and generate solid financial performance," said Geoff Ribar, senior vice president and CFO.

8 AWR Releases Millimeter Wave Wireless App Note

A new application note from AWR highlights the use of the company's Microwave Office circuit design software to develop a Q- to E-band doubler and a K- to E-band quadrupler circuit (including a medium E-band power amplifier) for millimeter-wave wireless systems. The design effort resulted in an increase in gain as well as output power, two critical criteria for E-band systems.

9 AltiumLive Now Includes Board-Level Design Content

This release delivers board-level component models and corresponding supply chain information, such as real-time price and availability data from distributors and vendors including Digi-Key, Mouser and Farnell, directly to designers using Altium Designer.

10 CST Releases STUDIO SUITE 2013 Service Pack 2

Service Pack 2 includes several new features demanded by customers. These features cover a range of applications, from PCBs and MIMO antenna arrays to accelerator cavities and low-frequency devices.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the complete Calendar of Design Events, click here.

Philadelphia Expo & Tech Forum
August 15, 2013
Cherry Hill, New Jersey, USA

NEPCON South China
August 27–29, 2013
Shenzhen, China

IPCA EXPO 2013
August 29–31, 2013
Gujarat, India

NEXTGEN AHEAD
September 9–11, 2013
Washington, DC, USA

International Test Conference 2013
September 10–12, 2013
Anaheim, California, USA

Capital Expo & Tech Forum
September 10, 2013
Laurel, Maryland, USA

2013 MEPTEC
September 17–18, 2013
Tempe, Arizona, USA

Failure Analysis of Electronics Short Course (CALCE)
September 17–20, 2013
College Park, Maryland, USA

Electronics Operating in Harsh Environments Workshop
September 17, 2013
Cork, Ireland

MRO EUROPE 2013
September 24–26, 2013
London, UK

ID WORLD Rio de Janeiro 2013
September 26–27, 2013
Rio de Janeiro, Brazil

SAE 2013 Counterfeit Parts Avoidance Symposium
September 27, 2013
Montreal, Quebec, Canada

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

PUBLISHER: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:
GROUP EDITORIAL DIRECTOR: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

MANAGING EDITOR: **ANDY SHAUGHNESSY**
(404) 806-0508; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:
PRODUCTION MANAGER: **MIKE RADOGNA**
mike@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA**

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Next Month in *The PCB Design Magazine:* Materials

Matching the right PCB material for your board's requirements can be a daunting task, especially when designing high-speed PCBs. In the September issue of *The PCB Design Magazine,* our experts make sense of the myriad of materials available today.