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Fabrication Notes

Do you hand off perfect fab notes to your fabricator? If this month's content is any indication, the answer is likely, "No." But this isn't about designers handing off bad data; the problem goes much deeper than that. This month, we decipher the process of creating fab notes, define what should and should not go into a design data package, and discuss what can be done to eliminate that dreaded afternoon phone call.

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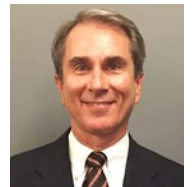


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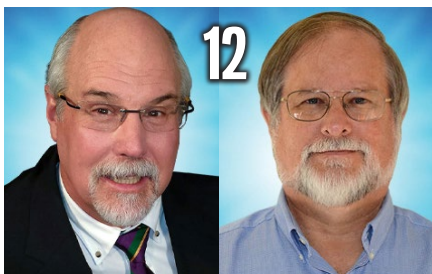


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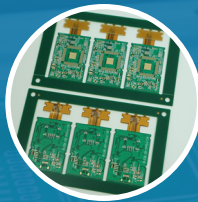
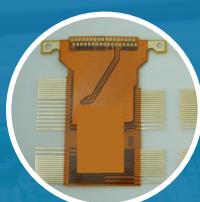
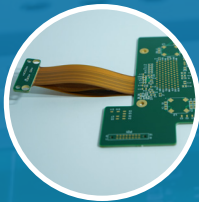
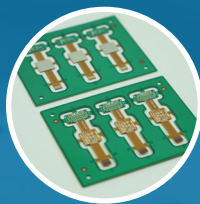
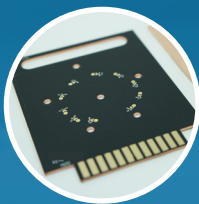
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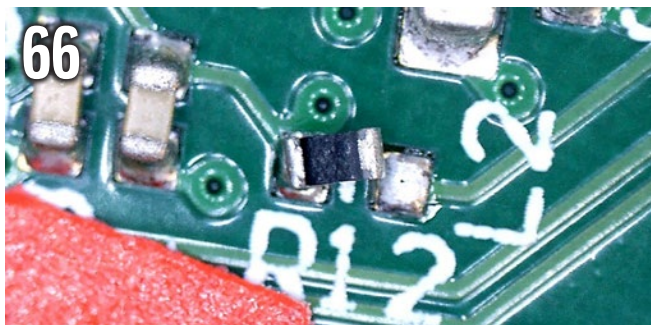


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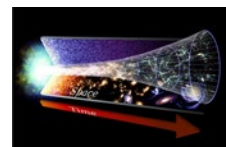


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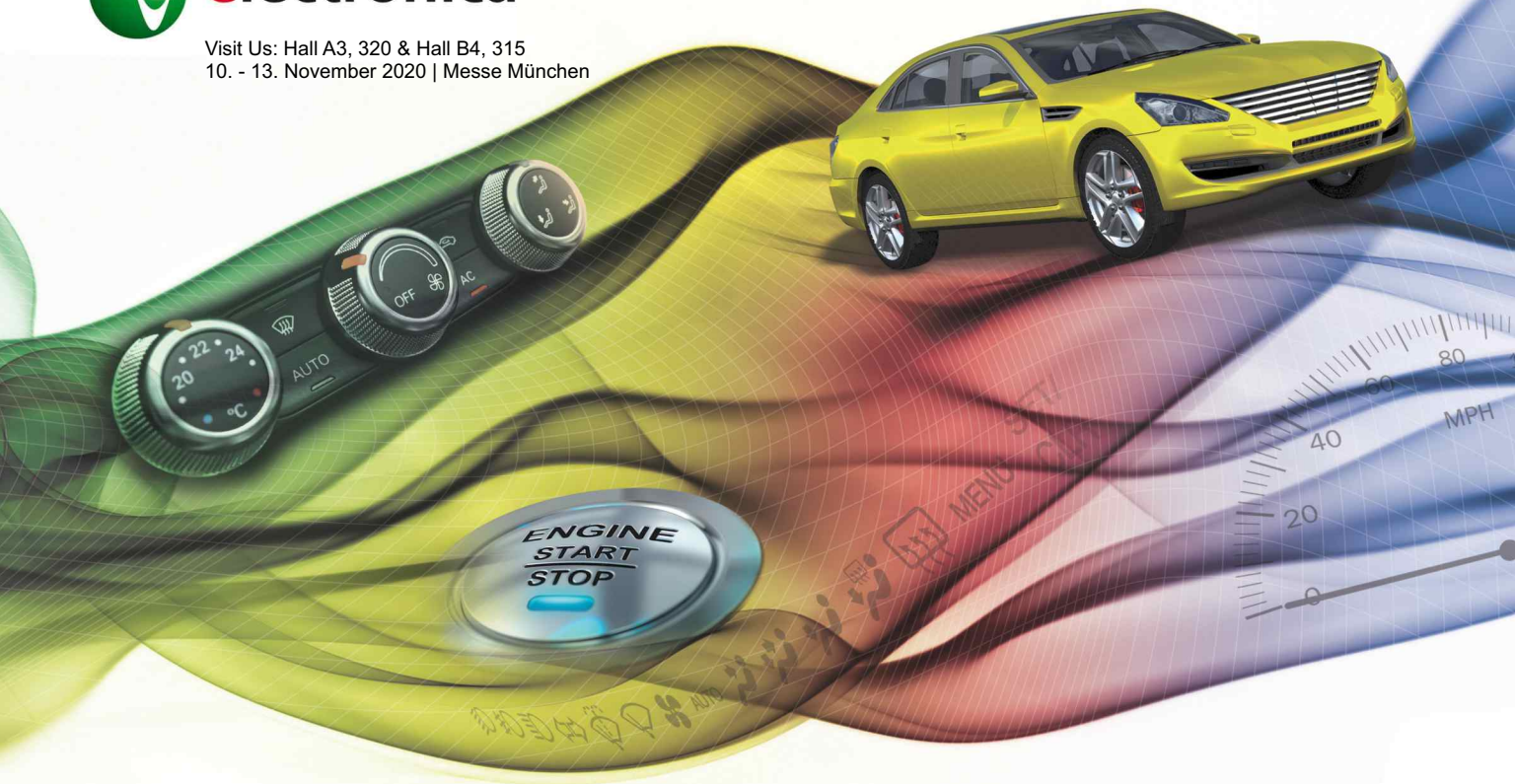
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This Month in Flex

Getting your fab notes correct and complete can be challenging enough, but the task is amplified for flexible circuit designers, who must convey 3D flex design intent to the manufacturer. Communication is king here, and accurate fab notes are the currency of the realm.

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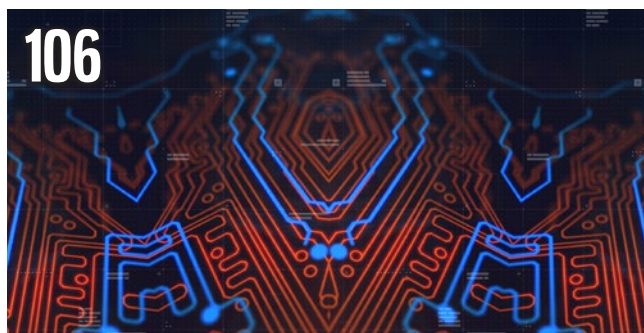
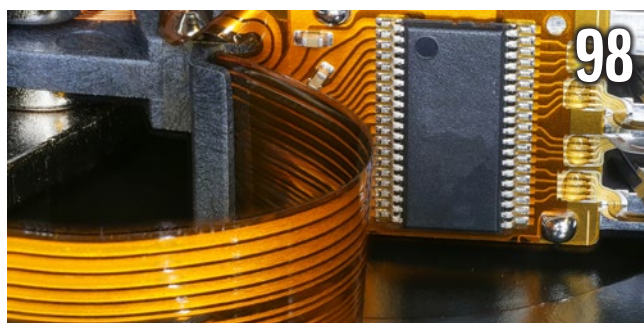
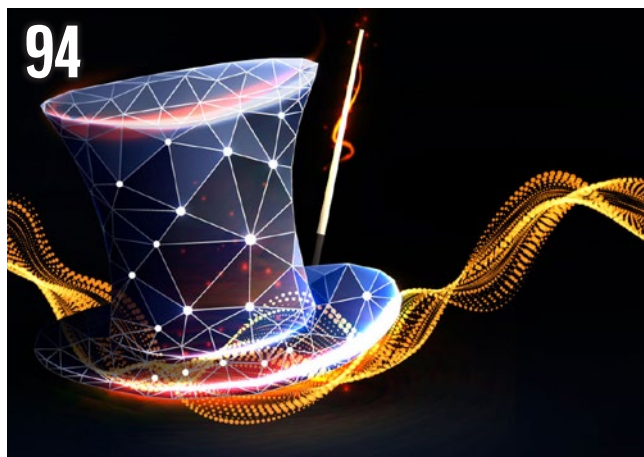
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Erroneous Fab Notes: Don't Blame the Designer

The Shaughnessy Report
by Andy Shaughnessy, I-CONNECT007

Do you hand off perfect fab notes to your fabricator? If this month's content is any indication, the answer is likely, "No." And you may not even know that your fab notes are incomplete or incorrect because your CAM engineers have been fixing your data for so long that it's become part of their job description.

But this isn't about designers handing off bad data; the problem goes much deeper than that. In fact, we really can't blame designers for a situation that they didn't create.

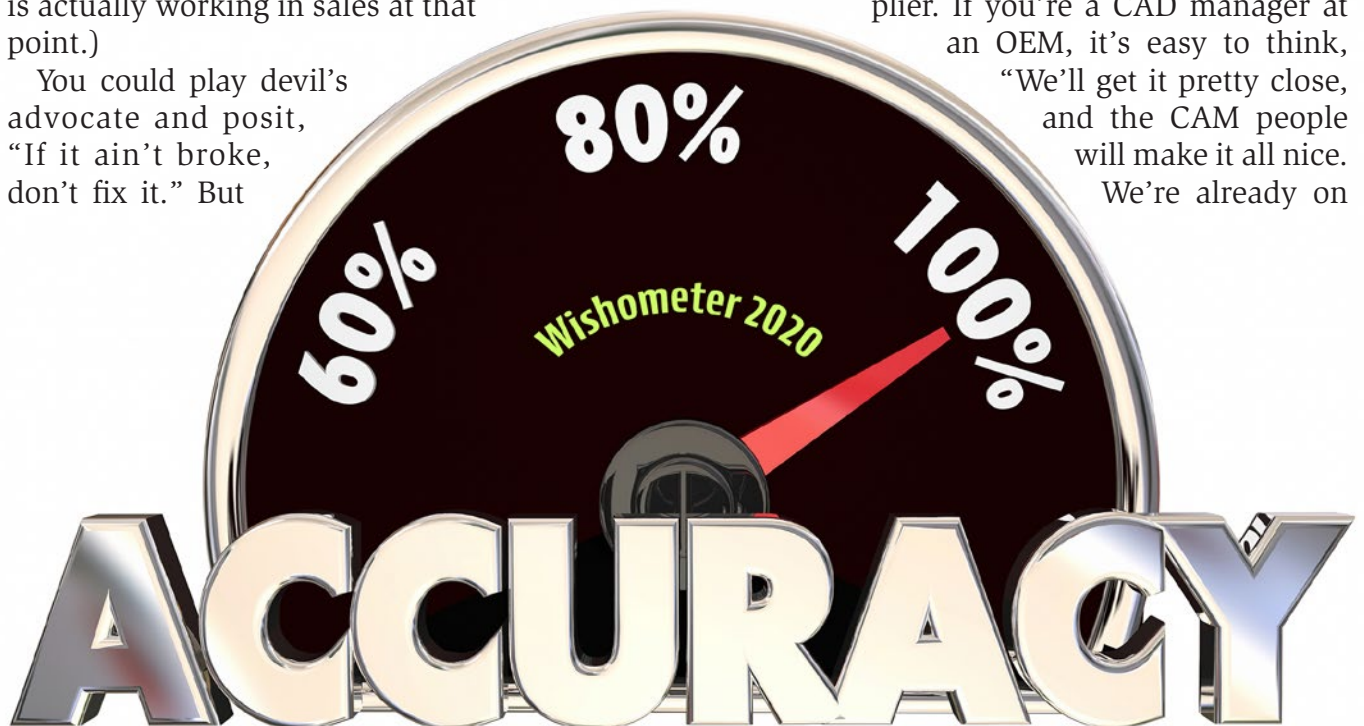
The system has enabled designers to continue sending out less than perfect fab notes—in effect, making the board shop's CAM department the final step in the design process. Some CAM engineers spend eight hours tweaking one data package, often before the fabricator even gets the job. (The CAM department is actually working in sales at that point.)

You could play devil's advocate and posit, "If it ain't broke, don't fix it." But

there are consequences for the OEM that hands off imperfect data, including time to market (which equals lost revenue) and weekend calls from the CAM department. But these ramifications are all "baked in the cake" at this point, and the actors seem to have accepted their roles.

What exactly does a fabricator need from a designer in the first place? We posited that question to Dana Korf, formerly the chief PCB technologist at Huawei. He answered, "Give me all of the data I need to build the board right the first time. Don't tell me how to do it; tell me what you need."

That clearly isn't happening very often. Some fabricators say that 90% of all new customers hand off inaccurate or missing data. But the CAM department's data-tweaking services make that fabricator an attractive supplier. If you're a CAD manager at an OEM, it's easy to think, "We'll get it pretty close, and the CAM people will make it all nice. We're already on



to the next design now, so don't bother me. Build the board."

Fabricators are caught in the middle. But what if fabricators started offering incentives for jobs that arrived with perfect data packages? The small- and medium-sized OEMs, especially startups, might just jump at such an offer. If board shops monetized the documentation process, I bet we'd see the percentages of imperfect data start to trend downward.

This month, we shine a light on the process of creating fab notes, define what should and should not go into a design data package, and what—if anything—can be done to eliminate that 5:30 p.m. call to the OEM on Friday night. We start with a conversation with columnists Dana Korf and Kelly Dack, who delve into the challenges of creating accurate fab notes, and the need to include all of the relevant data. Veteran CAD man Mark Thompson explains how easy it is to get design data right—and wrong—and he shares some of his tips for creating great fab notes. Rick Almeida and Ray Fugitt of DownStream Technologies address what happens to incorrect fab notes in the CAD department, the role EDA tools can play in this situation, and how the current system enables designers to continue to keep handing off erroneous data.

Next, Jennifer Kolar and Dan Warren of Monsoon Solutions discuss the importance of com-

municating with your fabricators and why they almost never get calls from a CAM department regarding their documentation. Patrick McGoff of Mentor, a Siemens Business, offers advice to new designers facing fab notes challenges and explains how intelligent file formats like ODB++ help eliminate miscues during the data handoff process. Tara Dunn illustrates how flex fab notes differ from their rigid PCB brethren, as well as how the 3D structure of flex presents even more data challenges.

We also bring you columns from Barry Olney, Istvan Novak, Kelly Dack, Patrick Crawford, Phil Kinner, John Coonrod, Matt Stevenson and Bob Tise, and Dominique Numakura. We also have a great article by Olga Scheglov, CID+, on design rules for new flex designers.

There's still a lot of craziness going on in the world right now, but we continue to see amazing examples of innovation in this industry. When COVID-19 is a thing of the past, this industry is going to blast off. The only question is, "When?" See you next month. **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 20 years. He can be reached by clicking [here](#).

Secretary Elaine Chao Unveils Guidance Document for Regulation of Hyperloop

U.S. Department of Transportation Secretary Elaine Chao and the Non-Traditional and Emerging Transportation Technology (NETT) Council unveiled the guidance document on a clear regulatory framework for hyperloop in the United States.

"This guidance bridges the gap between innovator and regulator, prioritizes safety during development without hampering innovation, and promotes mutual awareness between industry and government," said Chao.

The regulatory guidance document for hyperloop is the first of its kind in the world, further proving that the US intends to be the leader in the industry.

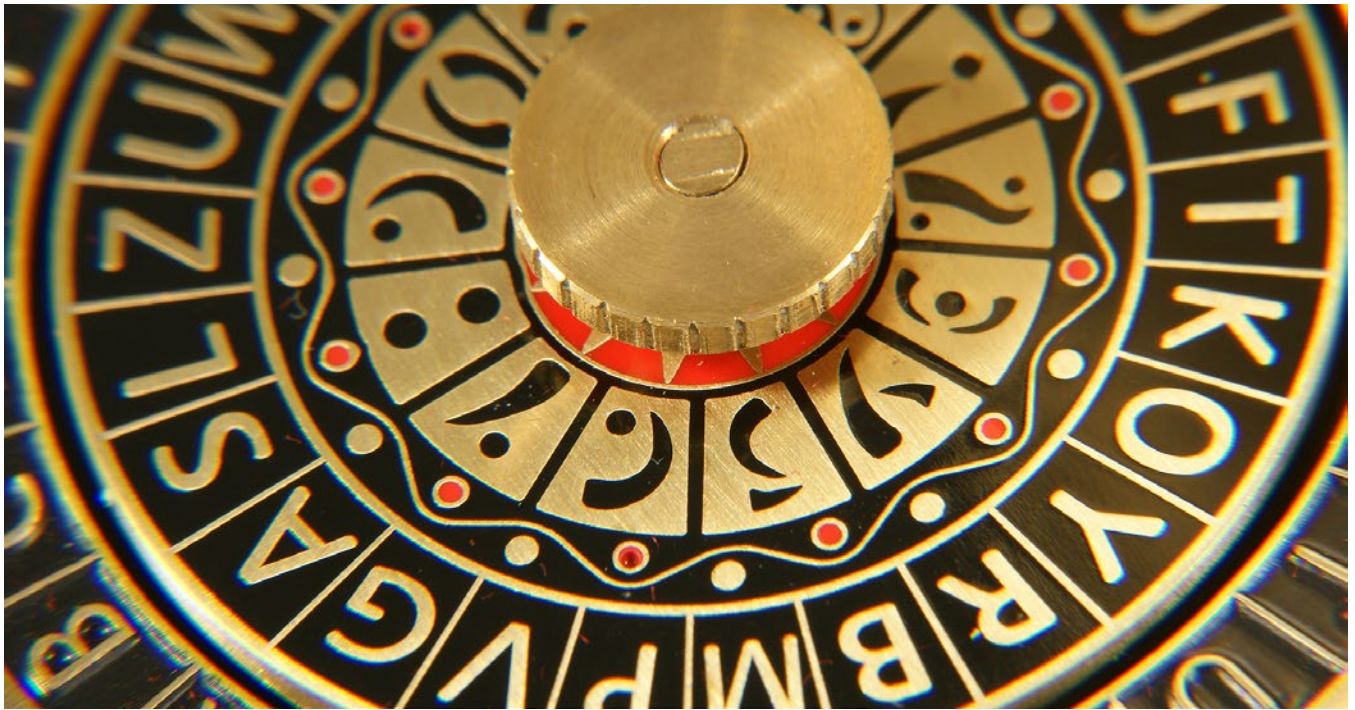
"Secretary Chao and the NETT Council are working at an unprecedented speed

to ensure that the United States is at the forefront of hyperloop development," said Jay Walder, CEO of Virgin Hyperloop. "It's clear that the USDOT shares our vision for infrastructure development as a way for the country to not just rebuild, but evolve as we emerge from this crisis."

As an entirely new category of transportation, hyperloop will unlock exponential growth opportunities for cross-industry manufacturing and development jobs, across construction, aerospace, rail, automotive, aviation, electric vehicles, and autonomous control. Last month, Virgin Hyperloop announced a partnership with Spirit AeroSystems, one of the world's largest aerospace manufacturers.

(Source: Globe Newswire)





Deciphering **Fab Notes**

Feature Interview by the I-Connect007 Editorial Team

When we started planning this issue on fab notes, we knew we'd have to speak with [Dana Korf](#) and [Kelly Dack](#). Dana is the former chief PCB technologist for Huawei and a front-end director for PCB board manufacturers, such as Multek, Sanmina, HADCO and Zycon. Dana has made a point of working with designers and helping them provide accurate fab notes and documentation each time. Kelly Dack has been dealing with (and correcting) error-filled and incomplete fab notes for years. In this wide-ranging discussion, Dana and Kelly explain some of the challenges they encounter with fab notes, and what designers can do to create better documents and head off that dreaded phone call at 5:30 p.m. Friday.

Andy Shaughnessy: Dana, why don't you give us an overview of what manufacturing notes are and their main function in the design process.

Dana Korf: When we talk about fab notes, to me, the fab print is the main document, along with

the graphical data, which has critical information like the stackup, drill tables, some dimensioning and tolerancing, and then—down the left-hand side—a series of notes where people talk about a lot of things. The fab notes will reference materials, solder mask type, laminate types, copper maybe, reference off their acceptability specs, and then some miscellaneous comments about the design—all telling the fabricator or assembler what to do or not to do.

Shaughnessy: They all fit under the umbrella term of manufacturing notes, correct?

Korf: I'd say most of the notes are manufacturing-related. "Here's what to do or not to do." Very rarely do you get design-related notes. Probably the most common ones I've seen are around signal integrity. "I want this Dk at 8 gigahertz." That's more design-related because you don't test it at 8 gigahertz. Typically speaking, they're more related to manufacturing or what I call acceptability.



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Shaughnessy: Kelly, on your side, you've been dealing with a lot of these manufacturing notes. Tell us about your engagement with manufacturing notes and some of the issues that you've seen.

Kelly Dack: It's a pleasure to speak with Dana. I think it's good to clarify that notes are meant to specify or define what a designer wants in a bare PCB. As we go through a list of notes, we need to be able to communicate and define



Kelly Dack

and specify the bare board in order to end up with what we want.

For instance, a board outline can be manufactured in several different ways. We don't necessarily need a manufacturing note to tell the board shop that the edges of the board shall be routed unless it really matters in the rest of the design or that the

board edges shall be V-scored. We do better by defining the board outline and tolerance, letting that stand as the specification, and allowing the manufacturer to deliver the specification.

Korf: I agree. As I tell people, "Tell me what you want, not how you want me to do it. I won't tell you how to design the board, and you don't tell me how to build a board." The most common problem I see in notes is that, a lot of times, the designer cut and paste from other boards, and they may not make sense. Or you have new designers who aren't familiar with the specs. My favorite one is, "This board shall meet IPC Class 3 requirements," yet the annular ring doesn't. You have to go back and say, "Your board doesn't meet Class 3, and I can't get there with this design. What do you want me to do?" You hear back, "Well, make it Class 2."

Dack: I can totally relate. Working for an EMS, I see a myriad of notes that just don't make

sense. Sometimes, we can tell that they've been cut and pasted, and the designer has no clue about what they are inflicting on the bare board manufacturer. I just had a scenario where a board requirement came in. The material was FR-4, and there were not too many notes. Our job as an EMS provider is to get this board quoted at several board shops with which we have relationships. We're going to get numbers based on what the bare board shop says they can do. Believe me, their job is to win the quote, and they're not going to do it by quoting the highest-rate materials or the highest Tg materials. They're going to presume that they can use the lowest-rated materials.

We had a board that was quoted at 130 Tg material, but it needed to be changed to 170 Tg because of all the different thermal excursions that it would be going through in assembly. A high-temp material would have been a better choice, but because it wasn't specified, we ended up wasting a lot of people's time. Actually, the designer, through his lack of specification skills, ended up wasting a lot of people's time.

Korf: Back when high-end boards were U.S.-centric or European-centric, the fabricator wasn't as cost-sensitive. The fabricator would pick a material beyond maybe what the designer wanted because we knew better. It would probably last better or perform better. Then when we started shifting to Asia, they did exactly what you said. You said FR-4, they quoted standard Tg FR-4, and they always came in cheaper. We had to kind of retrain everyone to say, "Give them what they say, because that's the world now. Don't give them more than they're willing to pay for."

We had a great example in China a couple of years ago. A company came in and just said FR-4, so we put in a halogen-free mid-Tg material, and we built the prototypes in a couple of cycles. It went just fine. We got it quoted. Correction quotes went out, and everyone was happy. Then, the final drawing came in, and it said, "We want high-Tg FR-4." "But that's not what you said on the prior two revisions." Everyone freaked out. "It's the fabricator's fault."

What do you mean it's our fault? The person said FR-4, so we picked one. Actually, we probably picked not what we thought the design actually wanted, but what the cheapest one was. As we always say, it's always the fabricator's fault. Front-end people know that board shops and front-end engineers are always at fault for everything because they give us the most money and computers and higher-paid people, so we should never make mistakes. That's kind of normal.

Another famous one we see all the time is when you get a drawing that says, "ITAR restricted." I'm looking at it in Asia. I'm going, "This says ITAR. We're not supposed to see it." "Well, you're American." No, I can't see this in China. It's supposed to stay in the U.S."

We go back to the customer, who says, "That's our commercial division." Well, your note says it's ITAR. We can't quote it. They respond, "It's okay." No, it's not okay. I can't take a verbal waiver for this. People, particularly purchasing agents, don't read the notes, number one. They don't necessarily understand what it means. I've seen that multiple times.

Dack: Usually, board manufacturers will not complain or raise questions until after winning the quote. That makes specification even more important. The less you specify, the more the supplier can agree that they can deliver until the time that they win the quote. That is when we typically see the questions roll out, and it's just a show-stopper.

Barry Matties: Do you see that prices tend to be revised at that point as well? Do you ever see an increase?

Dack: Yes. This causes a tremendous problem. For instance, in our EMS world, we negotiate with our customers because we have to deliver a quotation for the work also. Our quotation is based on quotations from other suppliers. In the case of a bare board, our job is determining a price, and our costs rely heavily upon the quotations that we receive from our suppliers. If we don't get an accurate quote due

to lack of specification, then we have to subject the customer to a change in price after we have quoted the work. When prices change, it's never pretty.

Korf: I'll kind of agree and disagree with Kelly on one point. I agree that a lot of quotes come in, and you don't do DFM reviews during a quote typically because it takes a lot of work, but at most front-ends in large volume shops, 25-50% or more of their capacity is taken on pre-design DFMs. You get a design that comes in, and prior to quoting, the sales folks say, "We need a full DFM." You do a full DFM, all the TQs, stackups, and everything and send it back. It's actually quite a significant portion of the capacity. You would always try to argue, "We shouldn't be doing DFMs for people unless we have a high probability we're going to get the order." I used to actually track that. I used to track DFMs per part number per customer to feed back to sales and say, "I had one customer one time. We did 11 DFMs for five part numbers and never got an order, and somebody else got a really nice design package to build."



Dana Korf

Dack: To add insult to injury in this industry, unless the customer has requested the DFM analysis, which good customers do, customers that have a lack of specification don't want to hear about all the problems with their product. Could it be that suppliers are concerned about losing the quote and therefore keep questions close to their chest until winning the quote?

Korf: There are two answers to that. At some OEMs, the designers want to know all of the issues, and they get mad if you don't ask all the questions. There are other ones that never want to hear a question. It's part of the psychology of front-end engineering. You categor-

size people that way. “These people want to hear, but these people don’t.” The ones that don’t want to hear issues, you just give them the ones that make it totally unmanufacturable. Just say, “We have to stop.” I call it “law of physics”-type questions. It can’t be built unless we resolve the issues. Definitely, in a competitive bidding situation, there are a lot of EMS providers and a lot of people that are buying the boards for assembly that would just be price-based. They don’t care. It’s just price. If you’re the cheapest, you get the order.

Companies will learn those customers, too, and tailor their responses to them. There may be a partial high-level DFM being done in the background. We look for any major issues that may cause a yield hit, a rework hit, or a major cost hit. Sometimes, it’s done in the quoting group, sometimes by another group.

Dack: I think it’s very valuable to establish the orientation of the documentation. We start every note set with the primary side of the board shown, and we follow the IPC standard declaration of a primary side and a secondary side. The interpretation of that is that the primary side is the side that the designer has designated. It got confusing. We all know the story of how the solder side of the board became the solder side, and the component side became the component side. With complex boards now, it’s not as clear. Where we have gone is that the primary side is the side that the designer has designated as such.

Korf: That note’s real critical for assembly. For fab, we’re going to look at a file that says the layer names. What’s the file layer name, and how do I match that to the board? The primary side, is it called layer 1? Is it called top? Is it

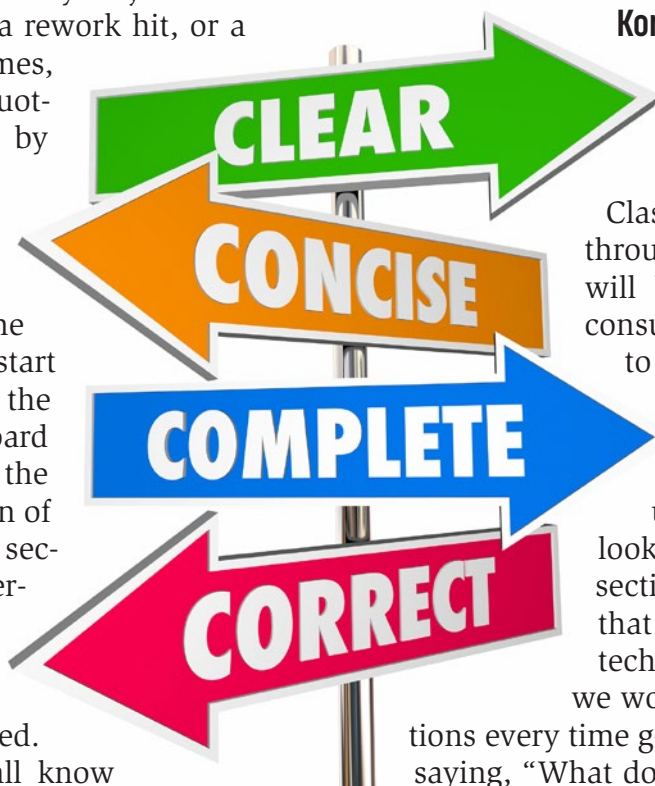
called Jim? I don’t really care what it’s called. Just tell me what it is. Most fabricators will align boards the way they want to build them. They might not label them the same way as the designer, just to have some standardization in the factory. From a conversation standpoint, it’s always good for assembly. For fab, it’s not too useful. We just care about matching the data layer names to the actual data provided.

Dack: In the context of the design, if you’re going to specify Class 2, you’d better be designing Class 2 and not a different class for manufacturing and inspection purposes. What do you think?

Korf: That’s critical because that guides a lot of default criteria, the IPC class in general. A lot of people will say, “I want Class 2, except for my plated through-holes. My annular ring will be Class 3.” One of the consulting projects I’ve set up to solve someday is this: Every IPC spec has this category called AABUS, or “as agreed between user and supplier.” If you look at IPC-6012E, there are 38 sections and tables that have that as a criteria. If everyone technically followed that spec, we would have to have 38 ques-

tions every time going back to the customer, saying, “What do you want to do?” No one does that in reality. That’s one of the conflicts in the specs versus reality. No one is going to ask 38 questions every single time just because of the IPC spec, and the committee couldn’t agree on an answer. Or, as I call it, some of these AABUS categories should be a tutorial. You should worry about this. I agree that the IPC class note and exceptions to it is critical.

Happy Holden: Dana’s hitting all of the key points. The big problem I always have is the



difference between a quick turn local PC shop and high-volume offshore company in terms of the difference of materials and the pain that it caused depending on how sensitive the board is. I don't have any notes of any particular references other than, eventually, you'll get around to hole plugging, which has always been a headache from a notes point of view. I always tell people, "Just steal the picture out of the IPC standard and paste that on the drawing so that we can see what it is. Don't make up new words." Especially if you're going to go to Asia, I remind people that English is usually not their native language. A lot of these made-up words that we use to describe PCBs don't translate well into Chinese or other languages. It's a source of misunderstanding and error.

Shaughnessy: What do you think is one of the biggest mistakes that designers make, and what advice would you give for correcting them?

Korf: From a notes standpoint, one of the biggest reasons I hear for a mistake is that they just cut and pasted from another design. They didn't really read them. They may not really understand the meaning of the notes that they're using. That's probably the number one reason I hear for errors. There's no designer out there that I know of who intentionally designs a bad board. It's just that they don't realize it. You see a lot of ODM designers who are designing a cellphone one day. The next day, they're designing a medical device. They just have no experience. They don't really understand what notes should be or shouldn't be on a drawing. That's probably my number one reason.

Holden: One of my biggest issues is that a lot of times in Europe and the U.S., for simplicity, you standardize on a standard panel size. But in Asia, because the material is so much of the cost, they're a lot more sophisticated on panel size. Designers, if they know they're going to go offshore, don't find out really what the panel size is and what the border requirements for a preferred vendor or something

like that are. You can easily, in choosing board sizes, screw up the cost because, with 1/4" less in some dimension, we could increase the panel array quantity, reducing the cost per board. Maybe Americans are willing to waste the laminate, but in Asia, they don't like to waste laminate.

Korf: That's very true. Also, we're still working in a 1980s Gerber-based world where we have just a plotter language telling you what line and circle to draw. I need a piece of paper to interpret these lines and circles. I'm very active in the IPC-2581 committee. If you look at having intelligent data where you can attribute everything, a lot of these notes actually disappear. Like materials, they disappear. You just include the material spec in your stackup data. You don't need a drawing. You don't need a note. There's a lot of notes you don't need telling you what to do because it's already in the data. That's part of the 10-year transition as we move away from Gerber-based data to intelligent data that we can start getting rid of some of these notes. A lot of times, these notes contradict with the picture on the drawing and/or the data. If it's included in the data from the CAD system, then we'll start to see the elimination of both the notes and some of the issues.

Holden: I can't figure out why Gerber still exists. Nothing else in electronics is 60 years old. If electronics are three years old, they're getting toward obsolescence, yet we're stuck.

Korf: ...on a plotter format from the 1960s. Exactly. One of the most common issues is that you get a board outline drawing on the fabrication print. You extract it from your data file, and they're different, or you get a netlist that doesn't match the data. I presented at IPC APEX EXPO a couple of years ago. I asked the audience, "When we ask the question, should we use the netlist extracted from the Gerber or the original netlist? What should we use?" Everyone responded, "Gerber," and then laughed. They all realized what a nonsensical answer it was.

Matties: Is there any sort of standard for creating fab notes, or is this really up to the designer to decide what you need to know?

Korf: A lot of board shops will give suggested standard notes to customers, but there are no standards in the industry that I'm aware of.

Holden: There will be with IPC-2581.

Korf: It will give you a way to transmit the data, not the actual note contents themselves.

Holden: Yes, but you have more descriptive descriptions. You also have a section of 2581 that includes notes.

Korf: Correct. You can embed it in the file.

Matties: But it's still discretionary as to what the exact notes are.

Holden: That's the whole thing about electronics and printed circuits: If you come up with a neat idea that nobody has ever thought of, and it involves PCB assembly, if you want the right product back, you'll have to describe it in the notes because it's not coming by any standard.

Matties: The designers realize that there are problems, and they're looking for answers. If you're looking for an answer, what is it, Dana?

Korf: I'm a simplistic person. My goal is to build whatever you send me without having to ask a question, and you get what you wanted. It sounds like a simple mission statement. The biggest issue is conflicts.

Matties: That puts the onus on the designer.

Korf: Yes. It puts it on the designer or whoever prepares the document package. Now that we have an EMS step in there, sometimes, it gets confused in there. They mix and match revisions together. I see that a lot, such as Rev B fab print with Rev C data. Someone will revise

a layer, so you'll have one layer of Rev D and everything else at Rev C, and it doesn't match all of a sudden. There are lots of reasons. As I tell the CAD system people, "None of your tools work." Talk to anyone in the world and say, "What percent of your data packages is coming clean that you don't have to clean up or have issues with?" Most people will say very few. It's a very small percentage.

Matties: If a designer is looking at the data set that they need, is the best course of action to first talk to the manufacturer?

Korf: From a design and capabilities standpoint, absolutely. The data required is the same for everybody. I doubt if there's any vendor-to-vendor or region-to-region difference there. It just needs to match. The problem is, a lot of times the vendor isn't selected until the design is done. The designer hands it off to an EMS company, which then visits 12 people. They select two, and it's too late.

Matties: Are fab notes generated during the design process or post-design?

Korf: Probably both.

Dack: From the standpoint of the designer, the designers don't know what they don't know. They need to know what they don't know. The only people that are going to enlighten them are the stakeholders that they're working with. In this case, if it's a bare board, they need to engage the fabrication stakeholder or supplier to discuss topics of capability because without marking that line in the sand, they are not implementing DFM.

Korf: As a fabricator doing pre-design DFMs, I was always happy to do that if they would do what we asked, or we compromised on what would work for the design. Unfortunately, there's a lot, especially large companies, that have in their process, "I have to have two DFMs before I can release to manufacturing." They get the first prototype and test it. Then, you get the second revision of the board, and

it includes all of the same issues they had the first time. Next, you get the production board. All the issues are still there.

Dack: They want to manufacture for their design. It goes contrary to everything that we've been pushing for the last few decades with regard to design for manufacturability—in other words, finding out what's available. This is not rocket science; these are standard, regular boards. There are proven capabilities out there that we need to design around if we expect that our board is going to go to market in the fastest time possible.

Korf: Also, some fabricators don't want to give out their rules because they think it's IP, and it really isn't. They're forcing bad designs to come in that they aren't capable of building because they refuse to tell them what their capability is. I put the fault on both hands there, not just always the designer.

Shaughnessy: If you have good communication between the designer and the fabricator, the designer gets to know your capabilities, and you know what to expect from the design team. It seems like that would be the key.

Korf: If the designer has five fabricators, all five

fabricators can agree on a common set. That's been done many times.

Dack: Yes. That gets back into the, "Well, the other people built it." That's problematic, too. It can go both ways. It was probably an onshore supplier for it to do anything because they're building three or four of them. When it turns into production, and they're building millions, things change a lot from a capability standpoint.

Korf: To wrap up on notes, when I was in Asia, my team would bring me a note and say, "What does this mean?" Think about it: You might have an engineer in France who speaks French and puts in a note in English, and I don't know if they've learned British English or other variations. It then goes to someone in China whose native language is not English. What English did they learn when they read the note? The problem with notes is that sometimes, it's not clear if you speak the native language what it is a person is asking. As Kelly just said, if you assume, you're going to assume wrong, and you're dead.

Shaughnessy: This has been great. Thanks for speaking with us.

Korf: Thank you, Andy. DESIGN007

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The Wavelength of Electromagnetic Energy

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

The speed of light is the one universal physical constant that we are yet to break. It is the limit of the velocity at which conventional matter and information can attain in our universe—without warping space-time, of course. At a lightning 299,792,458 m/s, it is the maximum speed at which massless particles (or waves) of light, electromagnetic energy, and gravitational waves travel in a vacuum. In this month's column, I will look at how to simply measure the speed of light and how the wavelength of electromagnetic energy relates to the multilayer PCB.

One morning recently, whilst eating my vegemite toast (as Australians do), I was reading my weekly *New Scientist Magazine* and came across an interesting article on how to measure the speed of light using a chocolate bar and a microwave oven. Here's how it works.

A microwave oven's magnetron (RF transmitter) oscillates at 2.45 GHz. Electromagnetic energy in this frequency range has an interesting property: It is absorbed by water, fats, and sugars. The microwaves, in the turned cavity, penetrate the food and excite the molecules heating the food throughout—provided the turntable is rotating. But for this exercise, the chocolate bar needs to be stationary, so remove the turntable.

Since the chocolate bar is not rotating, the microwaves are not evenly distributed throughout the bar, and regions of chocolate will begin to melt in the high-intensity areas. Chilling the bar first makes the molten areas more distinct. This will take approximately 50 seconds on high power. Take care not to exceed 60 seconds, or you may have a mess to clean (lick) up.

Electromagnetic energy travels in a wave through a vacuum or air at the speed of light. The distance between the peaks of the wave is the wavelength of the energy. As the wave travels, the peaks and troughs heat the chocolate. By measuring the distance between these hot spots, one can determine the half wavelength of the energy (Figure 1). You

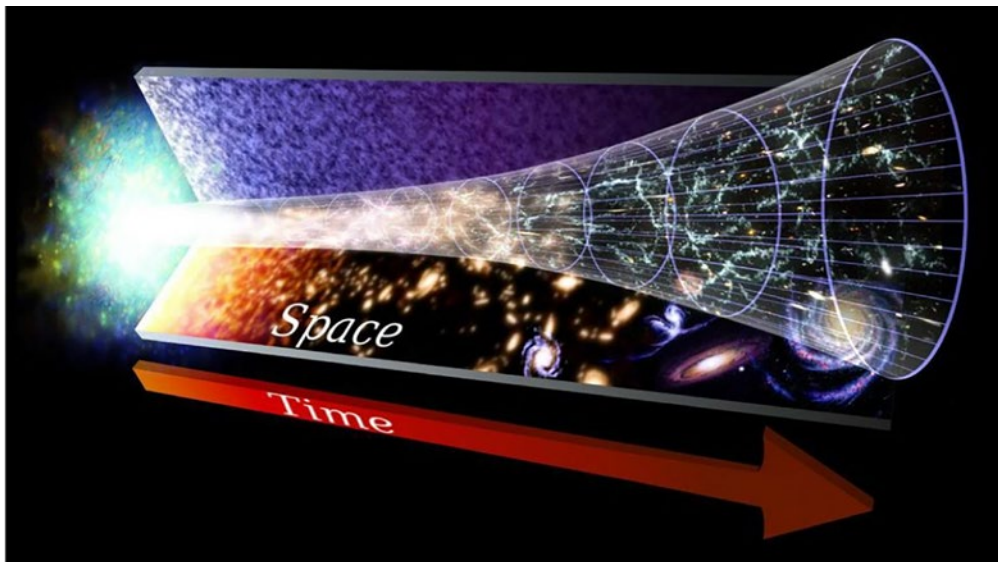


Figure 1: Half wavelength between hot spots. (Source: NASA Goddard Space Flight Center)

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should get about 60 mm between the melted globs. I got 58 mm after 45 seconds. However, there is plenty of leeway in the dubious accuracy of my plastic ruler and failing eyesight. Doubling this (120 mm) gives you the wavelength related to a frequency of 2.45 GHz. The following equation is used to calculate the velocity (v), where f is frequency and λ is the wavelength.

Equation 1:

$$v = f\lambda = 2.45\text{GHz} \times 0.12\text{m} = 294,000,000 \text{ m/s}$$

For an extremely rough measurement, this is very close to the actual velocity of light (299,792,458 m/s). Note that light will travel a little slower in the air than a perfect vacuum.

Now, let's look at how this relates to the speed of electromagnetic energy in multilayer PCBs. If you have a digital signal running at a clock rate of 2.45 GHz, then one would expect

the wavelength to be 120 mm. Wrong! Unfortunately, the relative permeability or dielectric constant (Dk) of the surrounding materials impacts the velocity of propagation at the speed of light (c).

Equation 2:

$$v = f\lambda = \frac{c}{\sqrt{Dk}}$$

A vacuum has a $Dk = 1$, air = 1.0006 and typical FR-4 = 4. Then, solve Equation 2 for the wavelength, including the Dk of the dielectric material:

Equation 3:

$$\lambda = \frac{c}{f \times \sqrt{Dk}} = \frac{299,792,458}{2.45\text{GHz} \times \sqrt{4}} = 61 \text{ mm}$$

Therefore, the FR-4 material in a stripline configuration slows the propagation speed and decreases the wavelength of the electromagnetic

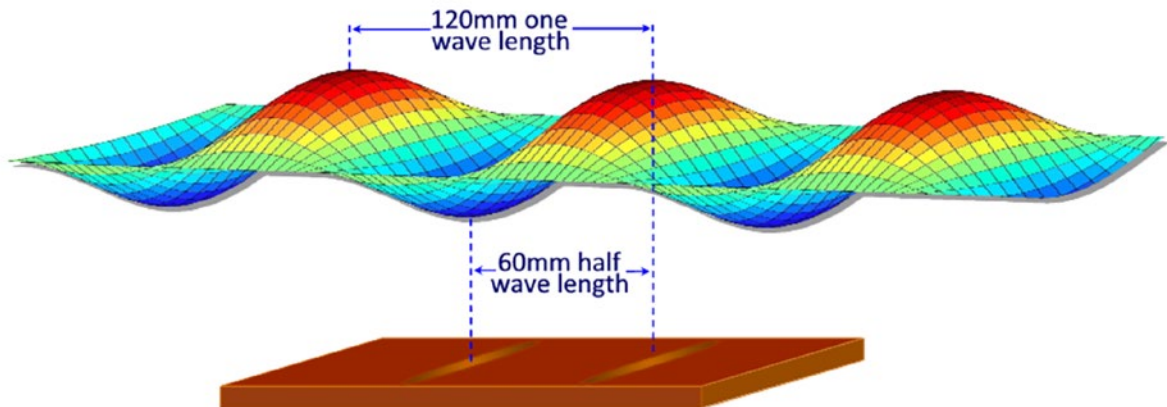


Figure 1: Half wavelength between hot spots.

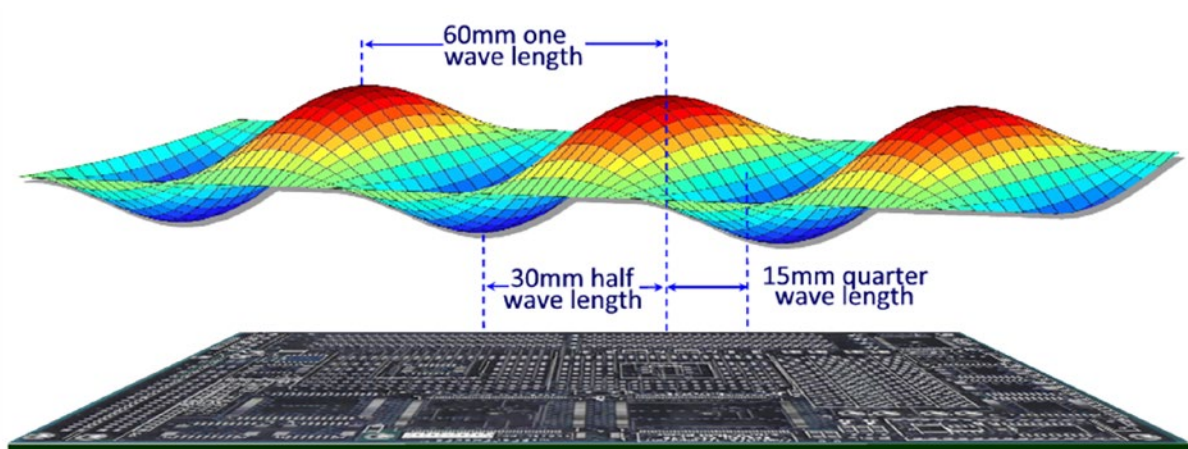


Figure 2: The wavelength of a 2.45-GHz signal on a PCB inner stripline layer.



Figure 3: Comparison of Dk per layer and relative velocity.

netic wave down by about half (Figure 2). But that all depends on the exact dielectric constant of the surrounding materials.

For the top layer 1, the electromagnetic energy travels in a combination of prepreg, solder mask, and air (Figure 3). The effective Dk will be around 2.68 with a propagation speed of 1.83×10^8 m/s. For layer 4, there is a combination of prepreg and core with an effective Dk of 4.03 and a speed of 1.49×10^8 m/s. This should be simulated by a field solver, as it depends on the combination of materials and their Dks, order, and thickness. From this, one can see that the propagation speed of the electromagnetic energy is always faster on the outer microstrip layers than the inner stripline layers.

At high frequencies, short traces (particularly stubs or unterminated traces) on a PCB can act as a monopole or loop antenna. Differential-mode radiation is the electromagnetic radiation caused by currents consisting of harmonic frequency components flowing in a loop in the PCB. The radiation is proportional to the current loop area and the square of the frequency of the signal. Common-mode radiation is the electromagnetic radiation caused by current flowing in an unterminated trace (or terminated with a high-input impedance device) and may require load terminating resistors to eliminate reflections. The radiation resembles that of a monopole antenna, and the magnitude is proportional to the current per line length and frequency.

Trace antennas form a monopole with a quarter wavelength ($\lambda/4$) at the resonant fre-

quency. Monopoles require a ground plane; this forms the other quarter wavelength to radiate efficiently, which is not desirable in this case. It functions as an open resonator, oscillating with standing waves along its length. The radiation pattern is practically omni-directional.

Unfortunately, the high-frequency components of the fundamental (lowest frequency in a complex wave) radiate more readily because their shorter wavelengths are comparable to trace lengths, which act as antennas. Consequently, although the amplitude of the harmonic frequency components decreases as the frequency increases, the radiated frequency varies depending on the characteristics of the antennas/traces.

At 2.45 GHz, an 18-mm trace on the outer, microstrip layers may radiate while on the inner stripline layers, 15 mm (600 mils) is sufficient. And as we increase the frequency to 10 GHz, the maximum length is just 3.75 mm (150 mils), which is incredibly short. Stripline traces are embedded between two planes, which dramatically reduces radiation with the exception of the fringing fields from the edge of the board. However, the outer microstrip layers will radiate; hence critical, high-speed traces should be avoided on these layers.

Since the wavelength of electromagnetic energy depends on the signal frequency and dielectric constant of the surrounding materials, a low Dk (circled in Figure 4) is preferred for high-speed design. Fortunately, low-loss materials generally have this characteristic.

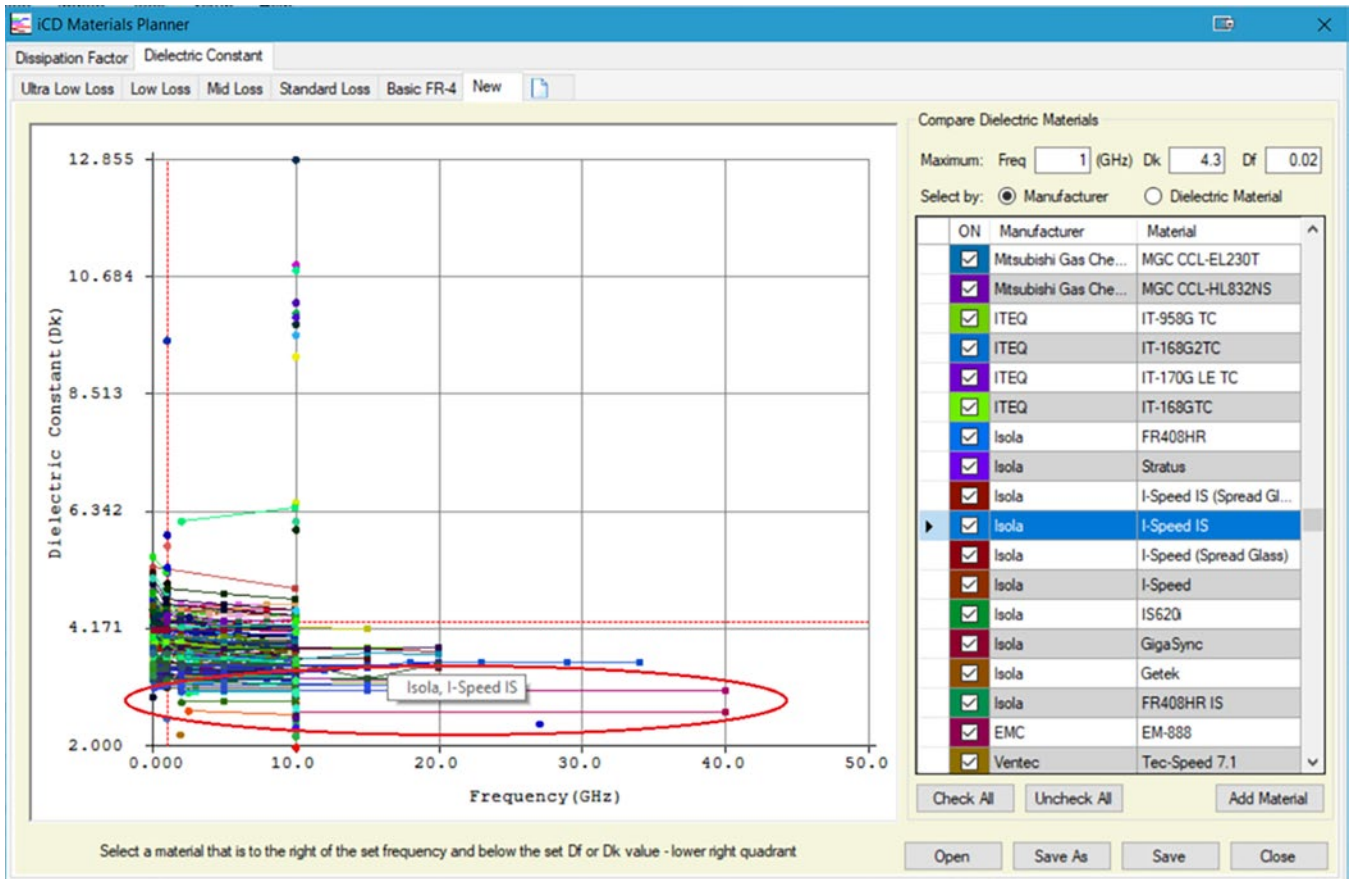


Figure 4: Plot of dielectric constants of high-speed materials (iCD Materials Planner).

Key Points

- Microwave energy is absorbed by water, fats, and sugars.
- Electromagnetic energy travels in a wave through a vacuum or air at the speed of light.
- The distance between the peaks and troughs of the energy is a half wavelength.
- The dielectric constant of the surrounding materials impacts the velocity of propagation of the signal.
- The FR-4 material in a stripline configuration slows the propagation speed and decreases the wavelength of the electromagnetic wave down by about half.
- In a microstrip (outer layer), the electromagnetic energy travels in a combination of prepreg, solder mask, and air, which reduces the effective Dk.
- In a stripline, there is a combination of prepreg and core.
- The propagation speed of the electromagnetic energy is always faster on the outer microstrip layers than the inner stripline layers.
- At high frequencies, short traces (particularly stubs or unterminated traces) on a PCB can act as a monopole or loop antenna.
- Trace antennas form a monopole with a quarter wavelength ($\lambda/4$) at the resonant frequency.
- High-frequency components of the fundamental radiate more readily because their shorter wavelengths are comparable to trace lengths.
- Outer microstrip layers will radiate; hence critical, high-speed traces should be avoided on these layers.
- A low-Dk material is preferred for high-speed designs.

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Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at icd.com.au. To read past columns or contact Olney, [click here](#).

Solaris Acquires Jetbrain to Aid in Using Robots to Fight COVID

Solaris Disinfection Inc., a leader in IoT-connected service robotics, whose flagship Lytbot automated disinfection system is currently being used by hospitals across North America in the battle against COVID-19, announces the acquisition of Jetbrain Robotics, an innovator in hospital logistics and patient experience using autonomous mobile robotics (AMR). Invested in and supported by world-class investors Brinc & Artesian Venture Partners (AVP), Jetbrain's technology improves operational workflows in complex healthcare environments, providing quantifiable efficiencies and patient experience improvements.

Since 2017, Solaris has conducted research on the effectiveness of its pulsed UV technology against communicable human respiratory viruses like novel coronaviruses (COVID-19). "COVID has accelerated robotics deployment by five years," said Adam Steinhoff, Co-Founder, and CEO, Solaris. "In continuing our mission to improve the safety of patients and support healthcare workers, we identified Jetbrain's technology as an opportunity to improve upon our core products while providing safety, accountability and compliance-based platform technologies that help our customers effectively utilize resources and improve workflows."

Adds Val Ramanand, co-founder and executive chairman, Solaris, "At Solaris we are very proud of the growing impact we make on a daily basis in the healthcare industry by delivering practical and approachable products, designed to improve patient outcomes and healthcare operations. The acquisition of Jetbrain supports our continued mission

to improve care, keep spaces safe, and ultimately help save lives in healthcare facilities globally."

Jetbrain products include delivery robots that feature a secure and traceable chain of custody for medicines and blood products, as well as patient experience robots that provide anything from clinical support to wayfinding help. The addition of Jetbrain's team enhances Solaris's expertise in healthcare robotics while extending its offering from whole room disinfection to automated delivery, logistics, and ultimately patient experience, thus delivering industry's first ecosystem approach to healthcare robotics.

(Source: PR Newswire)



Mark Thompson's Most Wanted: Accurate and Complete Fab Notes



Feature Interview by the I-Connect007 Editorial Team

Editor's note: When this interview was conducted, Mark Thompson, CID+, was in engineering support at Prototron Circuits. Mark is now a senior PCB technologist with Monsoon Solutions, a design and engineering bureau in Bellevue, Washington.

In his position in the CAM department at Prototron Circuits, Mark Thompson has seen his fair share of puzzling data and documentation. He discusses some of the difficulties he's encountered with designers' fab notes and provides designers with a number of points to consider the next time they send out a design.

Andy Shaughnessy: Mark, give us a taste of some of the more common problems you see with customers' fab notes.

Mark Thompson: From where I sit as an engineer in a fabrication environment, the biggest thing I see is designers who produce boiler-plate notes that they get from their CAD system. A lot of them have templates

that are already embedded in their system. They can just call it up and say, "Notes 1-14 are golden. We're going to put those on." Ultimately, if it doesn't have anything to do with the job, get rid of it because it's going to cause additional grief and phone calls from the fabricator.

There is some information that your fab notes should absolutely have, including standards, a board class, and material type. Flatness is another; if flatness is critical, put in tolerance for flatness. If it's a board that is massively dielectrically challenged, with very thin dielectrics on one side and very thick dielectrics on the opposing side, whether you add additional metal on the outside or one is a solid plane and one is a full signal, it can still end up with some modicum of warpage. Warpage being an issue, flatness is a callout that you're going to want to have in your drawing.

We also need hole tolerances, dielectric thicknesses, shape tolerances, and the overall board dimensions (is it 4" x 5"?), as well as surface finishes, immersion gold, immersion silver, deep gold, or HASL. All of the surface finishes have a tolerance and a thickness based on IPC standards that need to be adhered to. That's



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Mark Thompson

a number that you're going to want to have. Additionally, testing—not just electrical—but HIPOT, HAST, and all the other testing variables should be done. If you have a requirement for HAST testing, it's going to have to be on your drawing.

We also need to know the mask, ID color, and type. We have various dielectrics for our colors of masks. Why is that? We can't feasibly set up every possible color with the automatic flood coater. Some of them have to be hand-screened by an operator, and that person doesn't generate the pressure that the machine has. Ultimately, we may call blue or purple or red something closer to two mils of dielectric thickness over the top of the glass and one mil over the top of the metal. Does that make a huge difference on an eight and eight? Not really, but does it make a huge difference on sub-four and four? Absolutely. When you get down to the real small geometries, that additional mil of dielectric thickness and dielectric constant change for the solder mask makes a huge difference for controlled impedance.

Additionally, there are things like allowable X-outs and impedances. If you have any impedances, either call it out on a README or directly on your drawing notes. Typically,

it will say something like, "All five-mil lines on layers one, three, six, and eight to be 50 ohms." Now, one thing that I don't advise is chasing the impedances. We have a couple of our customers where if I send calculations, it will go back to the customer, and they will make those modifications down to the gnat's butt. They'll say, "If I say I need to change your 4-mil trace to a 4.25, I'm going to send data at 4.25." That doesn't mean that other fabricators would need that same change. If it's within 10%, don't mess with it at all. Remember that being the goal. As a designer, engineer, or layout person, they're just trying to stay within 10%. They give it to a fabricator, and we take it the next 10 miles.

Then, there are cut-outs and radiuses. If you have a cut-out that is drawn or depicted as 90-degree intersections, we're going to need to know what the minimum radius is. Is it 0.032", 0.062", 0.093"? What's the minimum radius to be able to fit that device inside that cut-out? Those are just some of those kinds of things that I'm talking about. One thing that can eliminate the confusion between fabricators and people that are generating fab notes is consulting your fabricator. Call us directly and say, "I'm working on some fab notes, and my board is heat-sensitive. It is controlled impedance, and I need this. I have a 0.8-millimeter ball grid array, and I need to ingress and egress out of that very tight pitch BGA."

Now, at that stage, I have to ask, "Are you going to have long runs of very small lines and spaces for differential pairs that are ingressing and egressing out of that BGA? Or are you only necking down to a very small distance from a much larger differential size outside the BGA?" And the reason I say that is because I have a number of customers that will ask me, "What do I do to control the differential pairs that are inside that BGA?" If they're less than an inch and most components are an inch, two inches, in maximum size, it means nothing. I'd say, "Control those larger differential pairs that are running 12 inches on the outside of the BGA and not those that are inside the BGA." Take the hit of having it going inside that BGA.

Shaughnessy: Are the fab notes incorrect, or are they primarily just incomplete? What is typically the biggest problem?

Thompson: Gosh, we see everything. We have over 5,000 customers. We see inaccurate notes and notes that are not relevant to the job and therefore require a phone call. “It looks like you’re calling out blind vias on this job, and there are no second drill files associated with a layer 1 to 2.” If they don’t exist, don’t call them out. Simple as that.

Shaughnessy: It just amazes me because many of these designers have been doing this for 40 years. But a lot of times, fabricators just accept the data because you want the job, and you fix the problems.

Thompson: Even the new guard, the new kids that are coming into PCB design, just don’t know what they don’t know. I try to assist them in any way I can.

Shaughnessy: But it sounds like there are often no consequences to submitting bad fab notes.

Thompson: Other than the hit on time. Because either a salesperson or I have to call the customer and clarify those notes. That takes time, and we sell time.

Shaughnessy: You said you have your regular customers, and that you have them trained. What are some of the things that a trained customer will provide you?

Thompson: For example, nesting, which is how much prepreg is going to get sucked up based on the copper weight that is an interface on an inner layer. If it’s half-ounce, it’s going to have less of an impact. If it’s two-ounce, three-ounce, or four-ounce copper, it’s going to be a huge impact. It also depends on the configuration of the layer, whether it’s a full signal, a split plane, or a plane. If it’s a plane, it’s going to have the least impact. If it’s going to be a split plane, it’s going to have more impact. If it’s a signal, if it’s a pure signal, two

or three-ounce copper, and you’re not calculating exactly how much break you’re going to lose off that dielectric value, your impedances could be way off.

Shaughnessy: Happy, do you have anything to add?

Happy Holden: I spent my first 30 years not allowed to use IPC specs. Our many packaging specs were far more detailed than IPC, and they were written around our fabrication. Everything was being built in Asia—not in China, but in Asia, where the engineers were not native English speakers. I cleaned up a lot of their stuff with pictures and diagrams because using words constantly got us into trouble in terms of different translations. Each engineer might translate it differently.

Thompson: Exactly. And that brings up a really good point about the dielectric constant. I frequently get phone calls, where people will say, “What’s the Dk of 370HR?” And I’ll say, “What prep ply? What dielectric? What speed?” There are a number of different questions I’m going to have to ask to be able to get to where they want.

Holden: Because all these things are built out of different cores with different weaves of glass, which all have a different glass-to-resin ratio, and that’s not even counting what frequency you’re operating in.

Thompson: It makes a big difference between 500 megahertz and 120 GHz. With 120 GHz, that Dk goes way down.

Holden: I always start with material because that can get you in trouble. And if an RF amplifier is not working on a cellular tower in Louisiana in the middle of the summer, they blame the fabricator. Did you happen to understand that this material that you selected, when it’s humid and hot, the loss tangent goes completely away, and your signals go away too? It has nothing to do with the board. It’s the fact that you didn’t understand enough about

the material you were selecting before you did it. Or you didn't bother to test the extremes in your simulation and things like that, which I've always faulted the EDA tools.

EDA tools let us put in a dielectric constant, and then those same EDA tools will come up with a thermal analyzer to ensure the difference in temperature on the board. And yet the impedance calculator and field software they have only allows one dielectric constant and no allow-ability to put in a slope between the temperatures that you just told me the boards are going to see anyway. That dielectric constant dissipation factor's not going to be the same at those different temperatures, as well as frequencies. Yes, we understand temperature gradience, but somehow, nobody's ever accepted the fact that there is an electrical performance gradient.

They consider materials to be constants or absolutely flat lines; it's not going to change temperatures, and it's not going to change the frequency or anything else. And they do all of their signal integrity and impedance analysis based on this assumption about material. And with FR-4, that couldn't be further from the truth. You can get some really expensive material that's relatively flat, but it's really expensive. I keep asking EDA people that question, and they just shake their heads and say, "Nobody's asked for it."

Thompson: Happy brings up another good point there. We have two facilities: Redmond, Washington, and Tucson, Arizona. And you can imagine that Washington is moisture-laden. It's rainy most of the time and very cool, which is vastly different from Tucson, where it is extremely hot and dry. The press parameters and temperatures are vastly different between our two facilities. Therefore, the effective dielectric constants of the materials we use

vary. And that's all over the map. Recently, I've been gearing over to helping with Tucson more. I use Tucson's effective dielectric constants on their materials and their dielectric press values, which are different than what we use here in Redmond.

Barry Matties: Pretty much every job that comes in has data that's inaccurate or missing.

Thompson: Absolutely. Even having gone through sending a customer effective dielectric constants and calculations and dielectric builds, it does not preclude the customer from

changing things and submitting data that has vastly changed. They may say, "Five mil lines for 50 ohms." We get the data, and now they're eight mil lines. And the dielectrics are vastly different. Not only does that happen, but we also get people asking for different colors. Originally, it was calculated as green, but now it's going to be calculated as black—or worse yet, white.

In fact, all of the material colors—from green to blue, red, purple, and black—are all an approximation of 3.9 at 1 GHz. The white, for whatever reason, is 6.3. It's virtually double the dielectric constant. And why is that? Years ago, when people were doing more whiteboards for RF type considerations, they had problems where they were covering whatever the substrate was, or the surface finish was.

Matties: When you get the fab note, though, part of the conversation we've had with you and others is there's no incentive for them to send you a package that's 100% accurate or complete because the fabricators will do the work. And if you don't, the customer will just go and find another fabricator that will.



Thompson: But do you really want a fabricator to tweak your stuff? That's really the question you have to ask yourself. Do you really want the fabricator to tweak with your stuff to the point where they're making a two- or three-mil change of their signal to be able to accommodate the impedance?

Matties: You could say no, but apparently they don't mind if what we're hearing is accurate. How do we get designers to do it right the first time?

Thompson: More training, I'd say.

Matties: Part of it is more training, but is the information available that they need to provide the fab notes that you need, or how do they go about getting that?

Thompson: Most of them use templates that are boiler notes that they have straight from their CAD system. Altium, for instance, has a template that has boiler notes that they can go in and they can massage, if you will, to fit the needs of their particular board.

Matties: Is it board-specific, or is it fabricator-specific too?

Thompson: It's board-specific—not fabricator-specific. Fabricators are vastly different. Even between our two facilities, I just made the point about temperature and humidity driving a big change between our facilities.

Shaughnessy: But designers must be aware of the difference in humidity in Seattle vs. Tucson, right? It seems like this goes back to our discussion about whether designers need to be experts at manufacturing. Nobody sets out to design a board that isn't manufacturable. These



people have been doing it for 35–40 years, but they're still going around in circles with data.

Thompson: When they do a whiteboard process and go through an engineering review, and they say to themselves, "We're going to have to drive this down to six-mil vias." Now, sending it to us with a six-mil via, if they want it epoxy-filled, we're going to have to

increase that between 0.008" and 0.20." That's the sweet spot for us for epoxy fill. How do we get there? All of what we've been talking about is only relative to signal integrity. What about the things that they are grossly neglecting, such as missing drill files, IPC netlists, and layers? We'll have a 10-layer board, and we'll just get outer layers. Where are the inner layers?

Shaughnessy: Right. But if they're using an EDA tool, doesn't the EDA tool sort of say, "You're forgetting this extra layer?" It seems like there would be something.

Thompson: You mean a DFM tool? Frequently, they get in such a hurry that they negate that process. It's sort of like saying, "We're going to send the space shuttle up, and we're going to forget about that particular process. We're not going to go through those 30 days of that particular thing for flight. We're just going to go ahead and push it and make it work," and that's when you end up having space shuttles blowing up.

Matties: Oftentimes, you invest six or seven hours, in some cases, just preparing to give them a quote, and you may not get the job.

Thompson: Sometimes, it's way more than that. At times, I'll have a series of 28 emails, and we won't get the job.



Matties: Do you consider that a marketing or cost-of-sales expense on your P&L? Is it attributed to your sales costs, or do you attribute it to engineering?

Thompson: It's attributed to engineering.

Matties: It seems to me that it should be attributed to cost-of-sales because that's all pre-sale. You may be an engineer, but you're in the selling process when you're doing that. And if you're in the selling process, maybe you should get a sales commission.

Thompson: Our sales manager has always said that I'm one of his best salespeople, although I'm not an official salesperson.

Holden: It's too bad that most fabricators can't get away with charging non-referring engineering (NRE).

Matties: We've framed this conversation around fab notes, but there are also the fab notes for assemblers that we haven't even really talked about. This is just on the bare board side. And if it's this bad on bare boards, it has to be kind of rough for the assemblers too.

Thompson: Oh, gosh, yes. We have assemblers we'll send data check logs, and we'll have no less than five or six reCAMs based on small nuances that they want to make. They'll say, "Can you move the fiducials 0.5 mils in

this direction? Can you make the rails this size? Can you change this to a score tab instead of a breakaway tab?" All these different things that should have been negotiated from the beginning and came in through sales as a complete package with an assembly drawing or a sub-

panel drawing. Some of them refuse to produce sub-panel drawings for that very reason; they reserve the right to be able to come back and say, "Our nebulizer bit needs at least two inches before I can start to pinch these tabs off."

Over the years, we've understood those requirements, and we put together what's called a CSR database—or customer special requirements database—that has all the hot buttons for all 5,000 customers of ours. If they say they need a specific shipping method, if they have a specific assembly method, they have a specific panelization method, it is understood. And all of the departments are required to look at their section in the CSR database and to be able to conform to that.

Shaughnessy: Is there a standard for fab notes? That's one of the things we heard from previous conversations is that there really is no standard. Designers create the fab drawings the way they want to do them.

Thompson: Ultimately, I gave one customer 10 different scenarios of how to panelize things—nesting, 180-degree rotations, various breakaway tab strategies, the size of perforations and tabs along with the size and location of score lines. Because some people want the scoreline inboard, and some people want them outboard. Having them outboard means that they have nubs that they're going to have to trim off after assembly, and a lot of folks don't want to have to do that either. It becomes quite cumbersome.

Shaughnessy: Do you all advertise your capabilities? Because that's one of the things we've heard: Some board shops don't want to put out their capabilities because they're afraid it's IP that's going to help their competitors.

Thompson: We absolutely do. We have a capabilities matrix, and we talk about all of the things that we would need to build a circuit board.

Matties: From what we hear, the fab notes are a problem, and there's no good solution. Is there a lack of incentive since you fix all their mistakes anyway?



Thompson: It really comes down to time and training working with a customer. I've worked with some customers for over 23 years, and some of those customers will send us precisely what we need every time. Some of them that are relatively new will send us the wrong data almost every time.

Matties: What is the benefit of sending data correct the first time?

Thompson: We sell time.

Matties: But there's more than just time, right? If you were to make a pitch to a designer on fab notes and why they should provide 100% accurate on-time to you, what would that sales pitch be?

Thompson: It could be a number of different things, such as time to market, for instance. If you work a new project and need time to market, you must ensure that those fab notes are accurate because if they're not, you're going to get boards that aren't going to perform for you.

Shaughnessy: What would you recommend to somebody who's a brand-new designer as far as creating fab notes?

Thompson: I've said this before, but consult your chosen fabricator and ask them to assist you in the generation of the fab notes. Now, having said that, only the customer ultimately knows what their performance characteristics need to be for that particular board. There are many hidden things that the customer may not tell us, such as heat considerations. Signal integrity is just one small part of it. And maintaining controlled impedance is easy. Fabricators can do that day-in, day-out. But where it becomes difficult is those things that they don't tell us that they need on their boards that they will not divulge due to NDAs or other reasons.

Matties: It's a big topic with a lot of room for improvement.

Thompson: Exactly.

Matties: Thanks so much for your time, Mark. We appreciate it.

Thompson: Thank you. **DESIGN007**

To read past columns or contact Thompson, [click here](#). Thompson is also the author of *The Printed Circuit Designer's Guide to... Producing the Perfect Data Package*. Visit [I-007eBooks.com](#) to download this book and other free, educational titles.

Be Aware of Default Values in Circuit Simulators

Quiet Power

by Istvan Novak, SAMTEC

Simulators are very convenient for getting quick answers without lengthy, expensive, and time-consuming measurements. Simulators range from simple spreadsheet-based illustration tools ^[1] to very sophisticated 3D field solvers ^[2]. Somewhere in the middle, we have the generic circuit simulators—the most well-known among them being SPICE. Berkeley SPICE has been the grand-daddy of all SPICE tools ^[3], and these days, there are many professional SPICE variants available. These tools have been around for a long time, and we usually take the validity of their output for granted. While the tools may be bug-free, no tool can give us perfect answers for just any arbitrary numerical input; sometimes, we can be surprised if we forget about the numerical limits and the limitations imposed by internal default values.

As an example, I will show a few simulation results on a simple ladder-like power distribution network, all done with the free LTspice simulator ^[4] from Linear Technologies, now part of Analog Devices.

Figure 1 shows the schematic diagram of a simplified ladder model of a point-of-load power distribution network (PDN). The PDN is represented by four cascaded blocks. On the left is an ideal voltage source with series resistance and inductance modeling the DC source. To its right is a PI model of the PCB with plane resistance and inductance, as well as bulk and ceramic capacitors.

The next block describes the package with its series resistance, inductance, and capacitance. The 10- μ F capacitance value suggests that this is not only the static capacitance of the package planes, but it also represents package capacitors. The last block on the right describes the die with a series RL term, a parallel capacitance, and a parallel load resistance, which is determined by the nominal voltage and the average power consumption.

Outside of these blocks is a 1A AC current source injecting test current into the silicon node. Since all elements are linear and time-invariant models, the actual current value does not matter, but the 1A value is convenient

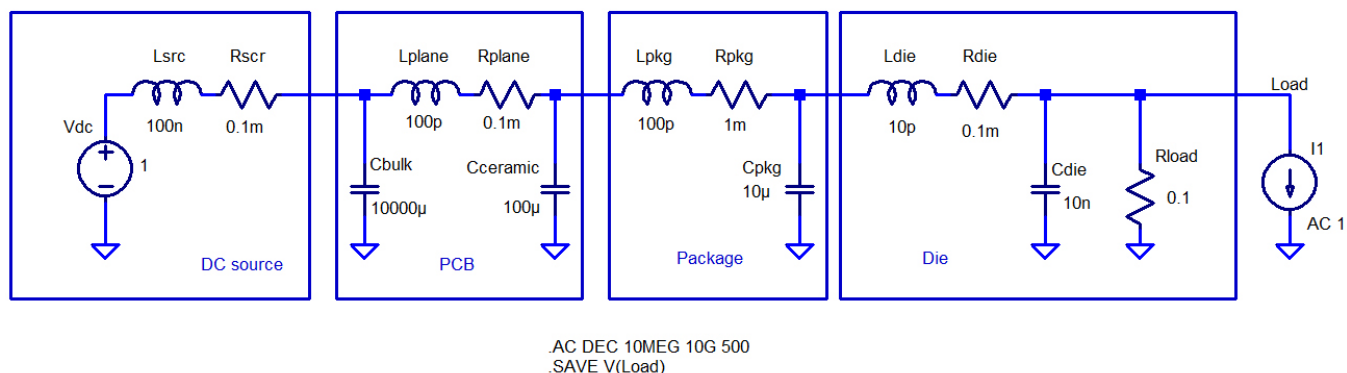


Figure 1: LTspice schematics of a simple PDN.

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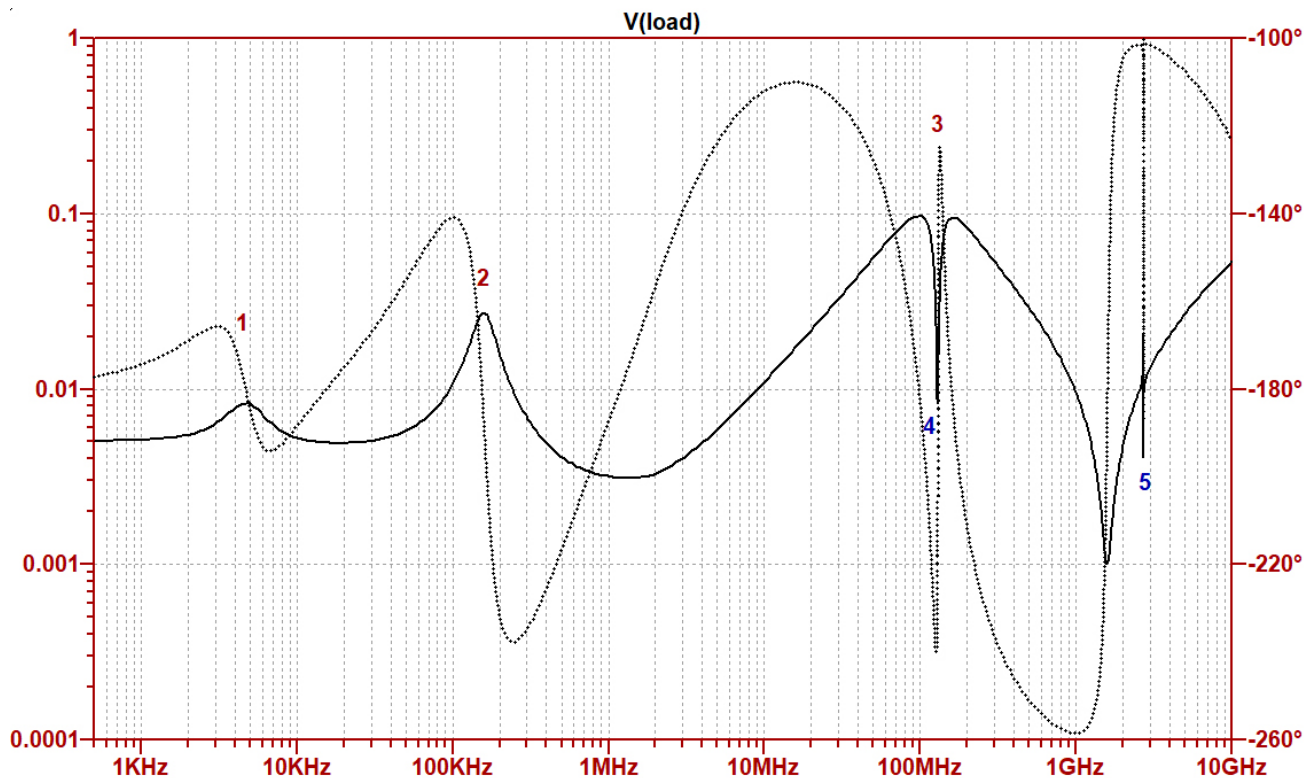


Figure 2: Impedance magnitude and phase of the simple PDN shown in Figure 1.

because the simulated $V(\text{load})$ output voltage directly gives us impedance without the need for further scaling.

Figure 2 shows the result. The heavier line is the impedance magnitude with its scale on the left, the phase is the thin line with its scale on the right. We see four resonance peaks and one sharp dip on the plot. Peaks 1, 2, and 3 come from the antiresonances of neighboring capacitor banks. For instance, the first peak is formed by L_{src} and C_{bulk} , and the LC parallel resonance of the 100-nH and 10000- μF values produce the 5-kHz resonance peak. To find the second peak, which comes from the series inductance of the C_{bulk} capacitor and the capacitance of C_{ceramic} , we need to know the assumed inductance of C_{bulk} .

You can notice that there are no series resistance and inductance symbols in series to the capacitors, so does it mean the simulation assumes zero values for those parasitics? In this regard, LTspice is unique among the SPICE circuit simulators. We can specify the usual simple parasitics without adding the corresponding schematic elements.

The equivalent circuit, as defined in LT Wiki [5], is shown in Figure 3. We can specify not only the equivalent series resistance and inductance but also two parallel loss elements and a body capacitance. These parameters will be frequency-independent entries. But how do we enter these parameters if we don't want to type up the SPICE deck manually?

LTspice makes it easy, offering multiple options. Figure 4 on the left shows what happens if we move the cursor over a capacitor in the schematic diagram and right-click. A window pops up where we can manually enter various attributes. On the right, you see the window which pops up when you hold the control key while you right-click.

The two windows offer somewhat different choices. On the left—in addition to the equivalent series resistance, inductance, and body capacitance—we have only one parallel resistance entry. On the right, we can enter every parameter listed in Figure 3, including the initial condition, temperature, and the multiplier (m or x), which is a convenient way to simplify the schematics if we have a number of iden-

C. Capacitor

Symbol names: CAP, POLCAP

Syntax: Cnnn n1 n2 <capacitance> [ic=<value>]
+ [Rser=<value>] [Lser=<value>] [Rpar=<value>]
+ [Cpar=<value>] [m=<value>]
+ [RLshunt=<value>] [temp=<value>]

It is possible to specify an equivalent series resistance, series inductance, parallel resistance and parallel shut capacitance. The equivalent circuit is given below:

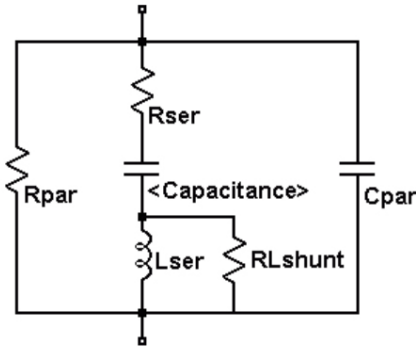


Figure 3: Screenshot explaining the capacitor equivalent circuit in LTspice.

tical capacitors connected in parallel. We can also hide parameters or make them visible on the schematic using the checkmark in the last column.

For the schematics shown, I turned on the feature only for the capacitance value; otherwise, the view would become very crowded. Notice that in Figure 4, I show the actual parasitic values that were used to generate Figure 2.

	Cbulk	Cceramic	Cpkg	Cdie
C [F]	10000u	100u	10u	10n
ESR [Ohm]	1m	0.5m	10m	1m
ESL [H]	10n	100p	1n	1p

Table 1: Parasitic values of capacitors that were used to generate Figure 2.

Now, we see that the series inductance of the bulk capacitor is 10 nH, and this creates the anti-resonance with the 100-μF ceramic capacitor. From these two values, we get a 150-kHz antiresonance frequency, and that is exactly where Peak 2 is. Peak 3 is at 150 MHz, and it appears to be split by the sharp and deep Notch 4. Table 1 summarizes the capacitor-parasitic values for all four capacitors.

We may wonder if the values in Table 1 represent reality because ESR and ESL for the ceramic capacitor appear to be unrealistically low. Yes, it would be unrealistic to expect these values from a single capacitor, but if we imagine that these values represent ten pieces of 10-μF ceramic capacitor with 5-mOhm ESR and 1-nH ESL in each, then it looks reasonable.

If we move on to look at the resonance at Peak 3, we realize that it is formed by the 10-nF Cdie capacitance and the equivalent inductance of the entire network looking back from the silicon, which is the well-known die-package

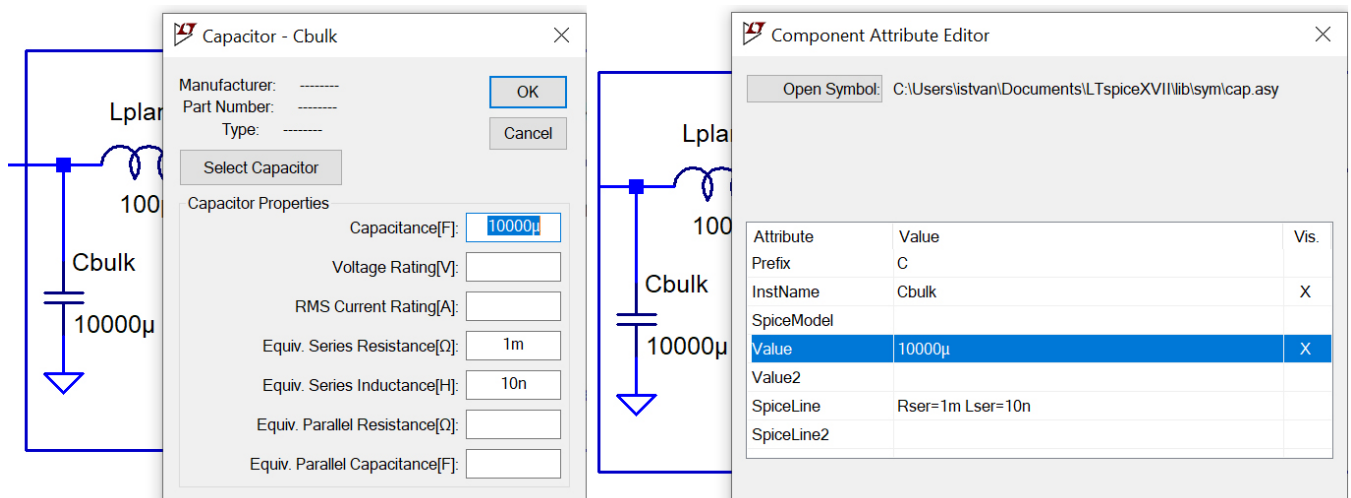


Figure 4: Options to enter parasitic values for capacitors in LTspice.

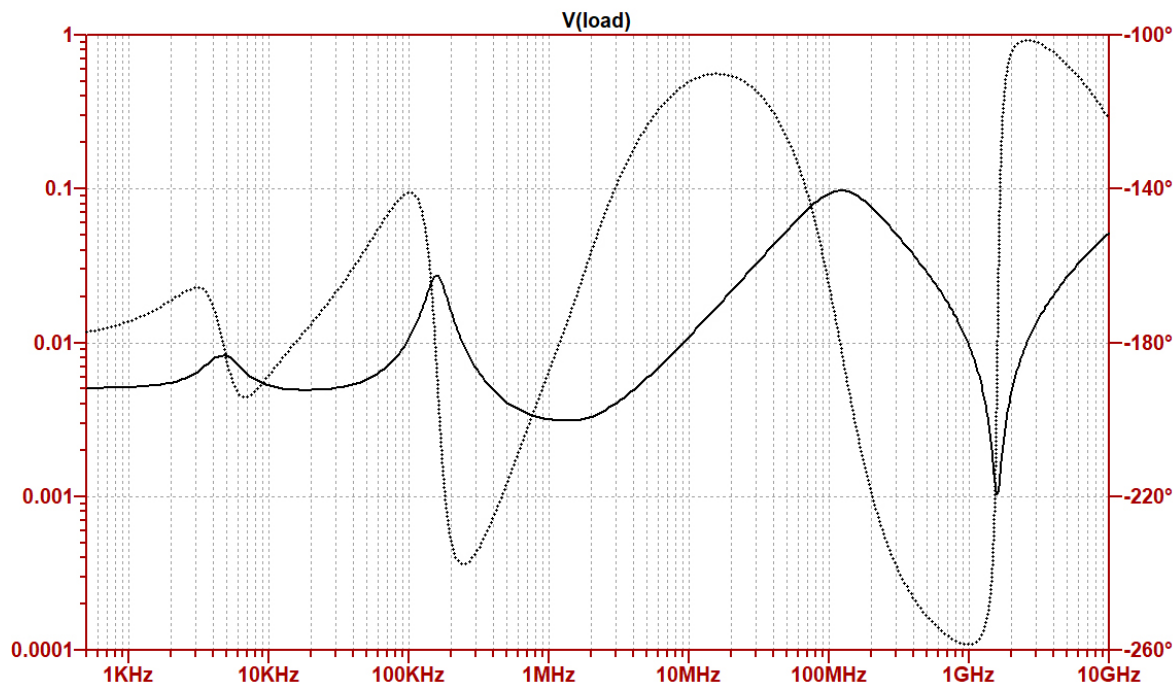


Figure 5: Impedance magnitude and phase of the simple PDN showed in Figure 1, but all parallel body capacitance is set to zero.

resonance. By the time we properly add up all series and parallel inductances, it comes out around 160 pH. The antiresonance with the 10-nF C_{die} value comes out close to 100 MHz, where the split antiresonance peak happens.

We still need to understand where the two extra resonances—Notch 4 and Peak 5—come from. To get the answer, we need to go back to Figure 4 and check what happens with the parameters that we did not fill out. On the left, there are two parameters we left empty: parallel capacitance and parallel resistance. What happens if we explicitly set the body capacitance to zero? The result is shown in Figure 5. Notch 4 and Peak 5 disappeared, but the rest remained practically unchanged.

Now, the resonance pattern makes sense, but there is still something happening. Why do we have 5-mOhm impedance at low frequencies, when the circuit calls out only 1 mOhm and three times 0.1-mOhm resistor values in the series path, altogether 1.3-mOhm series resistance? We need to look at the definitions of the inductors. The definition of inductor attributes is shown in Figure 6 [5].

In the same way we did it for the capacitors, we can call up the parameter-entry win-

dows for the inductors as well. In Figure 7, we see two parasitic components listed: series resistance and parallel capacitance. We also see a note at the bottom of the left window. There is a 1-mOhm default value for the series resistance. This means if we do not make an

L. Inductor

Symbol Names: IND, IND2

Syntax: Lxxx n+ n- <inductance> [ic=<value>]
+ [Rser=<value>] [Rpar=<value>]
+ [Cpar=<value>] [m=<value>] [temp=<value>]

It is possible to specify an equivalent series resistance, series inductances, parallel resistance and parallel shut capacitance. The equivalent circuit is given below:

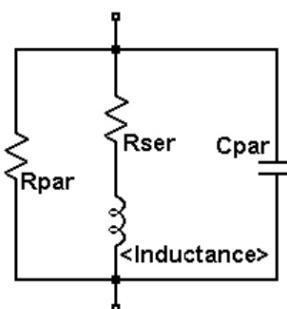


Figure 6: Equivalent circuit of inductor parasitics and attribute list.

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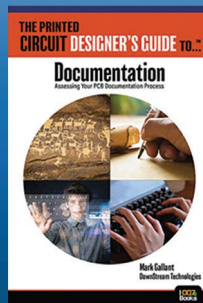
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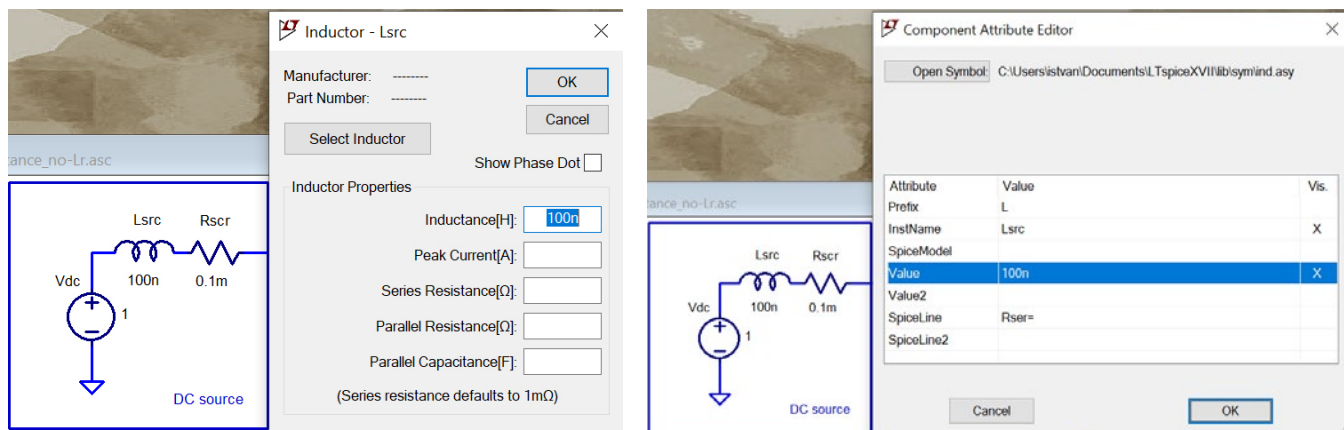


Figure 7: Parasitic definitions of the Lsrc inductor.

entry there, the tool will automatically add a 1-mOhm value (but this automatically-added value does not show up in the series resistance input field). This explains the low-frequency value in Figure 2 since we have four series inductors, each will have 1-mOhm series resistance by default.

If we explicitly call out zero for the series resistance parasitics on all inductors, we get Figure 8. Now, the low-frequency value starts at the correct 1.3-mOhm value, but we can also notice that the first two peaks get a little bigger. This is happening because we removed

the extra series resistances, which helped to lower the antiresonance peaks. Note that with the circuit values used in this example, explicitly calling out zero body capacitance for the inductors will not change the result.

This is eventually what we expect: a smooth impedance profile, no unexpected and unexplained sharp resonances, and asymptotic low-frequency impedance matches the sum of series resistance values.

We are almost done, but it still would be useful to check the capacitor's equivalent circuit one more time and take another look at

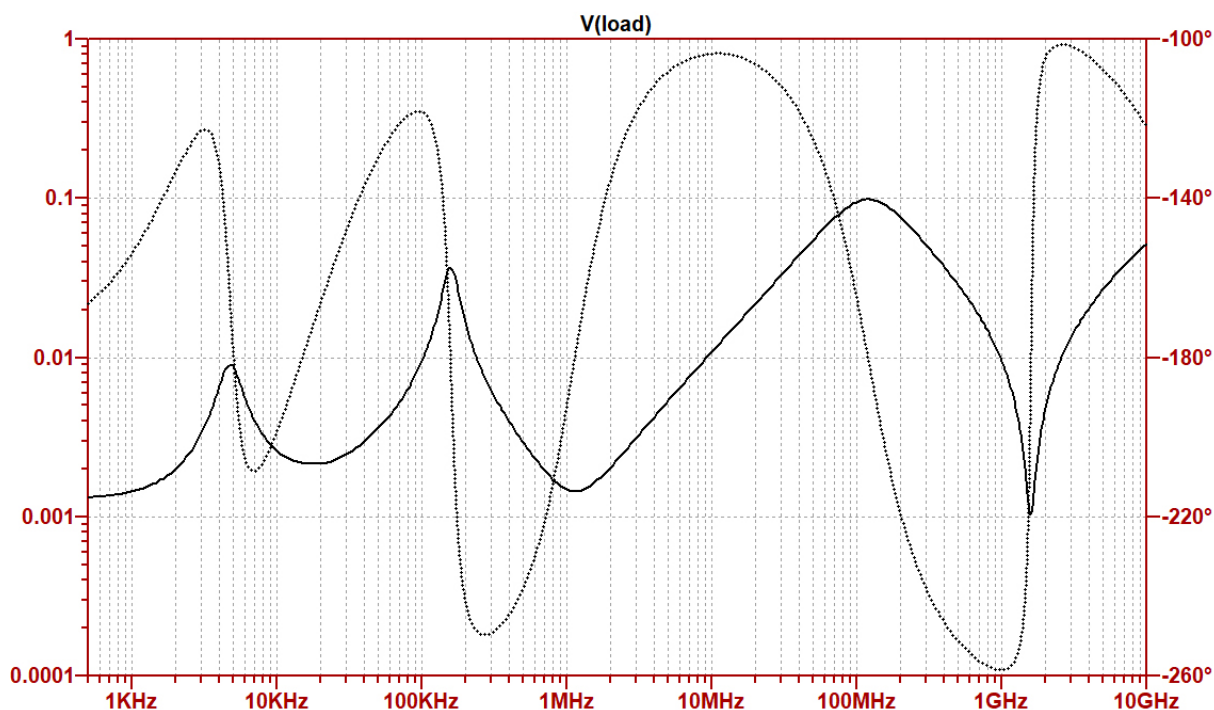


Figure 8: Impedance magnitude and phase of the simple PDN showed in Figure 1, with forcing zero body capacitance of capacitors and zero series resistance of inductors.

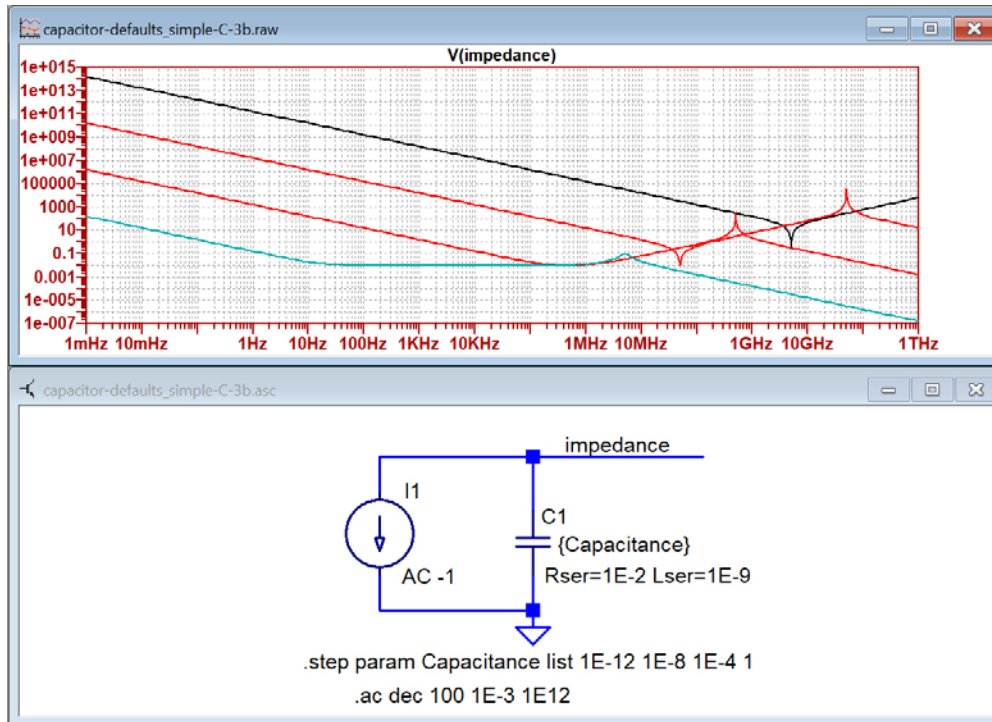


Figure 9: Checking the body capacitance default value for the capacitor model.

the body capacitance. To make it simple, we look at a single capacitor, as shown in Figure 9. We set the main capacitance as a parameter so that we can step it and set the ESR and ESL to fixed values—10 mOhm and 1 nH, respectively. To see what happens, we intentionally do not specify the parallel body capacitance; the entry is left blank.

We step the capacitance from 1 pF to 1F in four large logarithmic steps and sweep the frequency from 1 mHz to 1 THz. The result shows that, in fact, a parallel body capacitance is added by the simulator, but its value is not fixed; it depends on the other parameters. With the values used here, the body capacitance seems to be approximately one million times smaller than the main capacitance. While this looks like a huge ratio (and it is), we see that if we simulate our circuit over many decades of frequencies, this small default body capacitance value still can cause unexpected artifacts. The good news is that it is easy to deal with; we just have to remember to call out specifically zero body capacitance, unless, of course, when we know its correct value and want to simulate the effect of the body capacitance.

And a final note: Remember that all numerical tools have to set limits for the input numbers they can accept and process, whether the tools will tell you and remind you. Next time, when you see unexpected things in circuit-simulation results, first make sure that the input numbers, including potential defaults, are set correctly. **DESIGN007**

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Istvan Novak is the principal signal and power integrity engineer at Samtec with over 30 years of experience in high-speed digital, RF, and analog circuit and system design. He is a Life Fellow of the IEEE, author

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Dear Designers: Please Include a Sanity Check

Feature Interview by the I-Connect007 Editorial Team

No discussion about fab notes and documentation would be complete without the insight from DownStream Technologies. DownStream has spent 18 years developing tools to help PCB designers provide more accurate, complete data packages to the fabricator.

We recently asked Rick Almeida, DownStream co-founder, and Technical Sales Manager Ray Fugitt to discuss why so many fabricators are still receiving (and correcting) inaccurate and incomplete data from their customers. And if fabricators and designers are content with this current process, is it really a problem after all?

Andy Shaughnessy: It's great to speak with you both, even by conference call. Can you tell us about some of the biggest problems that fabricators have to deal with, as far as data from their customers?

Rick Almeida: Ray's experience is actually working for fabricators, so he'd have a pretty good technical knowledge of what some of the

issues are. But from what we see as a company, dealing with this on a day-to-day basis, is that some of the problems are in a couple of different areas. One is there's a myriad of data files that get handed off. The market, in general, is still Gerber-centric and not so much single manufacturing file-centric. Because of that, you have a lot of different data files and documentation to tell you how to use those data files, which creates issues. When you have so many different data files, you run into the issue of if all the data files are there and correct. Does the design itself line up with what the manufacturer is asking you to build? Those are the common things that we see people having problems with. Ray, do you want to add anything to that?

Ray Fugitt: One of the biggest ones we see, and especially since I'm in tech support now, is bad data out of the CAD systems. There is this thought throughout the industry that the CAD systems don't put out bad data, but we see it every day.

Barry Matties: Why are they getting bad data out of the CAD system?



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Fugitt: I have examples. Things like—I'll throw the term out there, and you can put yourself to sleep Googling it—"self-intersecting polygons."

Almeida: It's just a conversion of the intelligent design into unintelligent Gerber files, and what that entails to drive a machine, as opposed to screen graphics.

Fugitt: We're doing a translation, and just to carry that one just a little bit further is it's illegal, per the Gerber spec, to get all the CAD system's output and know how you can go any further with that.

Almeida: It always goes back to that common issue between design systems and manufacturing systems. This is at the end of the process, and it's where the smallest amount of R&D is spent on the manufacturing side of the design tools. And that's a large reason why people are still gravitating toward Gerber files, as opposed to an ODB++ or an IPC-2581 file; they just don't have that experience.



Rick Almeida

Fugitt: I'll go a little bit further with this. I have a major CAD system right now that outputs Gerber data so badly that most users output IPC-274D instead of 274X. If you know the differences between 274D and 274X, it's almost inconceivable. I love that word. Right now, I have a rep in the Czech Republic, trying to write a translator for 274D—remember that there was no spec 274D—and then I have a user in Germany who sent us an example of 274X from this same CAD system. It's unusable, bad data. There's this thought in the industry that Gerber is good, and the simple fact is it's not, in a lot of cases.

Shaughnessy: But 98% of designs are still output in Gerber, right?

Almeida: Something like that. It's still very high. I think the other problem you have is

that the ownership of the design over the last 10–20 years has been shifting from a specialist PCB designer, who had a lot of manufacturing expertise, to the EE, who is often more of a generalist. There's nothing wrong with that, but the EEs now have more ownership of the process, and they're not as well-versed in things like PCB fabrication or assembly. However, they can do everything from chip design right through to the board design and simulation, signal integrity, and so forth. The electronic circuit is getting faster and better and more complex but with the trade-off of less manufacturing information.

Shaughnessy: Now, the data gets to the fabricator's CAM department. What typically happens at that stage if the data package comes in and has incomplete or bad data?

Almeida: We discussed this in the earlier days of DownStream. We talked to fabricators, and some of them told us that up to 50%—or even more—of the designs they received were put on hold because there was an

issue. It either didn't align with their requirements, or there was ambiguous or missing data. But typically, the design goes on hold, and the production process comes to a stop until whatever issue they found can be resolved. Sometimes, that percentage can even be closer to 100% because it's just ambiguous when they get the information.

Fugitt: We spend so much time on database integrity, and now you're putting out data that somebody has to fix before you can manufacture this design. And of course, if you've sent it to me, I'm going to fix it one way. But if you send it to Rick, he may fix it another way. Now, you've lost your database integrity.

Shaughnessy: What is the impact on the job? What happens when fabricators have to deal with this bad data?

Almeida: Somebody has to figure out how to make it correct. Especially in PCB fabrication; it happens in assembly but not as much. You have two distinct groups: one dealing with the design, creating the manufacturing data, and the fabricator, trying to use it. And they're under a lot of time pressures, so they're trying to fix it as quickly as possible. As long as they're not rearranging the circuitry and the connections, they'll make the change on the manufacturing floor, and may not even notify the designer. The worst-case is when you have boards that are built, got messed up, and have to be scrapped. And that can be very expensive, depending on the type of design that was submitted.

Fugitt: And just to take that a little further, when they get in self-intersecting polygons, instead of using their high-end CAM tool to fix them, they are required to manually fix self-intersecting polygons because of the risk. They are risk-averse, as are most fabricators. Again, manually fixing your data is something no designer ever wants to hear.



Ray Fugitt

Shaughnessy: Why do OEMs still let this happen, knowing that it impacts them, and they still end up spending more time on the design, but I know that they're already done with it and moving on to the next design.

Matties: But who's really spending the time? Is it the fabricator spending the time or the designer? Because if it's the fabricator, how does that really impact the designer?

Almeida: Yes, it always comes back to the fabricator. There are a lot fewer of them, they have small margins, and it's a very competitive market for them. Their view is if they don't service their customer, the customer is going to go somewhere else. They try to minimize any perceived problems with design data; if they can fix it themselves, they'll try to fix it, pass it back, and hope for the best.

Matties: How can you help remedy this or transition this thought process? What's your company's impact on this?

Almeida: The way we look at it, we're trying to provide knowledge to the end-users. The first way we provide it is CAM350, for example, and BluePrint; they go hand in hand. BluePrint provides PCB documentation, and CAM350 provides the manufacturing verification of the outputs from the CAD system. Using these types of tools in the design process can help alleviate some of the problems you're going to find downstream. But it also requires a bit of progressiveness on the OEM to adopt these tools into their flow. And when you start adding new tools and processes, it tends to lengthen the design process. Even though it may keep the overall product development process at pretty much the same length, the design itself is getting longer because you're performing more steps in it—but everybody's trying to shorten the design process.

Matties: The case could be made that the slow road is the best.

Almeida: But still, when you're the one there, sitting with the time clock going, and you have to get this off your plate, you're trying to get it as correct and as complete in the shortest amount of time as possible. And it's just a human condition. If I'm done, and I ship it out, a few days later, a package arrives; if those boards are right and working, nobody seems to worry about what happened along the way between those two steps.

It's only when another problem arises that companies get really squirrely—like if they do another revision, or even the same revision—with a different manufacturer who doesn't correct the errors. Then they're stymied as to why one set of boards worked, and the others didn't.

Matties: As soon as it shows up at the fabricator, and your team has to start working on the files, oftentimes, they do it before the sale is even made just to make a quote. I look at that as a cost of sales. And your engineer should probably get a sales commission because they help close the sale.

Almeida: But with the engineer, when they sent that design off, they're done, and there's some transitional time there. By the time any issues may get back to that engineer, they're on a whole different design. They would have to stop what they're doing, bring the other design back up, get re-familiar with it, find out what the issue is, and test it to see how to make the right fix. They've moved on. And I think that kind of transition creates these little hiccups.

Matties: Ray, from your experience, why is a manufacturer going to change? It sounds like this is just part of what they do and part of their value-added services.

Fugitt: It really is. Here's another example from my past. I remember we were getting bad data from one source over and over again, so I said to our inside salesperson, "Let's talk to them and see if we can help them put out a better package." We went over to the Valley, and the designer said, "If you can't deal with the data, we'll go somewhere else."

Matties: We hear that we're in this era of early collaboration, from design with fabricator and assembly. Do you see more of that?

Fugitt: I do a seminar at PCB West every year with Dave Hoover of TTM. We talk about the same issues that we're going through right now. The first thing out of Dave's mouth as an AE is, "I need to be involved in that process before the design even starts." It is the way to do it—to get that person involved early on—and, hopefully, it's the way we're moving as an industry.

Matties: How do we get people to embrace this in a stronger way? Is there hard data or

some empirical information data out there that would make a case? Or how do you get this to happen?

Almeida: I think the first thing is that there's an educational piece to it. When people think about getting a board manufactured—and this is still prevalent in the design community—they look at the design as being that holy grail of all the information. They don't look at the outputs of that design with that same level of importance.

If we, as engineers, were to focus as much attention on the accuracy and the quality of the handoff pieces and deliverables, you'd see better improvement between design and manufacturing. But it gets taken for granted that whatever was on this top layer is automatically going to get translated into the top layer of the Gerber file when it's a translation in both cases, and whenever you have a translation, it would behoove you to verify that that translation happened correctly.

Matties: My understanding is that it could be a multi-day process to create a proper set of fab notes.

Almeida: It is, and a lot of these companies are smart, where they have templated fabrication notes, but they change based on the features of each different design. Fab notes are good, but in reality, they're only one piece of the holistic documentation piece, specification, or product. And what's happening is, more and more so, the fabrication drawing seems to be further and further neglected. We tend to rely more on text, as well as assembly vs. the fabrication process. But both pieces of documentation are equally important.

Matties: Are the tools getting better, in terms of being able to provide the graphics and the necessary data?

Almeida: They are. If you look at BluePrint, one of the reasons why we did it was to unharass all the CAD limitations for preparing documentation so that you'd have more flexibil-

ity in creating the type of documentation you need to convey the specifications. That's what a fabrication drawing is. It's a specification for the PCB component—how it's supposed to look, how it gets finished, how it should perform, and what type of manufacturing issues or deviations you can take during the manufacturing process. They're all part of it, and they all go together.

Matties: You mentioned people may start with templates, and my understanding is, when you start with the template, you often wind up with conflicting notes on a particular job. That creates additional confusion and delay.

Almeida: Right, and think of it, too. It's just not writing notes to tell somebody else what to do. The fabrication documentation is just as important for the company creating it as it is for the manufacturer who has to read it. The more information you give them, the better chance they have to meet your requirements. But it's also the company's record of how this thing is supposed to be built, and not just today, but 10–15 years from now.

Matties: I had not heard it from that point of view. That's an interesting angle to consider.

Almeida: PCB documentation is not the glamorous side of the design process. We tend to look at it and complete it, including all the manufacturing outputs, as quickly as possible, but it's the form, fit, and finish specification of that end-product; it's the record of the product. The design file is just the enabler to that.

Matties: What advice would you give designers on this topic?

Almeida: Don't assume it's going to get built the way it looks on your screen. You need to verify that what you translated out of that database matches what the database says for the first step. If you're not familiar with simple things like netlist compare, that is just a small effort that could have huge returns on the quality and accuracy of the design.

Fugitt: Let me just jump in for one second, Rick. I call it a sanity check. It is the single most important thing I think a designer can do before sending their data off—a simple netlist comparison. It was the '90s when it became required, and people would say, "What is it?" Then, I started with DownStream in the 2000s and would tell people, "You need to do this." They would look at me with blank stares, but now we see some real progress there. It has become a standard part of the process, and it is a sanity check.

I call it a sanity check. It is the single most important thing I think a designer can do before sending their data off—a simple netlist comparison.

Shaughnessy: Let's talk about IPC-2581 and ODB++. How does that change the fab notes situation?

Almeida: It's also a translation. For example, when we design a board, you have layers, vias, and components, and they all have intelligent interrelationships between each other. This trace on the top layer knows it's connected to these traces on the inner layer and the bottom layer, and they know what components they go to. When we create Gerber information, we strip all that intelligence away, and we create different files. What these intelligent formats do is take that ambiguity away because they give you a manufacturing file that is a direct correspondence to that intelligent database.

Fugitt: One of my favorite classes at PCB West a few years ago was presented by Mike Tucker. He was a fabricator and showed the cleanup that has to be done on the data incoming to fab. He spent the first 30 minutes of that pre-

sentation going through that whole process, and then he said, “If you were to send me ODB, I wouldn’t have had to do any of that.” That statement applies to IPC-2581 now as well. All of these different files are disconnected, and by sending these intelligent formats, I don’t have to do any of that.

Almeida: It’s a funky thing when you think about it. We take an intelligent design—a single entity—and split it into all these different files that have no relationship. Then, we ask a third party to read this drawing or these notes and put all that information back together again correctly to build the board where these ODB++ files and IPC-2581 files already do that for them. Otherwise, it’s like taking a chicken, making chicken nuggets out of it, and then trying to make a chicken out of it again.

Fugitt: With IPC-2581, one of the things that all the CAD systems do have is the ability to remove some of that intelligence and still send out a good portion of it, so if you do have security concerns, there are ways, especially with IPC-2581, to provide just what that part of the industry may need. A fabricator doesn’t need to know what components are going on the board, right. Why send it to them and be worried that they’re going to steal your design? I don’t think a lot of designers realize that. They think they have to dumb it down to Gerbers in order to ensure their security.

Matties: The choice for the designers is do they want more control over the output or to relinquish the control to the fabricator and let them interpret and then verify back?

Almeida: I’m not sure they even look at it that way. I think it’s more of this thinking that it had better come back correct.

Matties: But on a scale, the risk is much higher when you go the route of not owning the notes yourself.

Almeida: It does create more risk when you leave it up to somebody else to make those decisions.

But most of the time, it’s an accepted process that goes on, and it has happened for years and years. Now, individuals are assuming responsibility for processes that have even less understanding of what occurs back there, so they’re more reliant on the manufacturer to get it right.

Matties: That goes back full circle to the idea that in collaborative manufacturing, early communication is more necessary than ever.

Almeida: Exactly. We wanted to build as much manufacturing knowledge into the tools as we can so that these engineers can at least have more guidance going through the process. We can attribute layers in groups so that all of the copper layers appear as copper, all the dielectric looks like dielectric, masks look like masks, and so forth. The other piece we do as well is that with design analysis, we’re able to allow board engineers to pick their fabricators and outline or profile all of their specifications and requirements.

Matties: You must have that fabricator data available, and my understanding is not all of that is always available.

Almeida: Not all of it, but you usually can get it. A lot of your prototype shops typically provide all their specs online. With your bigger production houses, you typically can call them, and they’ll tell you. They want to work with you ahead of time. They don’t want to have these delays. The delays cost them money as well because they have to start and stop jobs mid-process. They’re more than willing to share those specifications with you. It’s just a question of making sure that the communication happens. And that’s where the onus falls on the OEM to change their processes to resolve that delay. It’s unnecessarily lost time to market, especially now when you have products that have short product life cycles of 12 months or less. Every week counts.

Matties: My understanding is that some fabricators offer incentives and price discounts for complete and accurate data packages.

Almeida: Yes, the smart ones do.

Matties: It seems like if you incentivize and monetize it, it's going to maybe be a catalyst for some shift in thinking.

Almeida: And the other problem is that fabricators' margins are already so thin that it's a catch-22 for them. It's like, "I'm going to put some of that margin back into this with the hope that it's going to make the aggregate bigger." They tend to look at it as, "I know what this is going to be. I'm better off with the devil I know versus the one I don't, even though that one couldn't really help us out financially." It creates another conundrum.

Matties: Right, that's a whole different topic. But we have been talking about the profitability of fabricators and how there's still quite a bit of profit left in fabrication if you start eliminating the waste in the process.

Almeida: Exactly. It's like leaning into a punch a little bit, or when your car's out of control, you turn into it as opposed to away from it. It's not a very intuitive reaction.

Matties: This has been great. Is there anything we haven't talked about that you feel should be included in this conversation?

Almeida: It's just interesting that we could have had this same conversation 15–20 years ago.

Matties: Thank you both for your insight.

Almeida: It's always a pleasure speaking with you all.

Fugitt: Thank you. DESIGN007

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NI, Eta Wireless Accelerate Wideband Digital Envelope Tracking

International Microwave Symposium (IMS)-NI is collaborating with Eta Wireless to implement and demonstrate full support of ETAdvanced, the industry's first ever Digital Envelope Tracking (ET) technology for mmWave 5G RF front-end devices. Developed by Cambridge-based Eta Wireless, the technology enables extended battery life in smartphones, wearables, and IoT devices, improving both data rates and connectivity range.

ETAdvanced addresses the power efficiency challenges that have historically plagued RF front ends. Wideband power amplifiers (PAs), such as those found in 5G devices, waste a significant amount of power in the form of heat, greatly reducing battery life. ETAdvanced uses the signal's envelope information to increase the amplifier's efficiency by delivering only the power needed at that instant.


Full support of ETAdvanced was achieved using NI software-connected PXI systems, making

possible a tightly synchronized combination of fine digital edge placement, as well as wideband 5G new radio generation and analysis with the mmWave Vector Signal Transceiver (VST). These technologies helped Eta Wireless demonstrate a data rate improvement of 3X and the doubling of the PA's output power, addressing core power and thermal problems of 5G mmWave deployments. This makes ETAdvanced technology a key enabler for mmWave 5G radios.



"At NI, we equip our customers to engineer ambitiously by providing the tools and expertise required to help them test new ideas," said Ritu Favre, senior vice president and general manager of NI's semiconductor business unit. "Connecting Eta Wireless with technology that helps solve one of the biggest challenges facing 5G adoption is at the heart of our vision to accelerate 5G commercialization."

[Source: Business Wire]



PRACTICE
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Monsoon Solutions: Creating Perfect Fab Notes

Feature Interview by the I-Connect007 Editorial Team

When we started planning this issue on fab notes, one company's name kept popping up: Monsoon Solutions, a design bureau in Bellevue, Washington. Monsoon has spent years optimizing the company's approach to the process of creating fab notes and packages, as well as dealing with customers' fab notes that often contain missing or erroneous data.

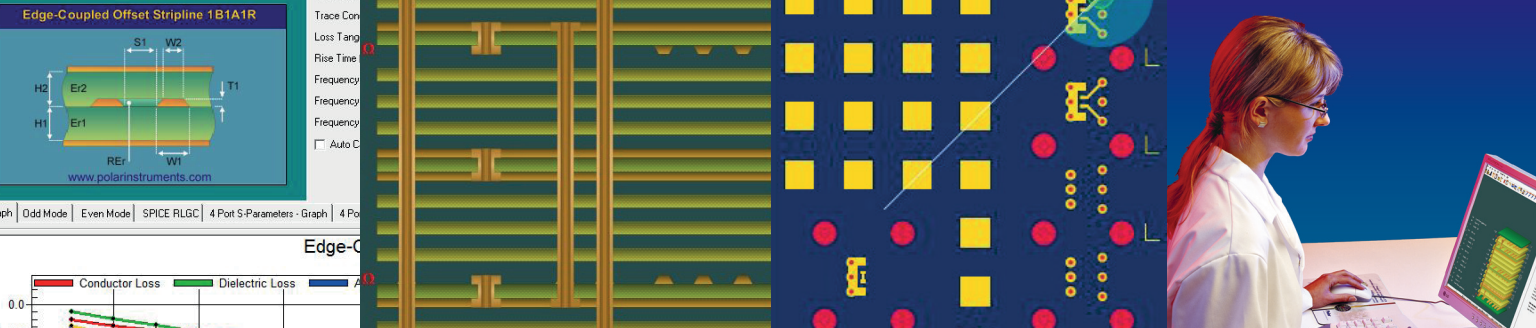
We recently spoke with Monsoon's Jennifer Kolar, vice president of engineering, and Dan Warren, principal PCB designer and director of designer development, about some of the common problems they see in designers' fab notes, the impact that bad data can have on the fab process, and the steps that designers and design engineers can take to ensure that they are creating complete, accurate fab notes every time.

Andy Shaughnessy: Why don't you all start by describing what fab notes and manufacturing notes are, and what they're supposed to accomplish.

Jennifer Kolar: Fabrication notes and manufacturing notes go along with the actual data for a build and should detail all of the requirements for the fabricator and assembler. Fabrication notes should include things like stackup, drill charts, drill drawings, board outline with dimensions, build and testing requirements such as IPC class, and any special customer requirements, potentially including panel requirements. Assembly notes should include all reference designators, polarity markings, and special process instructions such as type of wash, labeling requirements, etc. These notes, along with the manufacturer's quote and stated exceptions, essentially become your contract of what they have agreed to build for you. If you don't have it documented, you don't have anything to fall back on if the shop doesn't build the boards the way you intend.

Shaughnessy: I've heard that Monsoon creates perfect fab and manufacturing notes. Tell us about that.

Kolar: At Monsoon, we've now done more than 13,000 unique designs. We've had a long

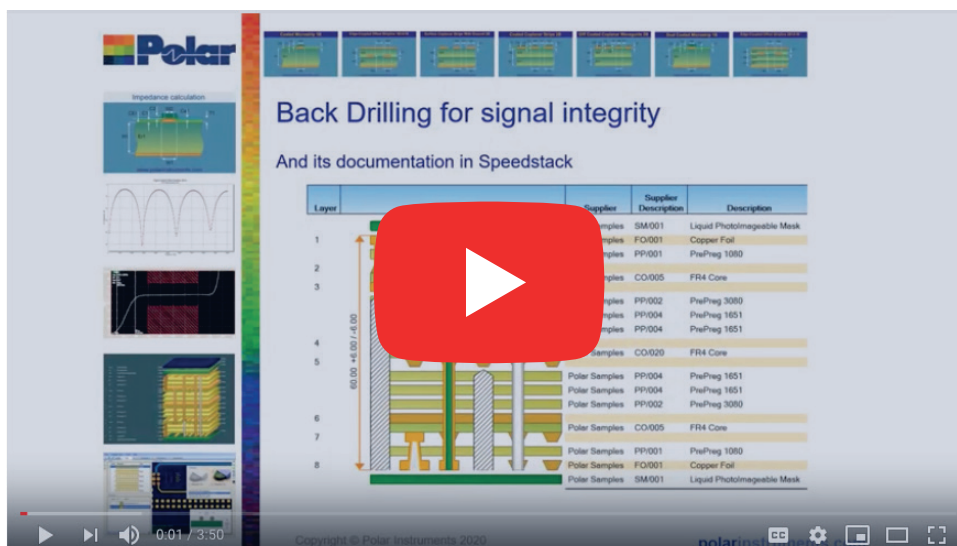


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time to fine-tune and dial in a process that works. Our company is split evenly, as a service bureau, between design and manufacturing. We have our people all intermixed and working closely together. One thing that gives us an advantage is our designers hear first-hand when the program managers (PMs) are getting questions from the fab vendors or problems from the assemblers—as well as when builds get delayed—so that they're very aware of the back and forth process.

From the manufacturing and requirements side, we worked with quite a few different fab vendors, both in coming up with standard templates for quotes and stackup requests, and then also what works well in our fab notes. From that side, we've helped the design side understand, "Here are the things we get questions on, that might add a day or two to the build, and that might add cost to a build."

One of the things about Monsoon is that we do a lot of builds for people that want it yesterday. We optimize to have no delays. Our biggest delays come from poor assembly diagrams that don't match with silkscreen on the boards that are missing reference designators, or polarity markings, and poor fab drawings. Those are the two biggest sources of delays. After that comes, "There was a footprint mismatch."

Barry Matties: How much extra time do you have to spend on a job to make it accurate when you send it to the fabricator?

Dan Warren: For us, not much, really. It's all part of a larger process. If you don't have a process in place, and you don't have anything documented, you're going to waste a lot of time making sure everything's accurate. If you leave it up to 13 different designers to do it with no process in place, you're going to get 13 different sets of documents. The fab notes are just



Jennifer Kolar

a small part of it. We have a series of internal documents that we've written, and one of them handles what goes in our output packages because we have multiple CAD tools, and they're all a little bit different.

We also have specific customer requirements. Some of them use our notes, some use their notes, but that's also documented. The designers are expected to know this process and look at it once in a while. We try to implement a continuous improvement process where just

because you did it and it's done, don't ignore it for three years. About every six months to a year, we'll go through the documents and refresh them. I also have a folder in my inbox. If any designer comes up and says, "This note is out of date," I make a note about how this needs to be updated and we get it done. That saves us a lot of time when it comes to the process.

The first time through, you can do a drawing quickly. You can get your fab data out, and then if something minor changes and you have to reprocess it, you know it's all golden and ready to go; you can reprocess it in half an hour without having anything automated. We live by the rule that if it's not on the board, it shouldn't be on the drawing, because that just confuses the fab shop.

If you have notes about blind and buried vias, but you have a through-hole board, those notes need to come off. In our standard notes templates, we have notes for blind and buried vias and via-in-pad different finishes. Pick the ones you want and get rid of the other ones.

Kolar: We have predefined templates for different drawing sizes and ideas of where we want things to be on the drawings. "Your stackup should appear here. Your drill charts should appear here. We want things to all look and feel the same."

Matties: How much time do you think you save by doing it right the first time?

Kolar: Pretty much any time you get a question, depending on the fab shop—and especially if you’re dealing with an offshore shop—you’ve just lost 24 hours. When you look at clock time, or if you’re doing a really fast build—such as if you’re doing a 24-hour or 48-hour build—every second counts on those builds. Some iteration on fab note packages can cost multiple days.

We have an internal design review process. One of the areas that we have people really emphasize and focus on is the drawings, going through the fab and assembly drawings. They have a whole checklist they need to go through. That typically can take 30 minutes to one hour for a board. We decided it was worth the overhead time that we have a peer review for every project.

Matties: How is it that you understand so much about the manufacturer that you’re contracting with or sending the job to?

Kolar: This is one of the things that we have an advantage in. Half of our people are our PMs who are technical and focus on manufacturing. We have about 10 different fab vendors that we work with, so we know what their capabilities are. When we send quotes out, we don’t just throw them over the wall. We know by the time we send a quote out who we want to go to, and whether it’s based on technology, time, or price point. Sometimes, we’ll quote a couple, but usually, most of our vendors know that if they’re getting a quote request from us, they’re going to get the project if we get it. That allows us to also iterate with them, and that means we know the technology of our vendors really well.

We know, for this particular vendor, you’re doing a rigid-flex. You need to make sure there’s this much pullback between the separation of these layers. Or we know this other vendor might get confused about something, so, “Let’s make sure we call it out specifically.” We try to educate our PMs on what to watch

for that they might need to call out to a vendor as unusual; this is more of an issue if we don’t do the design internally. For example, maybe this is referencing a stackup outside of the fab drawings. We try to have it explicitly called out to help the fab vendor.

Matties: We hear a lot about DFM and design for automated assembly. How does all that play into your process there?

Kolar: We use CAM350 as a pre-DFM tool internally. We have some streams based on different technology levels, and they are an automated way to do different rule checks on boards. We have some based on low-tech, medium-tech, and high-tech. We’ve started looking to do some in specific shops. After we’ve done all of our layout checks, we also required designers to do a number of CAM350 checks that look for things that might be issues. Designers might send an internal email to the team, asking, “Remind me of how much pullback I need here, or what clearance do I need here?”

There’s a lot where we just use best practices, based on experience. This is where Dan ends up being a huge resource for a lot of people. Our team members are a resource for each other. Following best practices resolves 99% of the issues. If we go outside of best practices, that’s when we ask in advance, “Can you handle this aspect ratio? We’re going to want to do something funky.”

Matties: Oftentimes, we hear that designers design in a vacuum, not knowing who the fabricator will be. It sounds like you know in advance who you’re going to use for particular jobs. That’s a huge advantage.

Kolar: We do. If we’re doing the manufacturing, our designers will know, and they’ll work with the project manager to get a stackup specified. We’ll know up front who the shop is and what the capabilities are. The PMs are savvy enough to know, and the designers are savvy enough to say, “I’m going to do something kind of funky. Why don’t you go check with the shop to see if they could support this?” Where does

this impact turn time? Where does this impact pricing? If I can stay above this spacing, is that going to drastically help manufacturability? And they know the sweet spots of each of our shops. If it's a customer that's doing the manufacturing, we'll work with them up front and say, "We need to get a stackup from your vendor."

We may not know the name of the company, but we'll still be working with that vendor up front. We avoid things like guessing at stackups. We tell our customers that we don't want to wait until the last minute to define the stackup. Then, we have fun times where people might want to support multiple vendors. That's another kind of fun trick. How do we design for that and document that?

Matties: We've talked about time, but are you also adding capacity back to your team as well so that you're able to get more throughput?

Kolar: Absolutely. Typically, when we do quotes for manufacturing, we're trying to get data that helps things go smoothly downstream—and this is the other thing Dan described—the life cycle that we have on the design side of the process. We ended up building this giant flow chart that's bigger than the biggest whiteboard in our office, which shows our entire life cycle process. It explains where things are jumping in and out for quotes, as well as all the validation and checkpoints; it was an exercise we did for our customers on best practices. Some of the things we do that save us time up front are that collaboration with the designers and the PMs and the fab vendors.

The second we have placement locked or mostly locked, and we know the rough size and dimensions, that's the perfect time to get a provisional quote for fab. You don't have to wait until later, and that allows you to call out red flags of, "The stackup isn't possible," or,



Dan Warren

"What do you want? What are the trade-offs that you can make?" From our side, we want to be able to get quotes back from our fab vendors within a couple of hours. A lot of times, our customers look for quotes from us really fast. We can't be in a business of sending crap data over the fence and having them spend hours trying to understand it back and forth, especially if we're working with an off-shore shop. We don't have the luxury to be inefficient.

Even if we don't have completed fab notes, we pre-defined a template to use for getting fab and assembly quotes. I'm the one that did those years ago. I worked with six or seven different fab shops and assemblers and asked, "What would be the best thing for you?" That helps our designers, too. Maybe they don't have the fab notes done yet because a lot of times, the fab notes are kind of near the end; instead, they can fill out this form and give us provisional data that gives the fab vendor everything they need. Then, we get provisional quotes, and then the fab notes help the fab vendor do a final vetting and final quotes. We're able to get quotes back within a couple of hours, usually from our fab vendors, because we know what information they need and don't need.

Matties: Why do you think there's such a challenge for designers to get the jobs to fabricators with 100% accuracy, with all the documentation? What's the issue?

Kolar: A lot of it is just time. The customer is focused on the base electrical connection. They're focused on how everything looks in the data, not the package itself, and they're like, "Get it out. It's done." They don't care about all the processing time.

Matties: But in the end, they're going to wind up spending more time.

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Kolar: Absolutely.

Warren: It's really hard to teach that to them, too. As Jen said, when you get to the end of the design, it's usually late because of changes, and this spin is behind somebody's schedule. Whether it's the latest schedule or someone higher up had different expectations, and people want to rush it out the door because it's connected. Get it out. A lot of people don't take the time to process things properly.

I also get feedback from our project managers. If any given project doesn't go smoothly, I usually have one of them contacting me and saying, "Why did this not work the way it was supposed to?" I'll say, "Did we do a design review?" or, "Were processes followed?" And if they weren't, I try to figure out why and I try not to put anyone on the spot. A lot of times, I'll use a blanket, "Remember to do this and tell the whole group," because nobody likes to be on the spot.

Whether it's the latest schedule or someone higher up had different expectations, and people want to rush it out the door because it's connected.

Matties: We always say attack the process, not the people, because it's the process that fails.

Kolar: Yes. We build a lot of designs that we didn't design. We get designs from our PM side, and we're constantly getting Gerbers thrown over the wall and projects thrown over the wall where the customer has no access to the original designer. They don't know any information other than what they provided, and maybe they have some access, but it's really common to have things thrown over the wall that we have to figure out. From the PM side, we have a lot of experience in dealing

with incomplete or imperfect data and trying to turn that into something reasonable to give our fab vendors.

Matties: And you extend the impact of time on the process.

Kolar: Right. We'll end up doing pre-DFM for some customers, or they'll say, "We're doing the design, but can you just go through and tell us what the obvious non-buildable issues are? Can you tell us what's wrong?" That's something we offer. Depending on the size of the project and how frequent the customers, either we just do it, or we might charge them for a few hours.

Matties: I would think that external designers would come to a service like yours and request the same sort of review, especially for the more difficult or challenging job.

Kolar: They do. The trick to that for us as a business is this: How deep do you want the review? "We need a review right now. We want to go to fab in two hours, can you do it right now?" or "We're doing a cursory review." We look for obvious red flags. That's typically what we end up doing because people don't want to pay or take the extra time. By then, it's already past you and down the channel.

Johnson: Early on, you said that the fabricators you work with give you some price breaks. On your side of the conversation, it's monetized, and you can put some dollar value to it. What kind of dollar value are we talking about?

Kolar: It can be a 5–10% difference on a fab, and that's not insignificant, especially when you're dealing with smaller margins or expensive builds. Because of our volumes, we can also get priority queuing and support with our regular shops.

Johnson: It seems to me that a fabricator could put together some pricing that encourages customers to move things through faster.

Kolar: We've seen assemblers do that more often than fabricators. For example, I've seen some assemblers say, "If you don't provide ODB++ data, and if we just have to work with pick-and-place data, it's going to take this much longer for setup. We're going to have to do this programming. We're going to do this tooling." I see assemblers doing that more now where they really take into account the manual effort. I don't see fab shops doing that as explicitly.

We have some customers who insist on designs being WYSIWYG: whatever they produce, the fab vendor must build and not touch. We try to push back on our customers with that. There are things we say, "Let the fab house do this. Let them specify the panel.

Here's within 5 to 10% tolerance for trace and space. Feel free to tweak it." There are certain things we feel it is better to have the fab shop do because it's optimized to their process.

It would be a good question to ask the fab shops: Which of these things are reasonable to expect them to do, and that they prefer to do? And which ones are we just assuming they prefer to do? Because that's where we really like to push back on customers who want us to predefine panel drawings and panel arrays or predefine that we've pre-expanded. We avoid doing pre-expansion and try to do one-to-one design. The shops can optimize that. **DESIGN007**

Part 2 of this interview will appear in the September 2020 issue of *Design007 Magazine*.

SparkFun, Alchitry Bring FPGA Hardware and Software to Electronics Enthusiasts

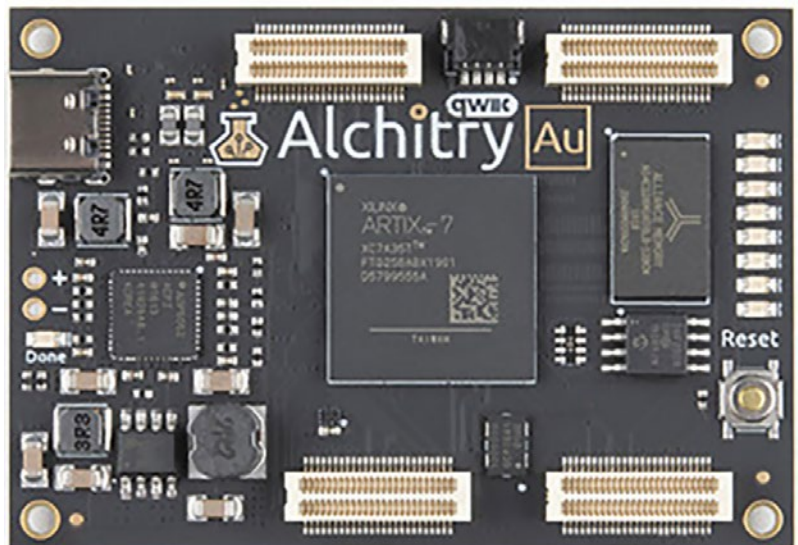
SparkFun Electronics and Alchitry are pleased to announce they have entered into a strategic partnership, combining SparkFun's logistics and hardware expertise with Alchitry's FPGA knowledge and experience.

SparkFun will manufacture and distribute Alchitry's line of FPGA boards, allowing Alchitry to focus on designing the next generation of FPGA hardware and software. The Alchitry Au and Cu boards will now come equipped with a SparkFun Qwiic connector, allowing users to easily interface with over 100 development boards, sensors and relays over an I2C connection. The addition of Qwiic to Alchitry's FPGA boards opens up the possibilities of designing with FPGA to near-limitless potentials.

"While FPGAs have been a niche component in the electronics industry for decades, the advent of FPGA-based solutions for machine learning and the ability of FPGAs to model CPU core designs is leading an expansion of FPGA use within the prototyping and research markets. With this partnership, we will be able to combine SparkFun's market presence and manufacturing capabilities with Alchitry's FPGA knowledge and experience," said Glenn Samala, SparkFun CEO.

"Alchitry was started with the goal of creating an FPGA board that was accessible to anyone with the motivation to learn digital design. As we evolved to include tutorials and the creation of software such as Alchitry Labs and Lucid, it became increasingly difficult to balance the manufacturing and production of existing products with the creation of new products, more tutorials, and better tools," said Justin Rajewski, Alchitry founder.

(Source: PR Newswire)



The **Nuts** and **Bolts** of Electrical Testing

Connect the Dots

by Bob Tise and Matt Stevenson, SUNSTONE CIRCUITS

Electrical testing verifies connections and paths in a PCB to ensure that current is moving in the proper way between components. Whether you're a beginning PCB designer or a grizzled veteran, electrical testing is an important step in PCB manufacturing. Without it, you might just end up with a useless chunk of substrate and copper.

In this column, we'll explore the world of electrical testing. We will examine a variety of testing methods, what options to look for in a PCB manufacturer, and how to ensure that you're getting the best value out of the electrical testing options available to you.

The Lingo of Electric Testing

Like everything else in the world of electronics, electrical testing has its own vocabulary. Before beginning our exploration, let's get a handle on the jargon.

Net

A net is, to put it simply, a circuit. Your CAD tool can output a specially formatted list of nets or circuits in your project known as a netlist. This is required for certain manufacturers.

Opens and Shorts

An open is a break in a net or circuit, while a short is as you would expect—an undesired connection in a net or circuit.

Bed of Nails

Also known as a clamshell or universal grid test, the bed of nails testing method uses spring-loaded, fixed contacts to test circuits on a PCB. This method is best for high-volume production, where a lot of speed is needed in testing.

Flying Probe

A flying probe test uses software-configured movable contacts to test circuits on a board





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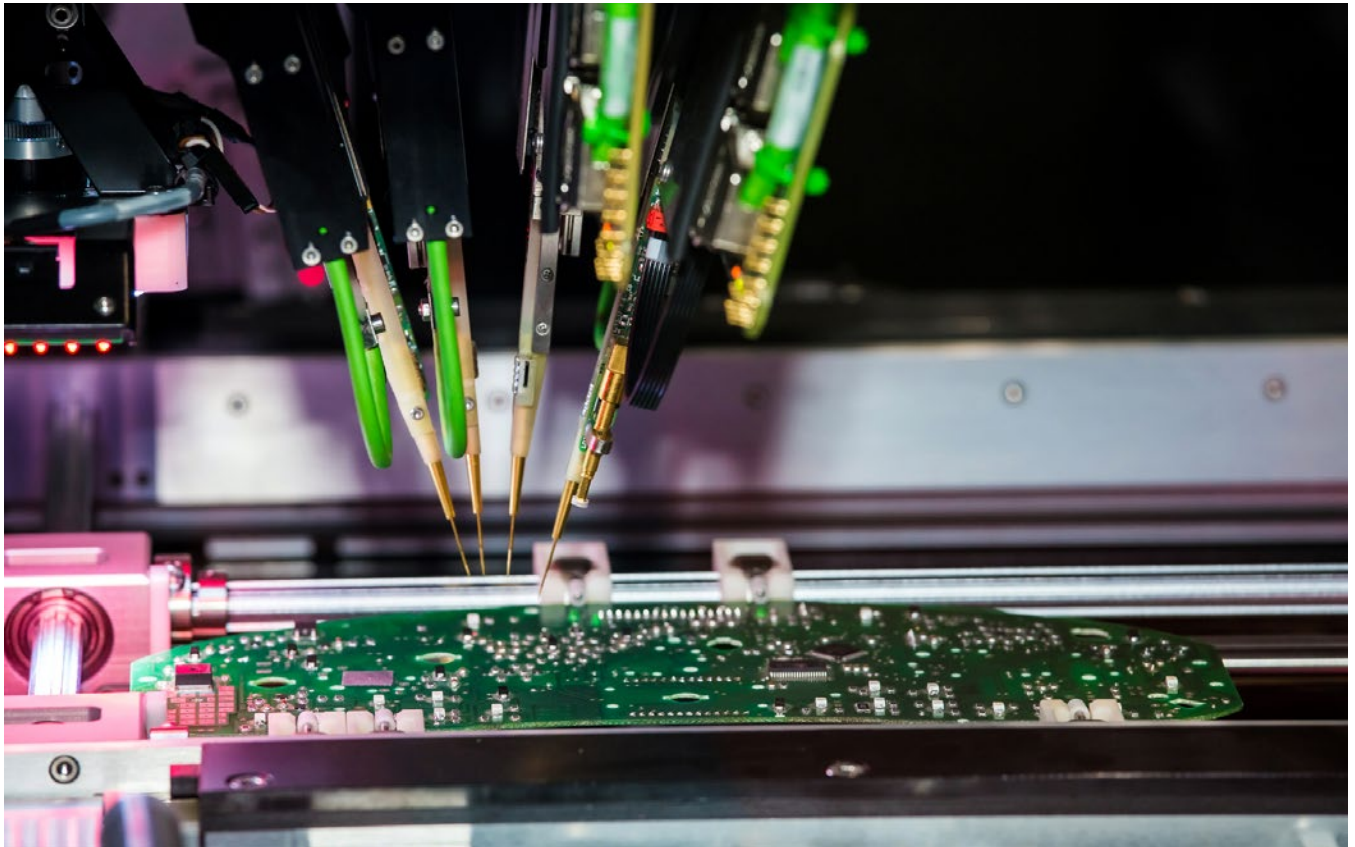


Figure 1: Examples of flying probe test.

sequentially (Figure 1). This method is slower than the bed of nails method but more flexible. It is perfect for prototypes and smaller print runs.

Bare Board Testing

This is a method of testing where isolated circuits are tested for continuity before components such as resistors and ICs are attached. Both bed of nails tests and flying probe tests can be executed as bare board testing.

IPC-9252

This is an industry standard document that lists the requirements for an electrical test. You don't necessarily need to read this document, but when an electrical testing service lists this, know that they are suitable for even the most rigorous of testing for commercial PCB purposes.

IPC-D-356A

This is a standardized format for netlist files. While important for verifying all the nets in a

PCB, it lacks the precision and data accuracy of a Gerber file.

Why Is Electrical Testing Important?

You're the one who spent hours and hours designing and building a circuit, as well as carefully configuring a design in your CAD tool. You are probably confident that your PCB is ready for production, but the transition from digital design to physical reality can bring surprises, even for the most experienced PCB designer.

The main objective of a PCB is to create a path of current across circuits in a defined and predictable way. Even though you've spent a considerable amount of time connecting and isolating the individual components of your design, there are a lot of considerations when it comes to a working layout. This is where electrical testing comes into play and saves you from frustrations and delays.

Without electrical testing, you could end up with a batch of PCBs that don't function properly. This could be because of faulty design. But

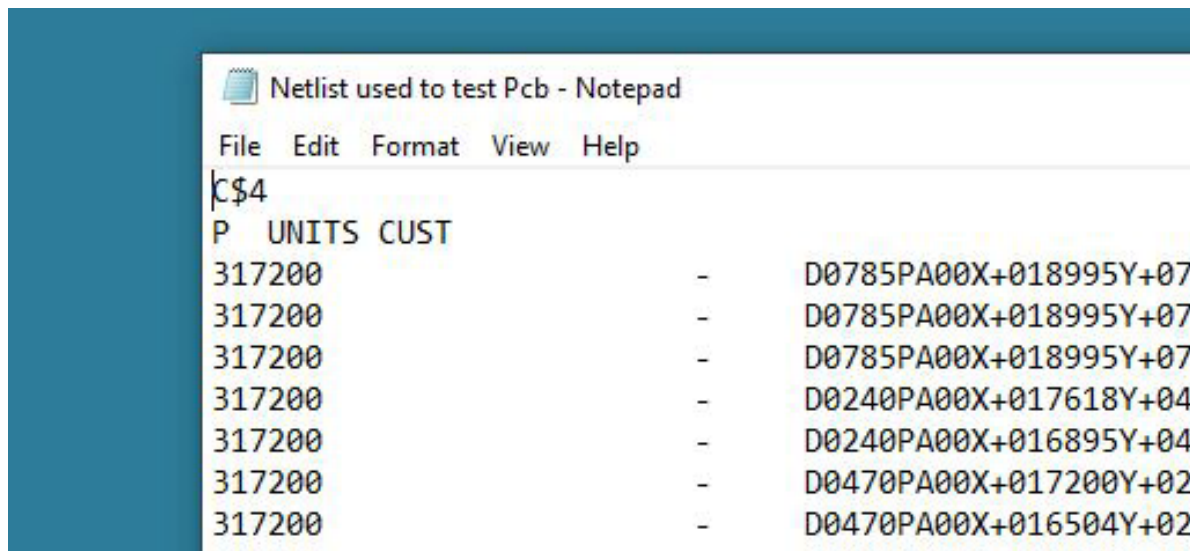


Figure 2: A typical Netlist for testing a PCB.

it could just as easily be because of manufacturing limitations at your PCB manufacturer or incompatibilities between your CAD's export files and PCB manufacturing processes. The only way to make sure none of these issues get in the way of properly working circuits is with electrical testing.

The Electrical Test Process

Your PCB manufacturer will perform electrical testing based on the information that you send them. Some perform testing straight from Gerber files. Other manufacturers will want you to generate a separate netlist file. Your CAD tool will have specific instructions that lead you through this process.

The Gerber or netlist file contains all the information necessary for your PCB manufacturer to create automated electrical tests. This includes individual nets, pad geometry, the location and sizes of through-holes, and solder mask openings. The testing process ensures that all nets are connected as expected and that no extra connections are created during the manufacturing process.

What to Look for With Electrical Test Services

Now that we understand the importance of electrical testing, we can spot some information to look for when picking a PCB manu-

facturer. You'll have different criteria based on the scale and where you are in your production. If you are just producing a few boards, either because it's a small project or you're in the prototyping phase, look for a manufacturer that performs a flying probe test.

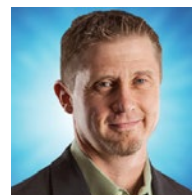
However, if you're looking for a major PCB run, it might be more cost-effective to find a manufacturer with a bed of nails testing option. Depending on the scope of your project, you may want to pay extra for IPC-9252 certification for your electrical testing.

Most importantly, electrical testing gives you the peace of mind that the manufactured PCBs shipped to you match the design files that you submitted to the manufacturer. This is the best way to make sure you aren't submitting faulty PCB designs, which will save you time, money, and headaches. **DESIGN007**

Bob Tise is an engineer at Sunstone Circuits, and **Matt Stevenson** is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Tise and Stevenson, [click here](#).



Bob Tise



Matt Stevenson



The Role of EDA Tools in Creating Fab Notes

Feature Interview by Andy Shaughnessy
I-CONNECT007

When discussing fab notes, there's a lot of focus on what designers should and should not include in the package. But what is the role of EDA tools in this process, and can intelligent data formats streamline the tasks and help eliminate fab notes that are less than fantastic? In this interview, Pat McGoff, market development manager for Mentor, a Siemens Business, speaks frankly about fab notes and what EDA tool companies like Mentor can do to automate this process.

Andy Shaughnessy: What do you think are the biggest problems that PCB fabricators face regarding designers' data packages?

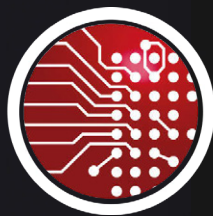
Patrick McGoff: The biggest problem with the designer's data packages is the confusion they often cause. Like other contract suppliers, PCB fabricators make every effort to be as accommodating as possible in terms of what kind of design data they will accept. I can remember when fabricators would take in a scanned

image of a PCB and digitize it to reproduce the board.

Today, when we say, "Send us the Gerber files," what we are really saying is "Send us the Gerber, drill, and netlist files, along with drill drawings, route drawings, stackup drawings, and notes," and that's just for the fabricators. Contract assembly providers need even more data and information. The problem with this legacy approach is that there are frequently discrepancies between the various files. The netlist file or drill file often does not match the Gerber data because they came from different systems and might not even reflect the correct revision of the design.

Shaughnessy: When there are problems with the fab notes and other data, what is the typical process that the fabricator goes through to resolve these issues? How does that impact the job?

McGoff: When a fabricator sees a discrepancy in the data provided, or if there is incomplete information, they put the job on hold until it can be resolved. The problem is that the deliv-



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ery clock doesn't start until the data package is complete and accepted. That five-day turn is sitting in the starting block waiting for the technical query (TQ) communication channel to do its thing. The CAM engineer notifies the manager of the issue, and the front-end manager notifies the salesperson, who then informs their point of contact at the customer side. Then, that information is conveyed to the designer, and only at this point can the correction and clarification process begin. All of this can easily take several days to resolve, so the designer pays for a five-day turn but gets the boards back in eight days.

It's even more problematic if the fabricator misses a discrepancy in the data package and runs with the erroneous set. This raises a lot of questions, such as, "Which is the go-to file: the Gerber data, the drill file, or the netlist?" Do all your fabricators have the same understanding? Who is responsible for the scrap when that does happen? I believe the larger question should be, "Why would you ever leave the potential for that kind of discrepancy in your process?"

Shaughnessy: How do Mentor's tools help designers provide solid data packages to their fabricators?

McGoff: We understand that a PCB is a product, and we model it as such. The PCB is constructed with specific materials, the features are attributed by purpose, and the manufacturing process to be employed is understood. Properties like build-up layers in the design let the fabricator know the sequential lamination cycles that are needed. Test points are attributed as test points and not merely as another round feature on the Gerber layer. This PCB product model is correct in design, validated in Valor DFM, and sent as a single container to the PCB fabricators.

Shaughnessy: How does ODB++ figure into this equation? Do you have any numbers on potential hours saved per design, etc.?

McGoff: Using ODB++ design data to transfer to fabrication eliminates the disparities found



Patrick McGoff

in legacy data sets. Everything the fabricators need can be found in this single, validated container: the board layers, drill data, and stackup information, for example. The ODB++ design format even supports the information usually found in the drawings, such as a reference to applicable specifications like IPC-6012A or the UL flammability rating.

With all the information the fabricator needs in a single container that has been validated, there is no opportunity for discrepancies, misinterpretations, or delays. One of our customers, Optimum Design Associates, did a study a couple of years ago that showed using DFM and ODB++ can help reduce the TQs from their suppliers by 72%. That's what we call Lean NPI.

Shaughnessy: It seems as if most fabricators are content to fix the bad or missing data, just to be sure they get the job. What do you think could be done to help change this situation?

McGoff: It's an understatement to say that PCB fabrication is a competitive business. These companies are expected to be the lowest bidder on a custom product with zero defects and to deliver as quickly as 24 hours. Because PCBs are often considered a commodity, the fabri-

cators accept that they must be flexible and accommodating in the data they receive. But if, as a design organization, you consider them a truly critical partner in your supply chain, you would ask them what you could do to make the design-to-manufacturing process go smoother. I'd be willing to bet most of them would suggest improving the data exchange package. And why wouldn't you? It helps you develop better products faster. When you have this conversation with your fabricator, make sure you are asking this question of the front-end engineering manager, as they are the ones who can tell you what the real issues are.

Shaughnessy: What advice would you give to new PCB designers regarding the creation of fab notes and other documentation?

McGoff: Don't do anything that is not needed and always look for ways to improve the process. Just because your company has sent the same data package the same way for 30 years and "the system is not broken" doesn't mean it can't be improved. Why create a drill drawing if it is not going to be used? Why use a drawing template with embedded notes that are not applicable to a given design? If you really want to improve your design to the manufacturing process, start a conversation with your fabrication partners.

Shaughnessy: Thanks for your time, Pat.

McGoff: Thank you. It's always a pleasure.
DESIGN007

Sondrel Looking for Electronic Designers to Become Chip Architects

Designing a large complex chip is not simply question of connecting together a set of IP blocks, according to Sondrel. There is considerable creativity required as well.

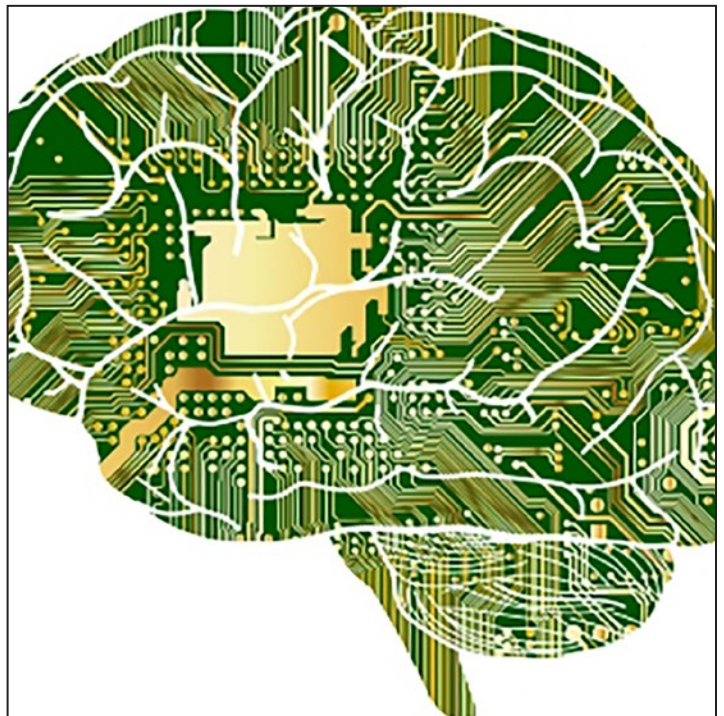
"Just like a great building design needs a great architect, a great chip design needs a great chip architect," explains Graham Curren, Sondrel's CEO and Founder. "Electronic designers are very logical and precise but a chip architect needs to also be creative as well to be able to think of a range of different ways to solve a problem. Being able to use both the left and right halves of the brain is a rare skill in electronic design. We are actively looking for such people to join us as chip architects as they play a fundamental role in the creation of the big complex chip designs that we do."

The real-world process of designing a big chip starts with a customer brief which can range from a simple outline of what is required through to a very detailed specification depending on the experience of the customer. Sondrel has a team of Solutions Architects that meet to discuss the brief in depth with the customer and create a feasibility study, which crystallises the design into a tangible form.

A key part of the possibility cloud of solutions is the continual trade-offs of the best possible techni-

cal solution, which would be unfeasibly expensive, to find the timely, commercially viable solution that achieves the key performance requirements of the project.

(Source: Sondrel)



Things Designers Can't Unsee



Interview by Nolan Johnson I-CONNECT007

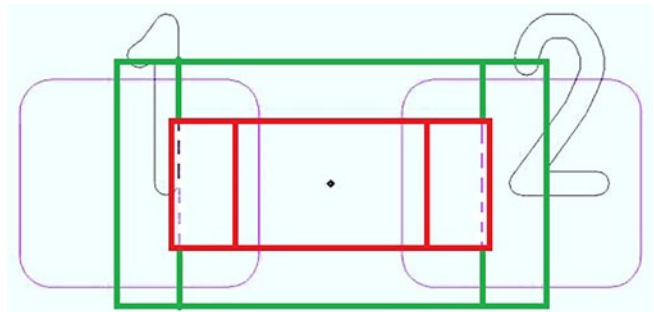
I spoke with Kelly Dack about certain things you can't unsee from a designer's perspective. We cover myths on topics ranging from SMT assembly to the "perfect" 0201 footprint. We delve into design issues relating to board outlines, panelization for production, and the need for enough copper pullback from board edges. We end by discussing the myth that a PCB designer is in the best position to specify material temperature grades and how electronic manufacturing services (EMS) companies must work together with designers to reduce costs.

Myth #1: There Is One Perfect 0201 Chip Component

Nolan Johnson: Kelly, we've been talking about some myths which exist between some design and manufacturing stakeholders that still live on. One myth has to do with the design of some small component footprints, and another affects PCB panelization of the board outlines for assembly. The last affects our perception regarding which PCB process stakeholder is responsible for determining material temperature grade and processing requirements.

And before we started this interview, you said that the idea of a perfect 0201 PCB design library footprint is a myth due to physical part geometry and solder deposition variables and that there is no single geometric answer. Yet, some PCB designers perceive that their job is to come up with a single, "perfect" PCB layout footprint for an 0201. Is this where the myth begins? How do you talk to your design customer about these concerns?

Kelly Dack: This is a very timely topic because designs continue to scale down. We've been talking about reducing fab and assembly sizes for decades, and they continue to shrink. I work for a manufacturing company in a PCB assembly context, and in a design context; we are constantly trying to stay ahead of customer designs utilizing some really challenging footprint strategies for smaller and smaller components.



0201 tolerance range.

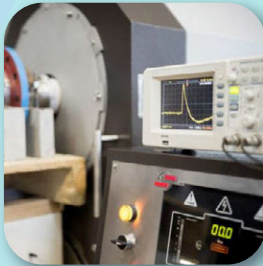


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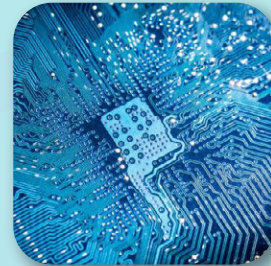
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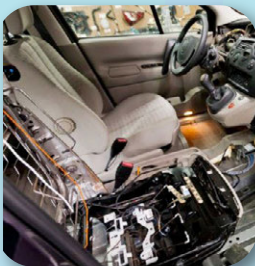
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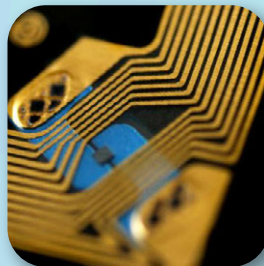
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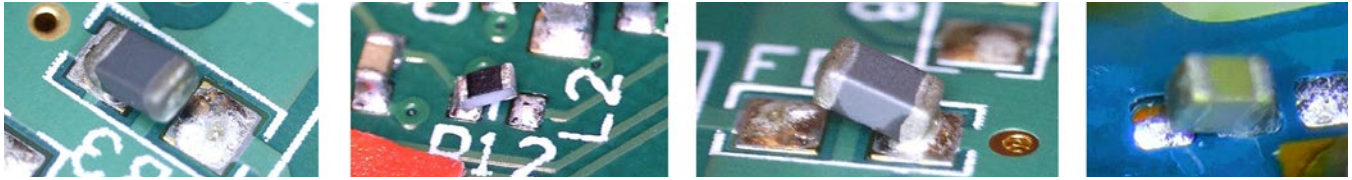
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Some examples of tombstoning.

Let's talk about the perfect 0201 footprint for a moment. I actually searched for "the perfect 0201 footprint" online. I wanted to find out what designers are considering when they mean their component footprint is perfect. As you might imagine, I found dozens of various land sizes, shapes, and land spacing for a generally specified 0201 component package. It seemed that each designer tweaked the numbers to their own idea of "perfection" without defining any of the manufacturing variables. I then analyzed one of our customers' designs, featuring 0201 parts that had been running successfully on our lines for many years. Guess what? The footprint didn't match any of the perfect footprints defined on the internet, but the footprint seemed to work perfectly for us.

Johnson: What was going on here?

Dack: The reason the solder joints were forming perfectly for us on our customer's board assembly was not due to a magical concept of a perfect footprint. Success was achieved because the designer had built in enough allowance for the footprint to be combined with all of the other elements of manufacturing to create the perfect solder joint. The designer's cognizance of component Z height and how it affects the solder fillet is what made this footprint successful (Table 1).

The relationships between the metalized ends of a chip component and the PCB land geometry are not to be underestimated. However, designers must understand that the purpose of stakeholder collaboration is not to yield the perfect footprint. This is a myth. We collaborate to

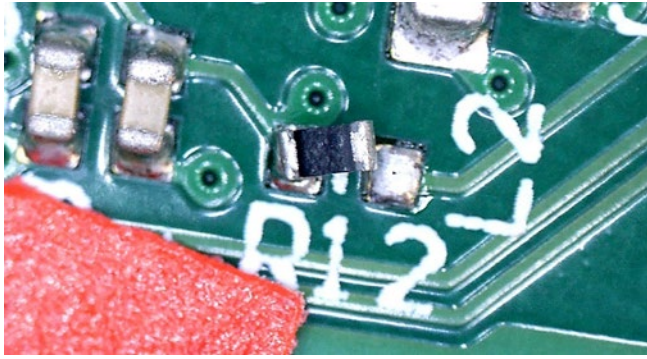
optimize the footprint to work with all of the other manufacturing requirements on the PCB. This allows the assembly stakeholder the best chance of forming perfect solder joints for all the components by manipulation of any of the many other variables.

If we look into the IPC-A-610 acceptability specification, there are clearly documented photographs showing a perfect solder joint. Looking at the perfect solder joint, you'll see that there is the wetting of the solder material after reflow. Evidence of wetting is a key factor, which has allowed the solder to climb up the component height on the metalized end about halfway, creating the perfect solder fillet.

There is a relationship between the extension of the land beyond the component's metalized end and how far the solder fillet will climb up the component. Too short of a toe extension will reduce the fillet size. Too long of a toe extension may lead to too much solder deposition. The solder may climb too far up the component end leading to defects including tombstoning, skewing, or solder ball contamination. As it turns out, a rule of thumb

Stakeholder Responsibilities for Adjusting the Variables to Achieve the Perfect Solder Joint	
Stakeholder	Variables
Design considers only a few footprint variables	Component footprint layout based on component contact geometry and tolerancing
Manufacturing considers solder deposition and elements of a perfect solder joint	Determines the appropriate volume of solder for each SMT component
	Selects the appropriate stencil thickness to account for the range of variables
	Determines solder deposition strategy variables: overprinting, aperture reduction, thickness stepping
	Determines solder type and size
	Determines stencil release quality requirements: laser cutting, etching, electro-forming, and polymer coatings
	Reflow oven profile: panel orientation, conveyor speed, temperatures
	Reflow environment: inert or other, flux considerations

Table 1.



Example of a skewed chip.

may be applied in which the land's toe extension should nominally extend half the component chip or lead height. This concept can serve as a starting point for helping to achieve a perfect solder joint.

Johnson: Would this mean that differing height 0201 chips would need different land geometries?

Dack: You got it! It is very common for small chip resistors to maintain a common Z height or thickness. But chip capacitors, on the other hand, have various heights that—without solder deposition compensation—affect the formation of the solder fillet. This is where the IPC-7351 land pattern calculator comes in handy. With this calculator, a designer can input all of the geometric attributes of a component or lead—including Z height—and the calculator will adjust the land sizing appropriately.

After calculation, some of these geometries could be considered standard or modified, depending on whether they're used in new designs, up-rev'd designs, or legacy designs. We get a lot of customers with legacy designs that were done 5–10 years ago. The fact remains that all of these designs use different land sizes and spacing for their 0201 footprints. But the reason the assembly supplier is still able to solder the parts on is only through adjustment of the other process elements. This is the magic behind the myth of the “perfect” footprint. Regardless of the perfecting of footprint geometry, the challenge has always been put upon the assembly supplier to adjust all of the manufacturing variables to create a perfect solder joint.

Johnson: Are there any more factors that come into play in order for EMS providers to yield perfect solder joints?

Dack: Yes. For instance, in the case of the 0201 package, we see that many customers' designers use the same footprint geometries to attach their 0201 packages onto a PCB design on both top and bottom. Many times, the component density is different on each side. It is very common to see only small chip components on the bottom side of a PCB. This consistency makes selecting a stencil thickness less of a challenge. But if small chip components are installed in the same areas of large power components with massive lands, it sets up a challenge for solder deposition. Larger lands need more solder calculated using different ratios. Therefore, thicker stencils need to be used to get enough solder onto the lands. But a thick stencil will overwhelm a small 0201 component footprint with solder paste. What to do?

Again, the assembly manufacturing engineer's only option after the design is complete is to go back to adjusting manufacturing variables. They have many tricks up their sleeve regarding variables. One trick is to use a thick stencil to satisfy the requirements of the larger parts. But then the manufacturing engineer can specify that the stencil is etched thinner in areas, which must address the smaller components. We can get several stencil thicknesses in one by “stepping” the stencil in a customized way.

Johnson: Unless designers want to redesign after talking to you, they need to take into account the height of the components that they're using. That points them to that IPC calculator. Does an EMS provider's DFM team check the calculations for every component height on a PCB assembly?

Dack: Every EMS provider should be checking this. They all have design review teams. Ideally, an EMS provider would run a base design through a DFM process. The DFM process is two-fold. At the EMS level, we look out for our bare board manufacturers because we're often tasked with procuring the bare board in panel



Kelly Dack

form. We screen the design to make sure that it will be acceptable to our bare board manufacturer so that the line widths and spacings are amenable and relative to the copper thickness. We look for stackup issues and copper topology on each layer.

Then, the land patterns will be audited against the component BOM for feasibility. Each component on the BOM is specified in the X and Y dimensions from the datasheet, as well as the Z direction, so that component footprint topology on the bare board can be audited for solder joint perfection.

Johnson: This sounds like an intensely manual process.

Dack: If done manually, it would be an intensive process. But today's collaborative layout and DFM review software solutions include links to component data. We link to the component databases through component sourcing from the large supply chains like Arrow, Digi-Key, Mouser, and others. They are directly linked so that the layouts are designed with instant component datasheet access and 3D step data, simultaneously, within the DFM review process. This concurrent process allows data to be fed into the auditing portion of the software to check for any showstoppers.

Johnson: You're suggesting that these checks can be done at two different stages. One, as a final check by the designer before the design is released to manufacturing and the other by the manufacturing engineers before the materials are ordered and sent to the manufacturing floors for volume processing.

Dack: These are checks that should be done by the designer before the design ever leaves the originator—our customer—and then again done as an incoming inspection review or design or DFM audit by the EMS provider.

Designers also need to learn from some of the important steps taken by the manufacturers to ensure quality. Tour a bare board manufacturing shop or an EMS provider's assembly shop, and designers would see that every step is measured for compliance after completion. Data is collected, and adjustments are made. The design community continues to need to realize this and implement a design process that checks for acceptability after every step of their design process. This includes checking in with other process stakeholders and setting up a database of design constraints to match those of the manufacturers. It's very important that this myriad of design rules be set up to match the capability of the supplier doing the work.

Johnson: Ultimately, the source information comes from the designer and is then made available to you. Your check on incoming designs should deliver a clean result with zero issues regarding footprint sizing and Z-axis for the component.

Dack: This only happens when there is outstanding communication between the designer and manufacturer before design release. Ideally, the designer is in communication with the manufacturing stakeholder well before the design is released to set up the design constraints in the layout.

Often, we receive designs that have passed with flying colors all of the DRC checks in the layout database, which were set up for manufacturing at a prototype shop that has extremely accurate processes and machinery and access to specialized materials. However, when this board is sent to an EMS provider to be built in volume, this is where we see the designs fall out because our offshore manufacturing stakeholders use different machinery. Or they don't have access to the same materials that the prototype supplier has. As an EMS provider, we use a different set of design rule check criteria than the designer did unless we were given the opportunity to communicate throughout the design cycle.



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Johnson: What's the best way for an EMS provider to communicate a design to their customers?

Dack: Through education. EMS providers must learn to engage with designers through social media outlets and trade publications. Both sides must engage. For example, the mission of the Printed Circuit Engineering Association (PCEA) is to bring the manufacturing suppliers together to discuss and build awareness from all of these perspectives. They are off to a great start in getting this accomplished.

Myth #2: Copper Can Be Flooded Close to the Board Edge—Panelization

Johnson: Speaking of going from prototype to production, another myth concerns board outlines and panelization relative to EMS work. What do you see there?

Dack: Another ongoing, problematic trend we see in manufacturing is a lack of copper imaging pullback from the board edge. We need to get designers to understand that when their design goes to volume, it must be conveyorized—processed on manufacturing assembly lines. To conveyorize a design, certain amounts of clearance must be allowed in the design so that the secondary and tertiary operations of production have room to operate. One thing that's on our hit list in the DFM auditing world is to verify there's enough copper pullback. Copper pullback refers to the distance between the nominal designed board edge and the copper, and whether the copper is flooded, exists as a via or a land, or exists as a trace. Is there enough distance between that copper image and the glass epoxy FR-4, polyimide, or material edge to process?

Ironically, electronics industry forums often recommend the opposite of what the EMS provider needs. The conversations I've read on design forums have asked, "How close can we get this copper to the board edge?" or, "I designed a board and flooded it right to the edge, and it was successful," as if there's a need

to get copper to the board edge. Some newer designers didn't have the depth of knowledge to know where their board was going to be manufactured. By pulling the copper out, or by not leaving enough space between the board edge and the copper, they hurt the depanelization methods for the board.

There are also several breakout methods to be considered in panelization. Individual PCBs can be tab routed, which uses a routing tool to carve a slot around the board. This creates a void between the edge of the panel and the board by leaving tabs or small areas of attachment while retaining the circuit board design. Often, perforations are added to these tabs to allow for breaking the tab and excising the board. If there's not enough space between copper and one of these tabs—especially if it has the perforations or mouse bites at the point of breaking—the tool can leave a frayed edge, which will extend into the copper and damage it; it may expose the copper surface leaving bare metal, which is not considered acceptable with IPC specifications. Insufficient copper clearance at the board edge reduces our ability to utilize mouse bites.

Another depanelizing strategy is V-scoring the board edges using a circular saw tool with a "V" edge that cuts a straight line on the top surface and on the bottom surface, leaving a small web of material in between. As designers, we like to refer to a one-third equation for a V-score. V-score blades come in differing angles. There are narrow 30-degree angles and wide 45-degree angles used for different purposes. However, depending on the depth of the V-score and the width of the angle, designers can get into trouble not pulling back the copper enough because the V-score is going to cut away a certain amount of material on the top and bottom edges of the board, causing more problems.

V-scoring and tab routing are the two main excising methods. There's also laser scoring, which is used a lot more in flex manufacturing. If there's not enough room between the copper and polyimide material, it will cause grave problems for laser excising because of the differences of the materials—copper versus polyimide.

Myth #3: Design Has the Final Say in Material Temperature Rating

Johnson: A third myth concerns materials—specifically, who specifies the glass transition temperature, which will avoid delamination and warping issues.

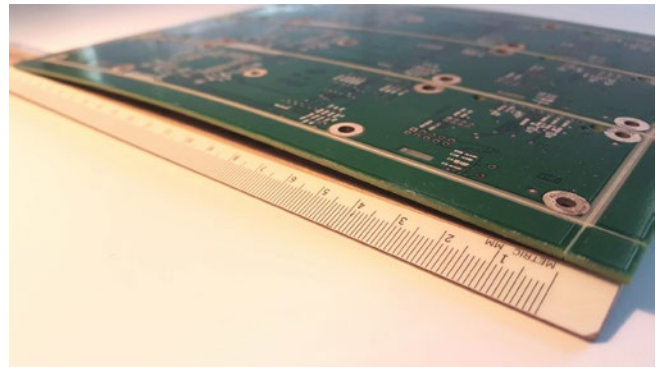
Dack: As an EMS provider, we often see a lack of definition in the designation of high-temp or low-temp materials. It is generally accepted that the best stakeholder to define material temp specification is the PCB designer. But this myth is not necessarily the fault of the designer.

Designers are expected to specify things regarding electrical performance. But it is a mistake to presume PCB designers should be specifying manufacturing processes. There is wisdom in the old saying that designers need to specify what they want in the part, not how to achieve it. Many times, a PCB designer is called upon to design or specify PCB features for which he or she has no idea of where the part will be built or the materials, processing, or capabilities available.

This is another good reason for designers and manufacturers to establish a means of communication prior to beginning the design. We see material on the fab drawing that reads “Material: FR-4.” This specifies a fire-retardant glass epoxy material but is not very specific at all with regard to other important characteristics. When we order the boards, we have to make certain determinations for that board with regard to vulnerability to heat in order to be successful on our processing lines.

In the customer’s best interest, we want the PCB to be the lowest cost possible. We like to use the least expensive material available for pricing reasons; however, this reason can conflict with quality, which is also a priority. When “FR-4” is listed as the only material specification on the bare board, we have to estimate how many thermal cycles the board will go through before it is fully assembled so it will not warp or delaminate.

If overall manufacturing data is limited and we do not have the complete picture, the



Example of a warped board.

boards will be typically quoted with low-temp material not to drive up costs. But that strategy can backfire on us during the manufacturing review, which sometimes occurs after we win the quote. Sometimes, the board may have to go through several additional thermal excursions. In this case, we will determine that we need to pay for the higher temperature material.

The thought process we go through involves asking, “Is the board a single-side two-layer board?” This makes it a candidate for low-temperature material because it’s only going to see one thermal excursion, and it doesn’t have to be flipped over and parts placed on the backside. If the panel warps slightly, it’s insignificant. However, if the board is a two-sided assembly, multilayer, we have to look at the layer stackup and make sure that it’s a balanced layer so that it won’t warp. We may also consider paying more for the materials to prevent warping and delamination during more thermal cycles.

A thermal cycle is a period of time that the board will be exposed to heat, which happens in a reflow oven, rework, and during wave soldering or select wave soldering. Any time this board is being exposed to heat, it can adversely affect the board laminate. For a double-sided, multilayer assembly, we will go with a higher-temp material—150–170°C—which will cost the customer more.

If we go to even more layers and add another process, it may take a single pass to install top-side surface-mount components, a second pass to install the bottom side components, and then a third pass through a wave solder operation to install the through-hole compo-

nents. We have to consider that we may go to a 180°C material, which is a noticeable cost difference in volume. It might only be 20–30 cents more per board, but if you multiply that by one or two million, it can kill a project. We want to expose the customer to expectations early on; the best way to do that is to communicate early on in the design cycle.

Johnson: What needs to be communicated to the designers as they're doing their designs?

Dack: In the design and manufacturing world, I'd like to see more communication and collaboration between the customer, design, and manufacturing. To do that, it goes back to organizations like IPC and the PCEA to foster that. For example, the PCEA is presently collaborating with the SMTA as they both want to incorporate more designer information to their people up front.

Johnson: That helps create more opportunity to have those conversations, but what happens right now? Do you have these conversations with your customers about design rules only after the quote has been received and priced out?

Dack: About 95% of the communication occurs after the design review if it even happens at all. Manufacturers are accustomed to not complaining during DFM reviews, as anything they point out might be considered a capability weakness. Personally, I think it is because they don't want to lose the quote; they want to submit a low price so that they will win the business. Once the quote is won, weeks or months have gone by, and the order starts, that's when the EQs come out, such as, "We can't etch this line using this thickness of copper foil because it's a poor design," or, "We can't plate the specified amount of copper in these holes. Will you accept a lot less?" Those are heavy-hitters.

If we could establish a better audit up front and a more communicative audit of awareness between the customer and manufacturer, we'd waste less time. The problem still exists: Who is supplier management going to buy from?

Supplier management is not technical; they're going to buy from the lowest complainer. That's just a fact of life.

On the assembly side, it's similar. EMS providers would prefer not to complain up front, win the quote, and then talk the customers through the issues, but 95% of the issues are not addressed at the time of build or contract. Hopefully, they'll work through it, and things can be manipulated or adjusted by time of build, but it's typically on the supplier to work through the problems; again, that's just the way it is.

Johnson: What are some things you can't unsee from a designer's perspective?

Dack: You can't unsee this stuff, such as 0201 components that are tombstoned or glass epoxy boards that are warped to high heaven. It's horrible and ugly and is a result of poor design, poor manufacturing capability, or both via poor communication.

For example, when an unbalanced double-sided PCB assembly goes through its first-pass component placement, the stencil screening process, and on to the reflow oven, it goes in totally flat but comes out warped like a potato chip. Now, it must be flipped over for the second pass stenciling, which may or may not work well.

But when it gets to the stage for automated placement of components for the second side, the warpage sets up a resonance on the board. I've seen components placed onto the surface of a PCB that was so warped, the springy condition caused a vibration to set up on the PCB; as the placement heads came into contact with the bouncing PCB surface at the end of the placement process, this caused the components placed at the beginning of the run to bounce off the board like popcorn! It was another crazy anomaly that I'll never unsee.

Johnson: Kelly, thanks for taking the time to speak with me.

Dack: You are very welcome, Nolan. **DESIGN007**



PCB007 Highlights



I-Connect007 Editor's Choice: Five Must-Reads for the Week ▶

Updates on trade shows, conferences, and associations dominated industry news this past week. Some events are returning to a physical venue; others are opting for a virtual version in 2020. Add to that a spate of cross-association cooperative agreements and new programs for career development coming from multiple associations, and you've delivered four of my top five picks.

Shaun Tibbals and Electra Polymer: Finding the Silver Linings in COVID-19 ▶

On July 8, Nolan Johnson spoke with Shaun Tibbals, sales and marketing director for Electra Polymers. Shaun discusses the Electra Polymer's business outlook responses to the ongoing COVID-19 outbreak.

Rogers Corporation's Advanced Connectivity Solutions Business Adds North America Distribution Channel ▶

Rogers Corporation's Advanced Connectivity Solutions (ACS) business announced the introduction of a new distribution channel in North America with the addition of Bonding Source, a Krayden Company, to their sales and service team effective July 6, 2020. ACS provides global customers with market-leading high performance and high-reliability RF material solutions.

The Big Picture: COVID-19 Helps Kill Globalization ▶

Globalization was in trouble even before the pandemic. The decades-long open system of trade that dominated the world economy has been damaged by the financial crisis and—more recently—the Sino-American trade war.

Mehul Davé explains how COVID-19 has added a third-body blow to globalization.

Standard of Excellence: Being a Valuable Customer ▶

We always talk about being a valuable vendor, but what about being a valuable customer? Anaya Vardya shares five guidelines for making sure that you are always your suppliers' most valued customer.

The Plating Forum: Minimizing Signal Transmission Loss in High-Frequency Circuits ▶

All PCB materials have both conduction and dielectric RF signal losses. In this column, George Milad highlights resistive conduction losses by the copper layer used in the board.

North American PCB Industry Sales Up 1.0 Percent in May ▶

IPC announced the May 2020 findings from its North American Printed Circuit Board (PCB) Statistical Program. The book-to-bill ratio stands at 1.10.

Punching Out! Acquiring a Distressed Company ▶

Everyone loves a bargain. Just like buying an old car or a fixer-upper house, you can get a great deal, or sometimes you get what you pay for. Tom Kastner shares some thoughts on acquiring a distressed or underperforming business.

Just Ask Happy: The Future of 3D Printing ▶

We asked for you to send in your questions for Happy Holden, and you took us up on it! The questions you've posed run the gamut, covering technology, the worldwide fab market, and everything in between. Enjoy.

How to **Overcome** Conformal Coating Challenges

Sensible Design

by Phil Kinner, ELECTROLUBE

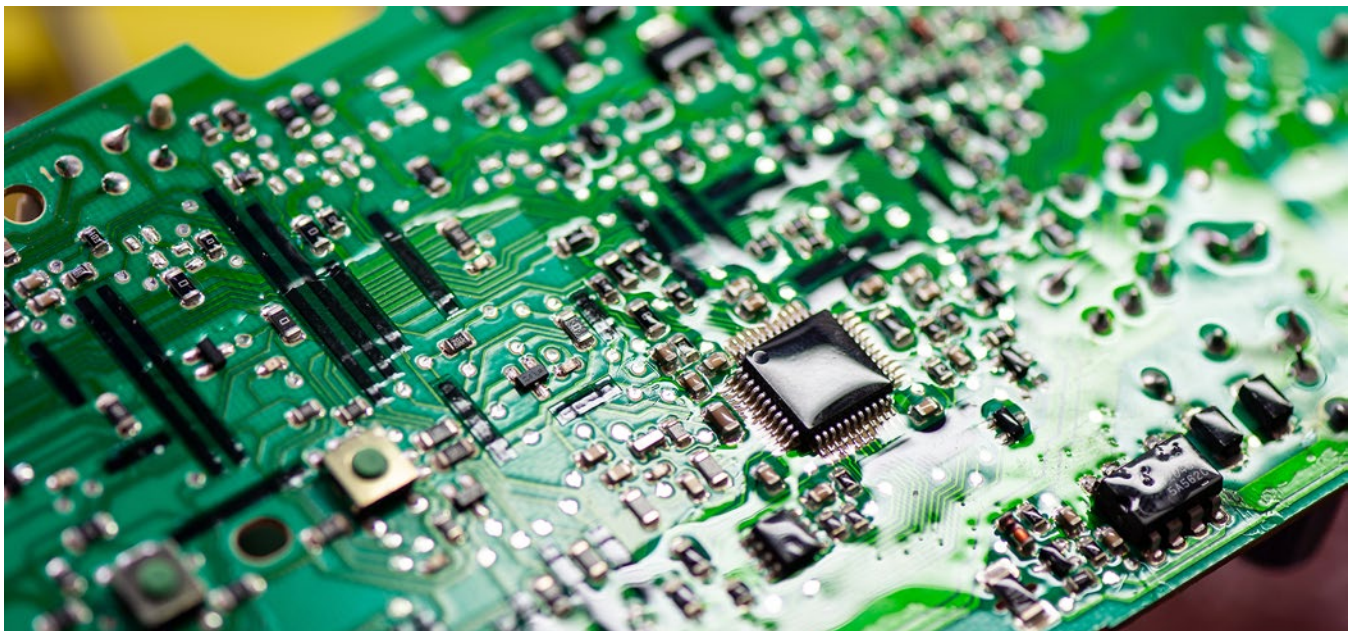
In recent months, I have encouraged readers to take a closer look at conformal coating problems, particularly those that circuit designers could address at the earliest stages of a project. In a [recent column](#), I also offered advice on how to identify some of the potential pitfalls that could sabotage your coating process. In this column, I'm going to look at some issues you are sure to face, from areas of the coated board that simply refuse to cure fully to masking components to the orange peel effect and examining the difference between a critical and a non-critical area of a board.

1. What kills coating quality and cycle time on a typical selective coating line?

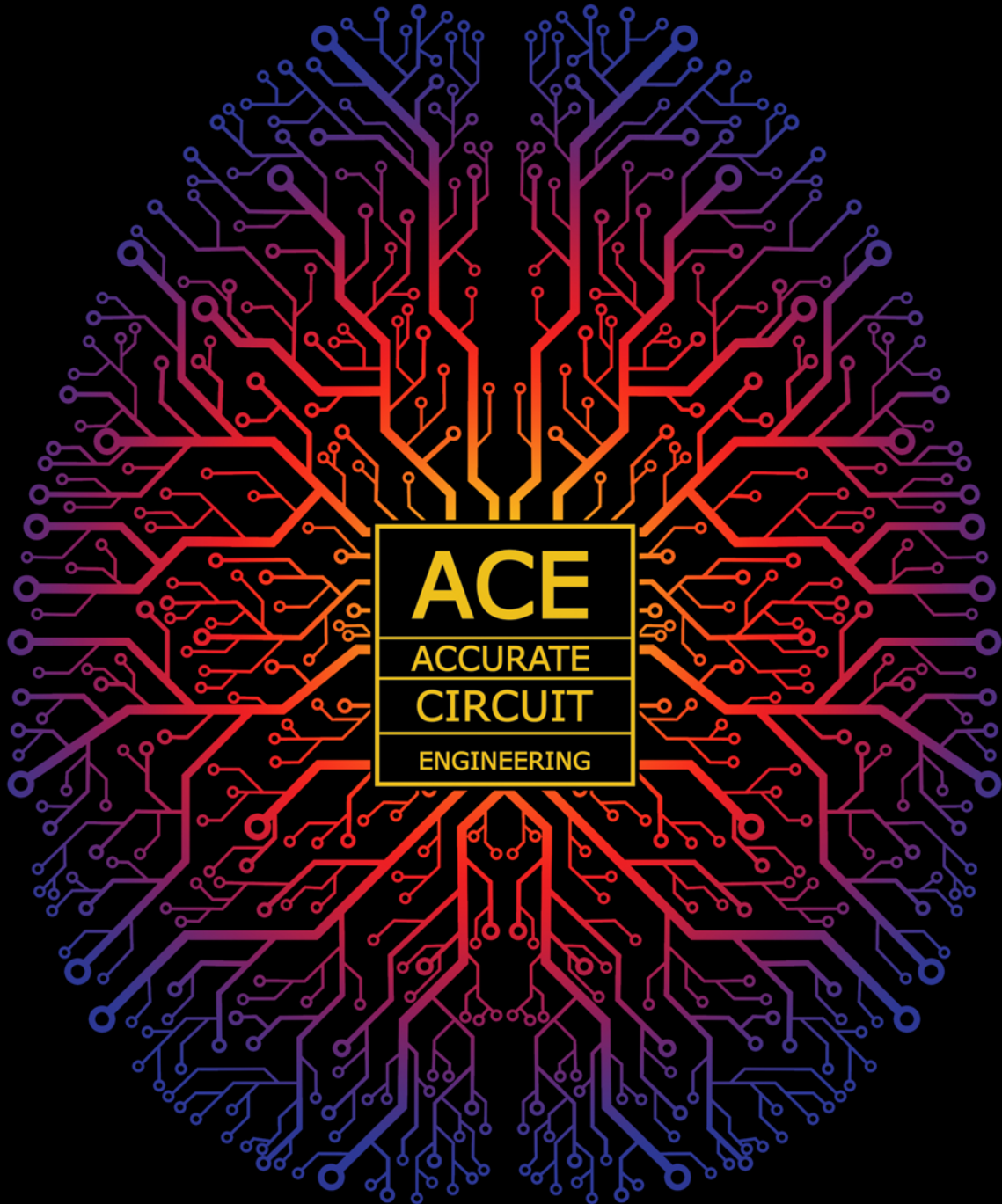
Selective coating machines deposit a stripe of coating material that can be programmed to

stop and start on demand. Stripes of coating can be deposited to create a coating pattern, avoiding areas such as switches, connectors, and test points that must not be coated to prevent interference with form, fit, or function. The coating stripes deposited are usually in the 8–1-mm range for optimum accuracy and minimizing overspray and splashing. When the area to be coated is less than 1 mm in width, then it is necessary to utilise a dispensing step, which is a cycle time killer.

Because of the combination of machine X/Y positional accuracy, material fluid dynamics, and component topography, 2–3 mm is usually as close to keep-out areas as anyone would be comfortable coating for a repeatable process. Must-coat and keep-out areas within 2–3 mm of each other present a problem; again, dispensing will be required—another process step that kills cycle time.



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2. Why would you need to mask some components/areas of the board?

Some areas of the board, such as test points, may need to be masked to avoid the application of coating to enable functional testing after coating. Other areas may need to be masked to prevent obscuring labels—for example, essentially wherever the application of coating is undesirable from a form, fit, or function point of view. In the case of unsealed connectors, switches, etc., the main issue is the coating “wicking” up and coating the connector mating surfaces, thus reducing the contact or potentially insulating the mating surface, preventing either the form, fit, or function of the connector or switch.

3. Can you please explain the “orange peel effect” in more detail? Where does it come from, why does it happen, and can it cause board failure or have other detrimental effects?

Orange peel is a cosmetic defect in which the appearance of the coating surface can appear matted and mottled under the correct lighting conditions, resembling the peel of an orange (hence the name). However, orange peel is poorly understood and often used incorrectly to describe a host of other cosmetic and functional defects.

True orange peel is primarily an issue with coatings that dry by solvent evaporation. During the drying of a solvent-borne coating film, the solvent at the surface evaporates causing differences in temperature, surface tension, solvent concentration, and density within the film. To balance the newly-formed thermodynamic non-equilibrium, currents occur in the coating film. These currents produce eddies in the drying layer, a phenomenon known as the formation of Bénard cells. The surface tension is higher at the edges of the cells than at their centres and coating material flows from regions of lower surface tension to regions of higher surface tension. The resulting unevenness in the surface dries into the coating film.

This produces an irregular surface as the coating shows marked texture resembling the peel of an orange under normal lighting conditions.

Under UV light, however, the coating will normally appear homogenous as long as the thickness is sufficient to cause correct fluorescence. Orange peel is exacerbated in coatings that dry quickly, especially when applied thickly. Since this effect is primarily cosmetic in nature and doesn’t really affect the long-term protection offered by the coating, it has been removed as a defect from various inspection guidelines. Applying the coating in the correct thickness range and replacing very fast-drying solvents in the formulation with slower drying solvents will largely eliminate these issues.

Sometimes, the formation of tiny bubbles of micro-foam in the surface of the coating can cause a matting effect and be confused with orange peel, but these can usually be seen under magnification, especially under UV light and are usually the result of a change in spray pressure or a change in the curing profile. These tiny bubbles can usually be ignored as a cosmetic finish, unless they are bridging conductor spacings or exposing metal surfaces. Any instance where the material does not fluoresce continuously is not orange peel and is likely to be de-wetting due to contamination.

4. What is the difference between a critical and non-critical area of a board?

Typically, during design and development, engineers will evaluate the robustness of their board design and prototypes. They will determine that certain areas of the board (or components) are critical to performance and more susceptible to failure than other areas and will concentrate their coating or protection strategies on these critical areas. These will often be denoted as “must-coat” areas. Areas of the board that must not be coated—including connectors, switches, test points, or any other area that will affect form, fit, or function—will be denoted as “must not coat” areas. The remaining areas will preferably be marked up as “don’t care” areas of the board. This helps simplify the coating of the assembly by focus-

sing on what is most important to the successful coating operation.

5. How is it possible that some areas of a coated board may never cure fully?

There are several reasons why conformal coating in some areas of a coated board may never fully cure, each depending upon the cure chemistry. With water-based materials, for example, a film develops as the water evaporates, but the drying process can take an extremely long time, which can increase exponentially with applied thickness. If the material gets underneath a component and the component is tented with coating material, the material will dry much faster at the component leads and may impede the subsequent drying of the material beneath the component. The evaporating water cannot readily pass through the tent, so there is no kinetic driver for the remainder of the water to evaporate, and the coating will remain conductive.

With UV curable materials, the primary reaction mechanism is initiated by UV radiation of suitable wavelength and intensity. Light only travels in straight lines, and due to the 3D topography of a typical PCB and tendency for material to wick beneath components, there will always be areas that don't see the UV radiation. To overcome this issue, formulators include a secondary cure mechanism, which is usually moisture initiated. The issue is similar to water-based in that very often the coating material will have cured around the component which was exposed to the UV light. If the coating is a good barrier to humidity—which you would hope from a conformal coating—then it can take a very long time for moisture to diffuse through and initiate the secondary curing mechanism. Even if this happens, 50–70% of a typical formulation will not be involved in the moisture reaction and the product “cured” by the secondary mechanism only will have very different properties to the bulk material.

The platinum catalyst used in certain heat-cured silicone materials is very sensitive to the presence of contaminants on the board, which can poison the catalyst and prevent

cure. These contaminants include many amines and halides, flux acids, and other chemicals widely used in electronics assembly. Cleaning, cleanliness, and process control become very important with these types of material.

Conclusion

It's no easy task choosing the correct conformal coating for your product—let alone having the confidence that in applying it, you will have achieved the ultimate goal of protecting your electronics. Conformal coatings are available in many generic types, and each type has its strengths and weaknesses. Choose the right

Conformal coatings are available in many generic types, and each type has its strengths and weaknesses.

coating for your intended use and operational environment, rather than one that is used by your subcontractor or qualified on another product line for a different end-use environment. And, most importantly, be sure to test your design to ensure that it has sufficient robustness for the intended application. Just because a coating has an industry-standard approval doesn't mean it will solve your coating needs. Testing is key to knowing what your material can and can't do.

In my next column, I will look at more coating-related tips. **DESIGN007**



Phil Kinner is the global business and technical director of conformal coatings at Electrolube. To read past columns or contact Kinner, [click here](#). Download your free copy of Electrolube's book, *The Printed Circuit*

Assembler's Guide to... Conformal Coatings for Harsh Environments, and watch the micro webinar series "Coatings Uncoated!"

An Update on the Italian IPC Design Chapter

Design Circuit

by Patrick Crawford, IPC—ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

Recently, I had the opportunity to speak with Pietro Vergine, the chair of the leadership team for the new Italian IPC Design Chapter. Pietro is an MIT who has more than a decade of experience in electronics manufacturing and is the president of Leading Edge, a Milan-based EDA solutions provider that also focuses on design, verification, and analysis at both the IC and PCB level. Pietro is passionate about training and design engineering education, and as part of Advance Rework Technology, Leading Edge has been an active certified IPC training center. Pietro was one of the first volunteers to open a pilot IPC Design chapter.

His combined expertise and drive made him a perfect candidate for leadership within IPC Design, and he accepted an offer to join the Design Community Leadership—IPC Design's panel of industry leaders—in early May. In early July, the Italian IPC Design Chapter opened its virtual doors to affiliations, with designers from all over Italy invited to take part. I spoke with Pietro about the design space in Italy, as well as his plans for the Italian IPC Design Chapter.

Patrick Crawford: Hello, Pietro. Thank you for taking the time to answer some of my ques-

tions. I know that this is a busy—or should I say insane—time for everyone. Let's start off with the big picture. Can you tell me a little bit about what the design landscape looks like in Italy, in general? What industries are most common?

Pietro Vergine: Hi, Patrick. We have big companies as well as a lot of mid- and small-sized companies working in different domains, such

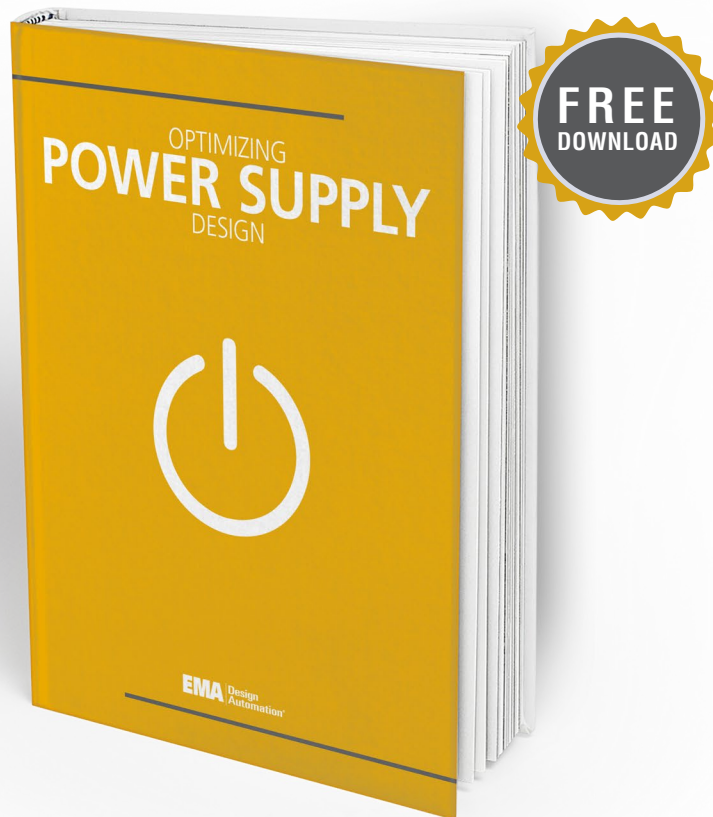
as aerospace, automotive, consumer, and IC manufacturing. There is also military, but that is less than the others. There was—and still is—a tendency for big companies to use design service houses for PCB design. In the past, this was to satisfy the lack of internal designers, and that

is still the case. However, they also do this because they feel that this reduces the cost of the design. This isn't always true, in my opinion.

Crawford: There's definitely an opportunity for smaller design companies to be successful as well as the larger companies; it isn't only locked up in-house with the major players. That's a good segue to my next question. If there are a lot of smaller design houses, then there are



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probably a lot of designers who may not have an equal understanding or access to training across all of them. To that end, in your opinion, what do board designers need across Italy or at least in your area in Milan? What problems might be solved by better cooperation across these smaller companies and designers?

Vergine: If you ask designers in general, they rarely admit to their limits. But I see that there is a lack of knowledge in terms of the flow of design information from the designer to the manufacturer. There are different scenarios. As for the big companies, most of them are fractured into divisions, and who does the schematic is very often not involved in the decisions regarding the PCB. You can imagine what may happen.

Crawford: Absolutely. That's a lot of emails to solve a simple problem if it does get solved before a design is completed.

Vergine: In the case of smaller companies, unless they do very high-end products, they normally rely on what the PCB manufacturer or assembler tells them regarding the materials and assembly processes. In some cases, the designer does not even know the potential issues they may face until they do a functionality test, or worse, it only randomly works. Of course, I am telling you the worst-case scenario. We have excellent designers, and they are usually extreme experts.

Crawford: I understand, and I would hate to generalize an entire nation of board designers. But I also understand that there can be issues with the information flow, and I think that this is common in most markets—not only in Italy. There are technical solutions to this, including standards that streamline how complex information is transmitted within the sup-



Pietro Vergine

ply chain. An example of that would be the IPC-2581 DPMX standard for communicating design-to-fab product information. Speaking of communication, how well does the supply chain play nice? Is there a lot of competition?

Vergine: Because the market is relatively small, competition is very high, and I do not only mean from the competing design services point of view. There is also a bit of competition within the larger companies themselves: “What I know is my power, so why should I share it with you?” Do you see what I mean?

Crawford: I do, and that is definitely not unique to Italy. However, I'm not sure how we can standardize ourselves out of that one. But maybe through education on sound design techniques and methodology that is available to everyone, regardless of their station at their respective job, we can decrease that delta in understanding and make all designers more competitive. During our Design Community Leadership meetings, we have all agreed that this kind of education doesn't necessarily have to be didactic; there are opportunities to enhance your skills through an open forum with other designers, experiential learning, etc. That brings me to the topic of the day—the Italian IPC Design Chapter. How can a cooperative program like IPC Design help designers in Italy?

Vergine: As we only started advertising our chapter a couple of weeks ago, we are still seeing affiliations and have not had the opportunity to meet. However, as I ask people to contact me in order to affiliate, the feedback I am receiving is that this is really a laudable initiative. For the reasons that I mentioned, the designer community is missing the networking and sharing of information to make everyone competitive. Knowledge is power.

Crawford: I couldn't agree more, and that's why I'm so invested in this. I'm really happy to see that you are invested in this, too. Can you share some of your goals for your chapter?

Vergine: Of course. I have a lot of ideas and expectations about the chapter, but I'd like to start working with the affiliates and discover their needs. I realized that what makes a lot of sense to me is not always exactly what others are looking for, or at least they know that they have a specific need but they might not admit it. Personally, I am coming from a place of the electrical design, so for me, the design is the place to start to create culture, methodology, standards, etc. Last but not least, I would like to involve schools and universities, but probably in a way that is different from the STEM programs that work great in the United States but are difficult to implement here. There is a different culture in Italy.

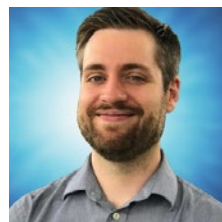
Crawford: Being adaptive to the needs of your area is what we're looking for, so that's great. As to your last point, what works within the United States even varies from state to state and across colleges and universities, so we're constantly trying to adapt to those sub-cultures. I think that the IPC Education Foundation (IPCEF) does a really good job at that, and I am working on integrating IPC Design into those IPCEF student chapters. I think that something similar can work in Italy, where we

adapt even at the university level. Speaking of adapting across cultures, how do you envision the Italian IPC Design Chapter will interface with designers across the world?

Vergine: That is actually something that I hope IPC can implement in cross-linking different chapters. I'd like to create a twinning with other chapters that might have very similar needs to Italian designers. Of course, we don't just "do anything for anything," as we say, and in the end, this also represents a business opportunity for everyone involved.

Crawford: Absolutely. If we make everyone more competitive, then their businesses become more competitive, and hopefully more successful. I hope the same for all involved. With that, I want to thank you for your time and for the insight that you've provided into what's going on in Italy. I really look forward to what we can do and where we're going. Expect another one of these conversations soon. Take care, Pietro.

Vergine: Thank you, Patrick. **DESIGN007**



Patrick Crawford is the manager of design programs and related industry programs at IPC. To read past columns or contact him, [click here](#) or email PatrickCrawford@ipc.org.

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The Digital Layout

by Kelly Dack, CIT, CID+, PCEA

Introduction

This month, I review the virtual PCEA grand opening, which took place on July 14 and featured guest presenter and PCEA educational committee member Rick Hartley. I also check in with the PCEA Education Committee and take a look at the organization's role in education. What do our education committee leaders have in store? I will highlight some of their ideas and plans for learning and curricula in the coming months. Finally, PCEA Chairman Steph Chavez shares his satisfaction with our recent open house.

PCEA Updates

The PCEA virtual open house and webinar was held July 14. PCEA Chairman Steph Chavez had some grateful words to say about our sponsors and the publishers of our columns. He then took an opportunity to state the PCEA's mission statement:

"At our core, our mission statement is to collaborate, inspire, and educate by promoting printed circuit engineering as a profession. Our goal is to encourage, facilitate, and promote the exchange of information and the integration of new

design concepts through communications, seminars, webinars, workshops, and professional development through a network of local and regional PCEA-affiliated chapters."

Steph mentioned that the association serves over 1,000 members worldwide. There are now eight regional chapters in the U.S. and Mexico, and the PCEA is cultivating five new additional chapters, which will be coming online to help serve our members. The organization has quite a few noble objectives by which to meet PCB engineering challenges. Steph laid them out:

"The PCEA is about meeting today's industry challenges from concept, engineering development, standard



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implementation, and manufacturing, including fabrication, assembly, test, compliance, and field service. This knowledge includes details concerning printed circuit board materials, components, manufacturing processes, allowances, and limitations. The final product should have high producibility, reliability, and yield. This should all be confirmed by quality assurance and compliance. The Printed Circuit Engineering Association is structured for these challenges.”

The PCEA's Objectives

The PCEA's objectives include:

1. Stimulating communication among and between printed circuit designers and others in related engineering disciplines.
2. Disseminating information regarding current activities and new developments in design technology via newsletters.
3. Maintaining a communications link between standards bodies related to printed circuit engineering and manufacturing. Coordination includes, but is not limited to, the activities of government, industry, trade associations, and special interest groups.
4. Coordinating the compilation of design standardization issues in printed circuit fabrication and assembly with related design technologies.
5. Encouraging and coordinating the compilation of design information, including equipment, equipment capability (tools and technologies), and related information.
6. Promoting the necessity of early collaboration between engineering, fabrication, assembly, test, and field service.
7. Assisting in the participation of suppliers and OEMs in chapter programs.

Steph thanked the audience and our sponsors before Rick Hartley was introduced, including

instructions for submitting questions and how to participate in online polling throughout the webinar.

Rick Hartley's Webinar Presentation

I've been to many presentations by Rick Hartley. Over the years, I've attended multi-hour presentations, half-day presentations, and full-day presentations. Regardless of the length of

the presentation or the venue, I always enjoy the points Rick makes and the way he makes them. Hartley's emphasis on subject matter runs in a scale of magnitude from simple and personal to flat-out, in-your-face tangible.

The one-hour webinar hosted by the PCEA featured Rick's topic, "Power Distribution Tips to Control SI, EMI, and Noise," did not disappoint. Rick is a master of making strikingly good points while explaining anything related to electronic performance on PCBs. I hope that all of our readers had the time to tune in. In case you didn't, here are a few excerpts from the presentation.

Regarding energy in a PCB, Rick said, "Energy in a circuit is not in the voltage or the current. Energy is in the electric and magnetic fields." He continued, "Energy does not travel in the copper elements, such as traces and planes. Energy travels in the space between these copper elements."

Rick went on to discuss many tips for SI and EMI control. He emphasized the importance of keeping inductance low and offered a few considerations for placement of vias in relationship to the positive and negative ends of a decoupling capacitor. When designing for high-speed signal integrity, Rick explained the "mounted inductance" of capacitors. He showed how to lower inductance by adding a pair of vias to each end of the caps and explained the best



Rick Hartley

arrangement of the vias. Rick moved onto a discussion of the importance of closely-spaced power planes and the challenges to performance wrought by two-, four-, six-, and higher layer-count stackups, which fail to provide copper shaped and positioned to address lowering inductance and improving impedance performance.

There was an obvious air of excitement among the viewers as Rick's presentation progressed. The more he presented, the more our web-host received queries regarding variables within which to apply the concepts. Polling showed that 78% of the audience had 11 or more years in the industry and were hungry for answers to questions they posed: "What about via-in-pad?" "Is it better to have lots of same-value caps or multiple-value caps?" "What is the best tool to simulate a power distribution network (PDN)?" Though the presentation was set for an hour, presenter Rick stayed on long after to answer the many questions that were posed.

Many thanks to Rick Hartley and our audience of viewers for making this educational experience a success!

Next Month: Interview With the PCEA Educational Committee

Recently, I had an opportunity to meet with our PCEA Educational Committee regarding their plans for the future. The educational committee consists of PCEA executive staff members Mike Creeden, Tara Dunn, Gary Ferrari, Rick Hartley, Susy Webb, and Steph Chavez.

This team has a lot of power-packed ideas and curricula lined up for our members. Our new website is also being sprinkled with many informational links and resources. I look forward to my informative meeting discussion with this dynamic group of printed circuit engineering veterans. Stay tuned!

Message From the Chairman by Stephen Chavez, MIT, CID+

Success! The PCEA has truly hit the ground running. We have now hosted two outstanding global events.

The first event was a great webinar that PCEA hosted in partnership with SMTA on July 9 titled "Creating the Best Data Package." I want to personally thank SMTA for acknowledging PCEA and seeing the value that PCEA brings to the industry as a professional industry association. SMTA's eagerness to collaborate with PCEA showed in how professional, seamless, and positive the event turned out. We received awesome positive feedback from an international audience.

The second outstanding global event was PCEA's virtual grand opening on July 14, which featured a presentation on PDNs by Rick Hartley. We had a great turn out with lots of positive engagement and attendee feedback. Rick's presentation was just a small golden nugget of what PCEA has to offer to the industry. It was a successful launch with lots of knowledge-hungry attendees seeking advice and industry best practice information. The feedback from our grand opening has been overwhelmingly positive.

That's two awesome events now under our belt, and there will be many more to follow. Stay tuned for more activities coming your way now that PCEA is official and extremely active. Our official website has been up and running since June 1 with a lot of activity and new members joining the PCEA collective, and we continue to gain industry sponsorship.

Lastly, I'd like to give a very heartfelt and loud shout of "kudos" to the entire PCEA leadership team for successfully launching the PCEA to the world. All the hard work and extra effort have paid off in bringing PCEA from concept to reality. If you have not yet joined the PCEA collective, I highly encourage you to do so by visiting our [website](#) and becoming a PCEA member.

I continue to wish everyone and their families to be healthy and safe.



Stephen Chavez

Upcoming Events

- August 11-13, 2020:
CadenceLIVE Americas 2020—Virtual
 - August 20, 2020:
SMTA/PCEA Webinar “Avoiding the Most Common PCB Failures Modes” by Mike Creeden
 - September 7-11, 2020:
PCB West—Virtual
 - September 16-17, 2020:
Del Mar Electronics & Manufacturing Show (San Diego, California)
 - September 28 -October 23, 2020:
SMTA International—Virtual
 - October 6-8, 2020:
AltiumLive North America—Virtual
 - October 20-22, 2020:
AltiumLive Europe—Virtual
-
- January 23-28, 2021:
IPC APEX EXPO (San Diego, California)
 - January 26-28, 2021:
DesignCon (Santa Clara, California)
 - May 11-13, 2021:
IPC High-Reliability Forum 2021 (Baltimore, Maryland)
 - November 10, 2021:
PCB Carolina (Raleigh, North Carolina)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Conclusion

No matter where you may find yourself in this worldwide network of PCB engineering professionals, your trajectories for success will vector about your ability to learn and apply knowledge. I encourage you to “lock on” to the PCEA as a valuable resource for your future missions. If your aim is to learn and engage, our aim is to serve and assist. See you next month or sooner! **DESIGN007**



Kelly Dack, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). To read past columns or contact Dack, [click here](#).

Tianma Orders Kateeva Yieldjet Inkjet Printing System for OLED Display R&D

Kateeva reports that Tianma Microelectronics Co., Ltd. has ordered a YIELDjet EXPLORE inkjet printing system to expand its research and development (R&D) programs for next-generation OLED displays. The new system, which is built for 200mm glass substrates, will be used to develop devices and materials for various new mobile device applications. The tool will be shipped to the customer's Shanghai facility later this year. The installation will bring the number of Kateeva printers at customer sites to 60.

Kateeva developed the YIELDjet EXPLORE tool at its Silicon Valley innovation center to give display leaders a proven system to develop new OLED devices, evaluate advanced materi-

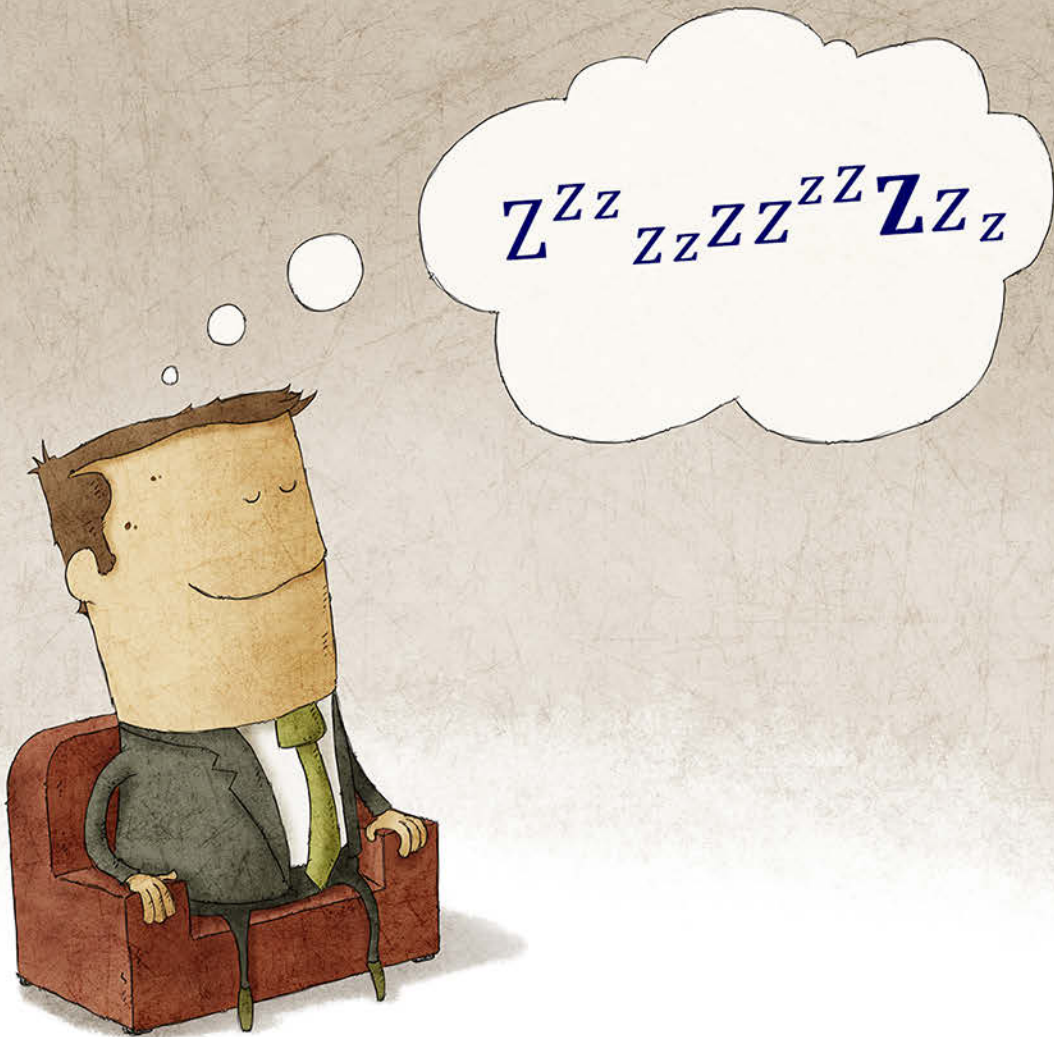
als, and pilot new processes. The first product to emerge from the platform was the YIELDjet FLEX system. Today, the vast majority of high-end mobile phones feature displays that are produced by Kateeva tools.

“Tianma is known for integrating industry-leading technologies into their mass-production lines as they relentlessly innovate new displays,” said Kateeva CEO May Su. “The EXPLORE system lets them stretch their innovation aspirations and evaluate the myriad ways their future OLED mass-production processes can benefit from a proven inkjet deposition solution. We’re proud that our technology continues to enable their roadmap.”

(Source: Globe Newswire)



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Utilizing mmWave Technology to Optimize High-Speed Designs

Lightning Speed Laminates
by John Coonrod, ROGERS CORPORATION

For the past several years, I have been working with many different millimeter-wave (mmWave) applications. I have also been working more with high-speed digital (HSD) applications, and when looking at some of the data, I had become somewhat frustrated. Sometimes, the insertion loss curves generated for HSD applications have a tremendous amount of noise, and the few times I investigated, I found the testing results had poor return loss, and the HSD engineer was not concerned. From my mmWave background, that really disturbed me because return loss is one of the critical properties for obtaining valid data. However, as I have learned more about HSD, I find the technology is commonly focused on the time domain—and return loss has much less influence on most time-domain performance issues. With my learning curve improving for HSD—and more specifically,

very high-speed digital (vHSD)—I now see a lot of areas where understanding the tricks of mmWave technology could help improve design and performance for vHSD technology.

Impedance transitions for mmWave are extremely important to characterize, and this is typically done to get the best return loss behavior for the circuit. Just as a quick side note and clarification, return loss is also sometimes called reflected loss and refers to how much energy is reflected from a propagation medium. For example, the transition from the connector to the circuit usually has an impedance anomaly. If that is not well characterized, much of the energy that would be desired to be inserted on the circuit will get reflected back to the source due to poor return loss (reflected loss). In this case, the poor return loss is probably due to the impedance transition between the connector and the circuit, and that transi-



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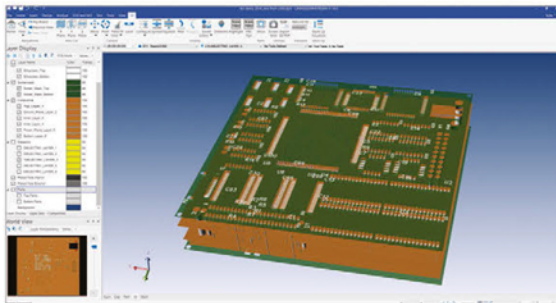
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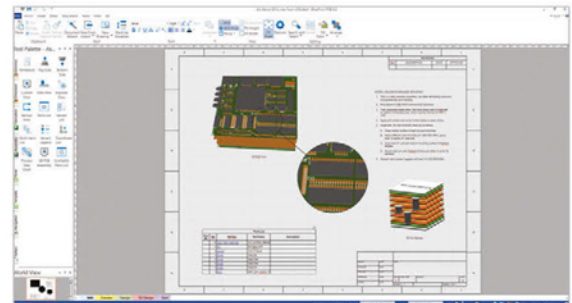
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tion not being optimized. If the testing system knows how much energy is sent to the circuit and how much energy exits the circuit, it will assume the losses (insertion loss) are due to the circuit only. But if the return loss is poor, then much of the insertion loss is not due to the loss of the circuit but is actually due to the reflected energy that was never resident on the circuit. The insertion loss measurements of the circuit are not accurate with poor return loss.

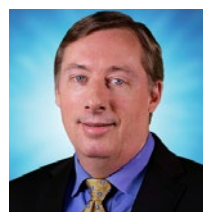
For time-domain aspects of HSD, impedance transitions may or may not be an issue, depending on the digital rate, rise time, and the sensitivity of the circuit. For a circuit operating with relatively slow rise time, impedance transitions have much less impact on the performance of the digital circuit. However, when the rise time is much faster, the circuit is more sensitive to small anomalies often associated with impedance transitions; then, the HSD performance of the circuit could be negatively impacted.

The digital rate (speed) and rise time are related to analog or RF wave properties. The simple square-wave of an HSD clock signal is generated by summing an RF wave and its upper harmonic waves to create the square wave. That means for a slow digital speed, the RF waves used are relatively low frequency. For example, a digital rate of 1 Gbps has a fundamental frequency of 0.5 GHz, and the next several harmonic waves will be at 1.5 GHz, 2.5 GHz, and 3.5 GHz. At those frequencies, return loss is typically insignificant for most

PCB applications. Additionally, the impedance anomalies associated with impedance transitions for frequencies and digital rates that low, are typically not a concern.

However, for a vHSD application running at 28 Gbps, it will use waves at 14 GHz, 42 GHz, and 70 GHz. At 42 GHz, return loss and the associated impedance transitions are very important, and at 70 GHz, these concerns are critical for mmWave applications. These RF issues can have an impact on the eye-diagrams for vHSD, but from limited experimentation, the effects have not been as dramatic as I would have expected. However, for a sensitive vHSD system running at this speed, the return loss and impedance transitions should be considered. The effect of return loss and impedance transition may make a difference for eye-diagram performance in higher-speed vHSD circuits, which operate at 56 Gbps.

Understanding mmWave issues in more detail is highly recommended for the designers of vHSD applications. There are several places where more information can be found for mmWave technology online, including many resources to learn more about the practical aspects of mmWave technology. **DESIGN007**



John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, [click here](#).

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MilAero007 Highlights



Defense Speak Interpreted: DMEA ►

A June 17 article announced a supply chain award of \$10.7 billion to eight defense companies for semiconductors. Dennis Fritz explains how the Defense Microelectronics Agency (DMEA) administers this contract and keeps the technology secure.

Understanding MIL-PRF-31032, Part 1 ►

Over the course of this series, Anaya Vardya will discuss topics such as MIL-PRF-31032 requirements, the quality plan, responsibilities of the Technical Review Board (TRB), and the testing and reporting requirements for the certified shop into the DLA.

Cyberattack! Think It Couldn't Happen To You? Think Again! ►

Eric Cormier and Dave Ryder of Prototron address the ransomware attack that locked them out of their system last December, bringing business to a screeching halt and forcing them into the arduous process of a full rebuild. With things finally starting to normalize, Eric and Dave now offer precautionary advice they've accumulated over the past six months.

Lockheed Martin Chooses Austin American Technology for Cleaning Needs ►

Austin American Technology announced its newest machine sale to Lockheed Martin, which purchased an X30-A Vertical Format Batch Cleaning System.

Sparton Corporation Sells Its Manufacturing & Design Services Business to One Equity Partners ►

Sparton Corporation, a provider of engineered products for the defense industry, entered into a definitive agreement to sell its contract man-

ufacturing unit, Manufacturing & Design Services, to One Equity Partners, a middle-market private equity firm.

Book Excerpt: Thermal Management With Insulated Metal Substrates, Part 3 ►

The following is an excerpt from Chapter 3 of *The Printed Circuit Designer's Guide to... Thermal Management With Insulated Metal Substrates* written by Ventec International Group's Didier Mauve and Ian Mayoh. In this free eBook, the authors provide PCB designers with the essential information required to understand the thermal, electrical, and mechanical characteristics of insulated metal substrate laminates.

IPC: Shawn DuBravac and Chris Mitchell on USMCA ►

On July 1, 2020, the USMCA trade act (United States-Mexico-Canada Act) phased in as a trade agreement guiding economic trade and growth in North America. Nolan Johnson spoke with both Shawn DuBravac, IPC's chief economist, and Chris Mitchell, IPC's vice president of global government affairs and an *I-Connect007* columnist, about the impact of USMCA on North American electronics manufacturing.

Synopsys Awarded DARPA Contract for Automatic Implementation of Secure Silicon Program ►

Synopsys Inc. announced that the Defense Advanced Research Projects Agency (DARPA) selected Synopsys as a prime contractor for the Automatic Implementation of Secure Silicon (AISS) program. The program's goal is to automate the inclusion of scalable hardware security mechanisms in IP and system-on-chips (SoCs) to explore security versus other design trade-offs.

The Black **Magic** in the Business

Flex Talk

by Tara Dunn, OMNI PCB

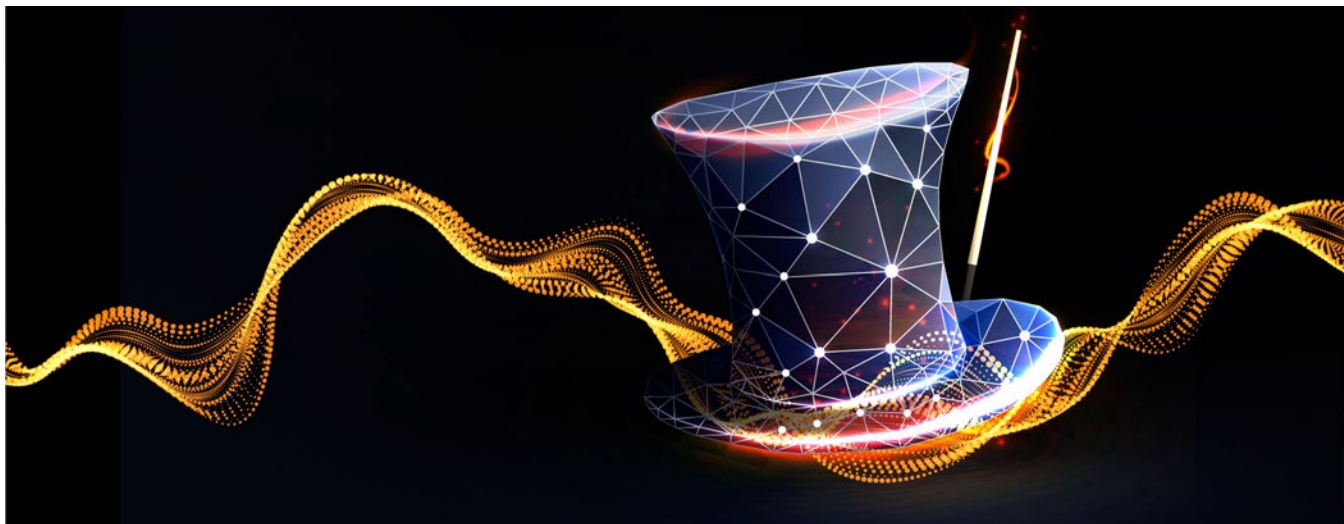
“For rigid boards, I really don’t need a drawing and can get the fabrication vendor where they’re going based on material and a starting point. But flex is different, often called ‘black magic’ in the business.”

Before giving a presentation on flex and rigid-flex a couple of years ago, I reached out to several designers who I knew were experienced in flex design and asked for their best tips I could pass along to those brand new to flex and rigid-flex design. Apparently, I have some generous friends in the industry because I received excellent advice to pass along. The introductory quote above is one that I always remember and often use when speaking about flex. On the surface, it makes me laugh, but I understand what they were saying. When you work with flex or rigid-flex, the communica-

tion between designer and fabricator needs to be impeccable, and the primary method of transferring information is through the fabrication notes.

There are many resources available that provide a checklist of items these fab notes must include, including materials, IPC quality standards, tolerances, critical dimensions, UL requirements, via plugging requirements, and special quality requirements, just to name a few. Today, I will give a recommendation that, although not strictly required by the fabricator to build the product, will certainly benefit the end-user.

When creating the fab notes, include a picture of how the flex is going to be bent, folded, or flexed during end-use. This information, if included in the data package, is more likely



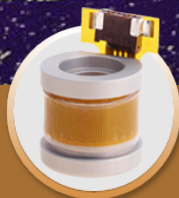
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to be included in the assembly drawings, but those drawings rarely get passed along to the bare board fabricator. Most often, although the flexible circuit is intended for three dimensions, the data files and information the fabricator receives is two-dimensional. Including the end-use requirements in the data package, and then taking the extra step of asking your fabricator to review the design for any recommendations to improve flexibility and reliability, is a simple combination that can yield great benefits. Who better than the fabricator, building flexible materials day in and out, to provide recommendations on product performance?

Who better than the fabricator, building flexible materials day in and out, to provide recommendations on product performance?

There are many subtle ways to improve flexibility and reliability. From a fabrication standpoint, the way parts are oriented on the production panel can improve flexibility. The rolled annealed copper on flexible laminates has a grain direction; orienting the circuit so that the bend areas are aligned with the grain direction can impact flexibility. Another fabrication tool used to improve flexibility is the decision to button or pattern plate. Some fabricators elect to use a panel plating process as a default, while others choose button plating as their standard. When panel plating, the entire panel is plating with electrodeposited copper. This electrodeposited copper is not as flexible as rolled annealed copper on the flexible laminates. Button plating, on the other hand, plates only the pads and through-holes, leaving the circuitry to be formed on the rolled annealed copper. If this is a concern, adding a note to the fab drawing will ensure the button plating process is used.

It is common practice to include the materials stackup in the fabrication notes, and we also encourage designers to use the IPC materials slash sheets when calling out materials. The overall thickness is important in rigid board design but takes on even more significance with flex and rigid-flex design. IPC-2223 provides guidelines for minimum bend radius. Again, your fabricator is another excellent resource when there are concerns about flexibility. Once your fabricator understands how the circuit is designed for end-use, they can offer insights based on their years of experience. One tip to improve flexibility is to use “un-bonded” layers to reduce the overall thickness. This simple adjustment significantly improves flexibility and prevents the dreaded “flex that doesn’t flex” experience.

Another recommendation may be using crosshatch shielding rather than solid copper shielding. This is often a balance of electrical and mechanical requirements, and the crosshatch pattern is highly customizable. For example, if solid copper shielding is required, but there are concerns in the bend area, the crosshatch pattern can be created in just the bend area, leaving areas that are not flexing as a solid copper shield. Removing more or less copper in those regions or layers has a significant impact on flexibility.

These are just a few of the ways that your flexible circuit fabricator can provide guidance and suggestions to improve the flexibility of the circuit in end-use. Communicating those requirements in the data package and working with your fabricator during the design process is simple and can have a significant impact on the successful outcome of the design. While I don’t really think that flexible circuit design is black magic, I do think there are tips and tricks that, learned over time, can greatly affect the performance of flexible circuits in end-use. **FLEX007**



Tara Dunn is the president of Omni PCB, a manufacturer’s rep firm specializing in the PCB industry. To read past columns or contact Dunn, [click here](#).



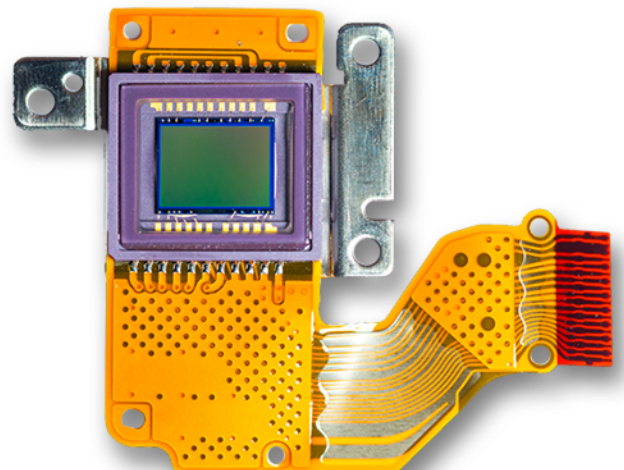
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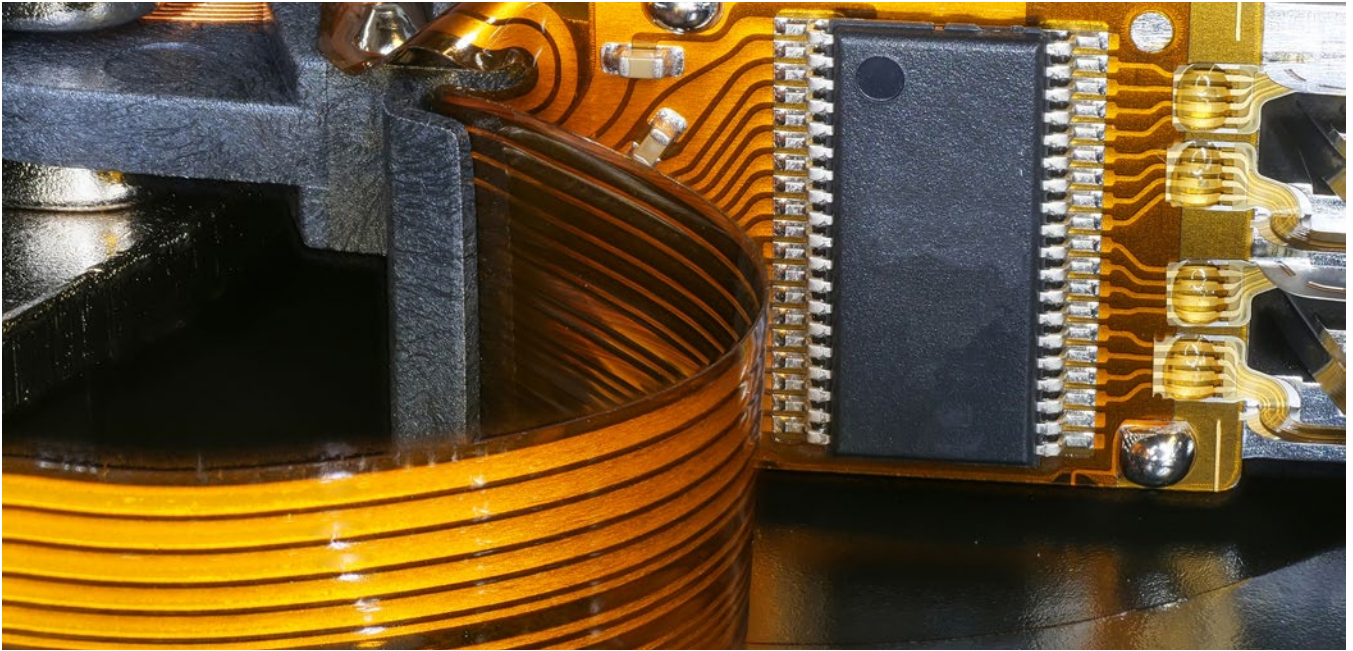
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Flexible Circuit **Design Rules** for Beginners

**Flex Feature by Olga Scheglov, CID, CID+
EPTAC CORPORATION**

Have you ever designed a flexible printed circuit (FPC)? Many seasoned PCB layout designers and electrical engineers have never designed a flex or rigid-flex circuit (Figure 1).

The purpose of this article is to raise awareness about possible FPC construction, essential FPC layout requirements, restrictions, and limitations induced by FPC stack-up materials, while highlighting the importance of communication with the flex fabrication and assembly providers.

FPCs offer advantages that rigid PCBs and round wiring cables cannot provide: flexibil-

ity, weight and volume reduction, reduced production cost, uniform electrical properties, and the ability to be used in dynamic applications where parts of the product must move constantly. They can also be bent, folded, and fit into a 3-D space.

Each FPC manufacturer has different equipment, capabilities, and personnel; each has different FPC layout requirements that the flex designer should understand. Sometimes, the flex designer may conduct an on-site vendor assessment.

Communication between the FPC designer, fabricator and assembly provider is key in the success of the final product. Design of the flex printed circuits shall be done in respect to the fabrication rules of this specific fabricator. This aspect will minimize the list of production technical questions and the time spent for clarification, compromises and consequences caused by pushing production limits.

This list of technical questions regarding problems found in the design during DFM review is known as a TQ. These problems may compromise the level of producibility and consequently the reliability of the product. The same FPC design for different vendors could be



Figure 1: Flexible printed circuits.

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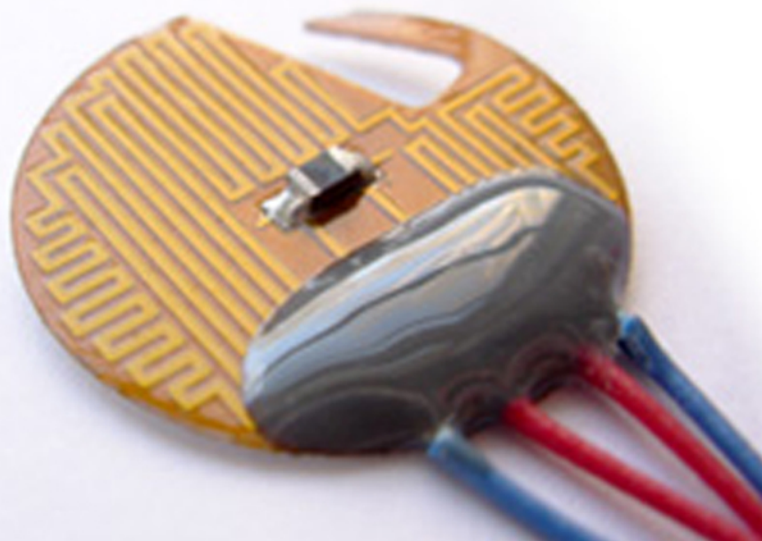
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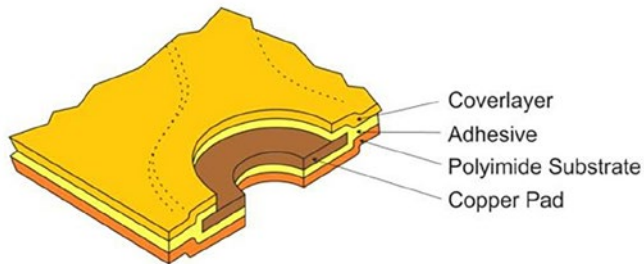


Figure 2: Type 1 single-sided adhesive substrate.

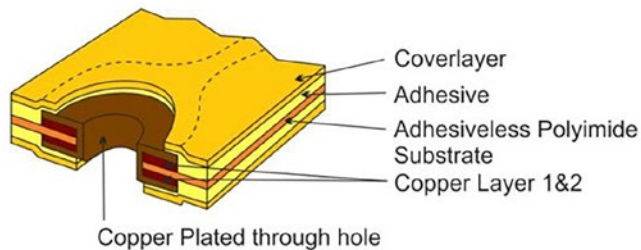


Figure 3: Type 2 double-sided adhesiveless substrate.

a standard, or an advanced and unachievable design because of their capabilities. And this illustrates the importance of knowing vendor capability in advance.

Production capabilities change with technological progress and the sophistication of production equipment. As a result, production design rules will be updated accordingly. Starting layout, the FPC designer should be familiar with IPC standards—such as IPC-2223, IPC-2221, IPC-2222—and be aware of the product class and the type of FPC. According to IPC-2223, there are five types of FPC constructions for adhesive substrates and the same five types for adhesiveless substrate. Figure 2 shows examples of Type 1 adhesive substrates and Figure 3 shows Type 2 adhesiveless substrates.

The flex designer should be aware of the final assembly requirements. Connections between rigid and flex circuits can be achieved with B2B connectors, ZIF connectors, anisotropic conductive film (ACF) or paste, and hot bar soldering (Figure 4). Each of these techniques requires a different size and shape of the terminations in the layout.

The choice of flex materials and the stackup depends on the budget, application, and mechanical restrictions. Since long ago, the most popular flex laminate material has been

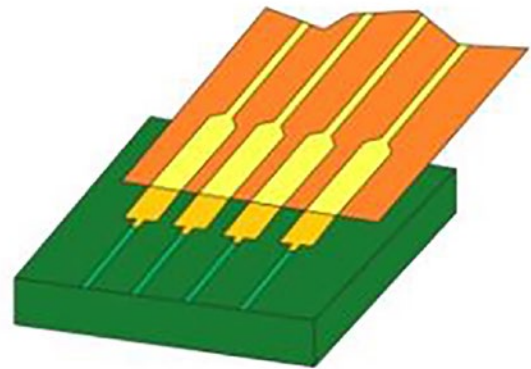


Figure 4: A hot bar connection.

polyimide. Polyester films are popular for inexpensive constructions. In addition to these widely used plastic materials, liquid crystal polymer (LCP) and polyethylene naphthalate (PEN) substrates are also utilized.

FPC design procedure has these general rules regardless of application, type, and the vendor's level of sophistication:

1. All FPC corners must be rounded.
2. All traces' corners must be rounded.
3. All vias, plated through-holes, and SMT pad connections to traces must have teardrops/fillets.

In addition to these three rules, it's good practice to make the SMT pads oval or round in shape. It is also possible to round corners of larger SMT pads (Figure 5).

Since copper adds rigidity to the construction, the designer shall route traces in a staggered manner on the adjacent layers and avoid copper planes, a technique which eliminates the "I-beam effect" and increases the FPC's reliability.

Decreasing the rigidity of a flex circuit's button copper plating also reduces the amount of copper. Button plating is a production process that selectively deposits copper onto the pads and consequently barrels of vias and plated through-holes, and it requires additional work with Gerber files.

The other method of flex copper plating is panel plating. During panel plating, copper is deposited on the entire copper pattern of the external layers and TH barrels. Flexibility can be increased by using crosshatched copper rather than solid copper planes.

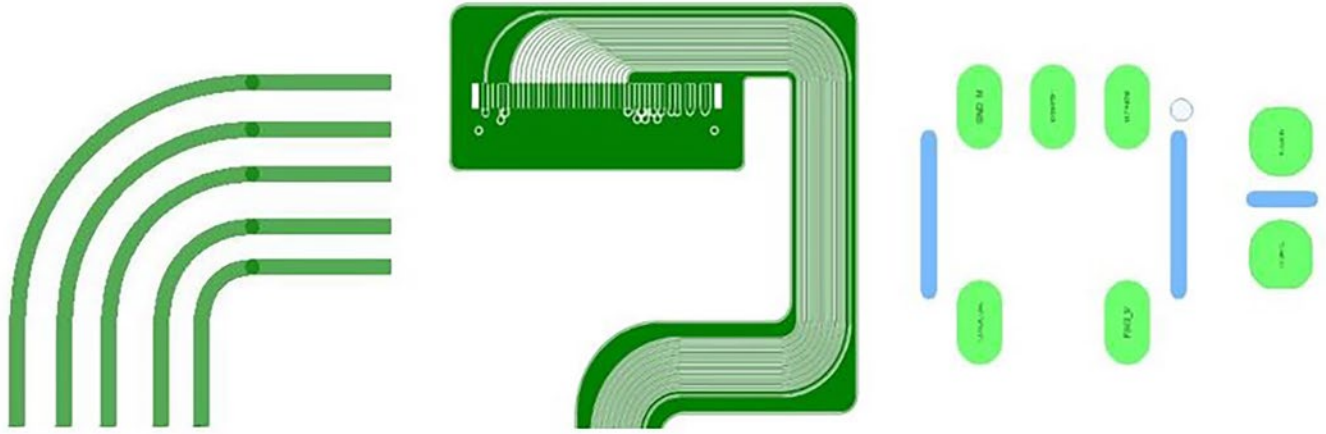


Figure 5: From left to right: A trace with rounded corners, an FPC profile showing rounded corners, and SMT pads with oval and rounded corner pads.

Copper features' spacing to the edge of the flex circuit is a very important parameter which varies with each fab vendor, depending on their capabilities. As an example, some production rules require 0.2 mm (8 mil) clearance from the FPC edge to copper traces, planes, and SMT pads. Via-to-edge clearance requires more separation; I recommend 0.45 mm (18 mil).

A beginning FPC designer may use a solder mask as a cover layer instead of coverlays. Solder mask is a very thin layer; however, it will turn a flex circuit into a rigid spring. Here is another reason why communication with FPC production is very important.

FPC stackups usually have dielectric coverlayers. The coverlay's purpose is to seal in and protect the FPC's copper pattern. Since coverlay is a relatively thick material, all clearances to other features will be larger than if solder mask is applied. Therefore, a beginner FPC designer should learn all about the restrictions and limitations of coverlay applications provided by the FPC manufacturer. It is important to understand coverlay materials and methods that FPC production applies when creating access openings for component pads (drilling, punching, etc.). Common production capabilities require the coverlay's web to be at a minimum distance of 0.25 mm (10 mils) and 0.3 mm (12 mils) between any opening in coverlay to the FPC outline. Fine-pitch components will get a gang opening in a coverlay.

Due to the fragile nature of flexible circuits, in FPC layout, the designer should always address the problem of a potential material tear. Figure 6 shows possible techniques for flex tear relief: slots, slots, holes, corner tabs.

Connector areas and heavy components assembled on FPCs require stiffeners. Some areas rich with components may also consider having a stiffener underneath. Stiffener material can be polyimide, FR-4, or stainless steel.

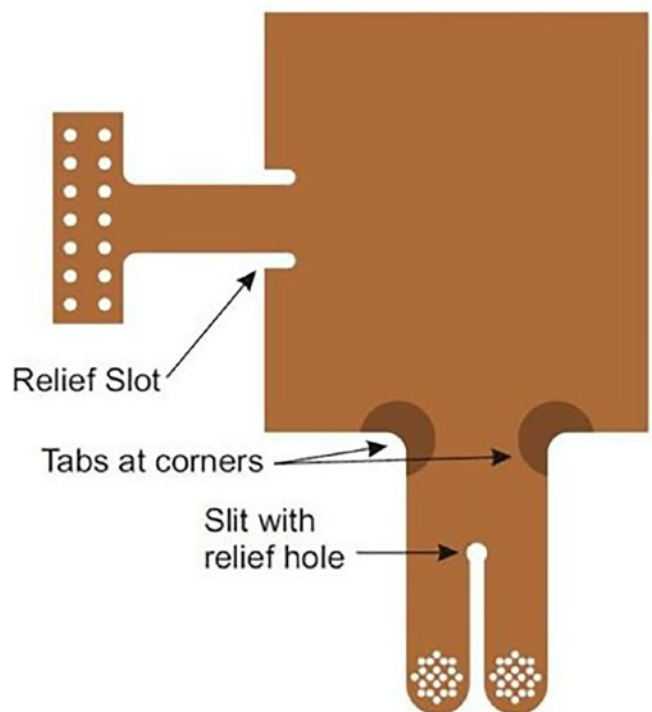


Figure 6: Tear relief techniques.

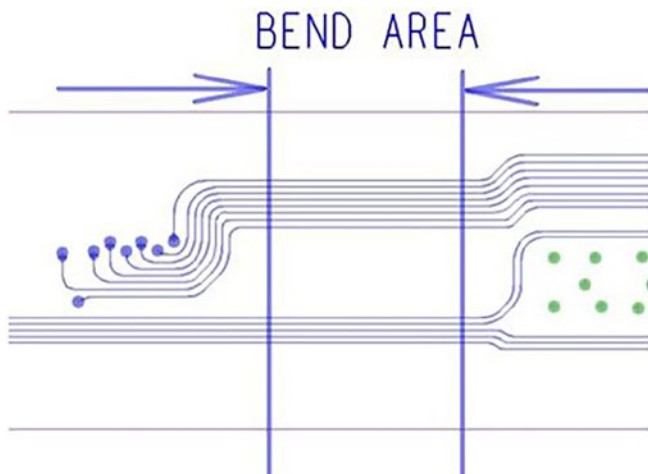


Figure 7: Trace routing in the bend area.

The stiffener's edge on a thin FPC could create a stress area. To avoid cracks or tears in the close proximity to stiffener, a space between the stiffener edge to a via pad edge should be in a range of 1–1.8 mm, depending on the stiffener type. The minimum clearance between the two stiffeners has to be considered. For example, a distance of more than 0.6 mm should be provided between a stiffener located on the top side and the second stiffener located on the bottom side of the FPC.

The static and dynamic bend areas of a flexible circuit are difficult to design. Traces must be routed perpendicular to the bend area (Figure 7).

The designer can find minimum trace width and spacing in the fabricator's capability section. Minimum trace spacing also depends on the copper thickness on the inner layer. For the

calculation of the external layer's minimum trace spacing, copper plating should be added to the copper thickness of the trace.

High-speed designs always include controlled impedances. The reference planes for single-ended and differential pairs should be carefully considered. Copper is the main ingredient that adds rigidity to any construction. Knowing that, an appropriate technique will be applied to each case. If the FPC has no bend requirement, a multilayer construction is possible. The preferable FPC type for dynamic bend is one layer construction. However, double-sided adhesiveless substrate and even three-layer with an air gap will also work for dynamic bend.

For controlled impedance (microstrip), at least two signal layers are required, where one of the layers is a reference plane. When controlled impedance signals are routed on the area of a dynamic bend, the designer should consider air gaps in the stackup.

For signal integrity improvement, blind and buried via techniques can be useful. This technique allows via stub elimination in high-speed applications. However, this production technique costs extra.

Using a low-profile additive copper deposition technique makes it possible to produce 100-Ohm differential with 1-mil trace width and 1-mil spacing.

For high-speed designs, EMI is always a concern. Shielding techniques are applied. The perfect EMI shields are silver films. These films' thick-

ness could vary from 22–32 μm . However, at frequencies higher than 10 GHz, the material must be tested since the efficiency of the films could be deteriorated (Figure 8).

Tolerancing of FPCs is very important due to the nature of materials. In comparing thick adhesive and coverlay materials and thin adhesiveless laminates, the designer should understand that the material movement will be different for each of these materials; as

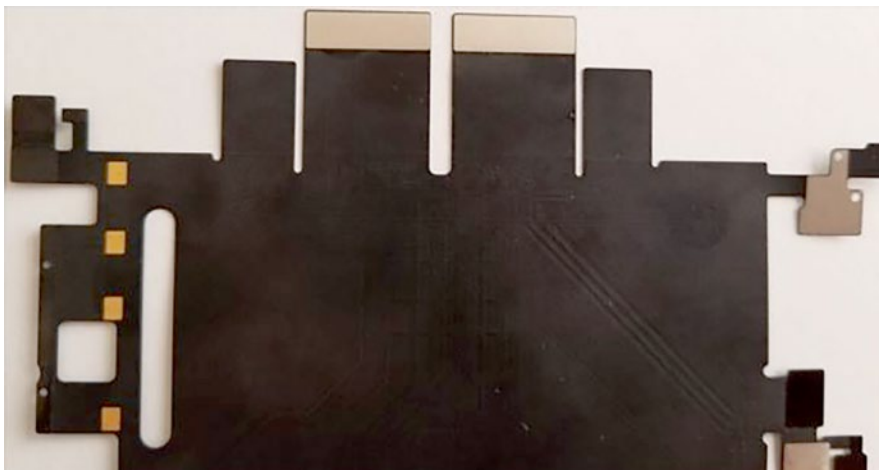
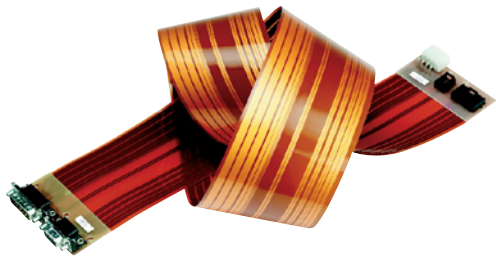
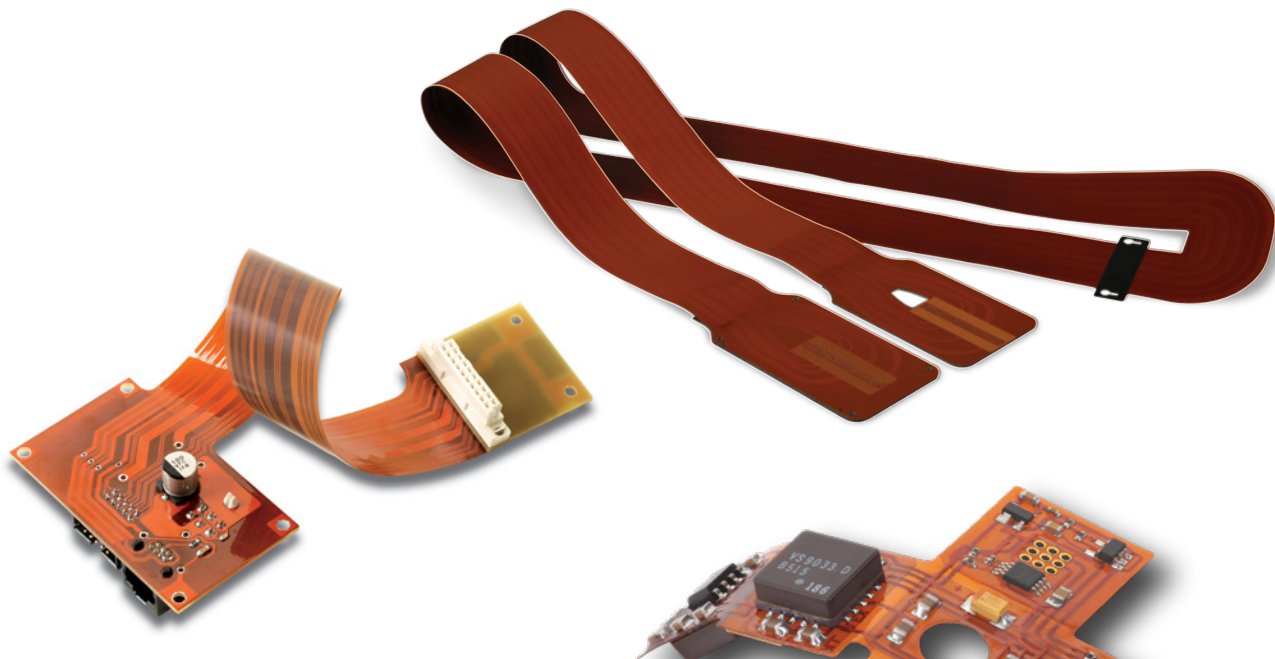


Figure 8: Shield film application.

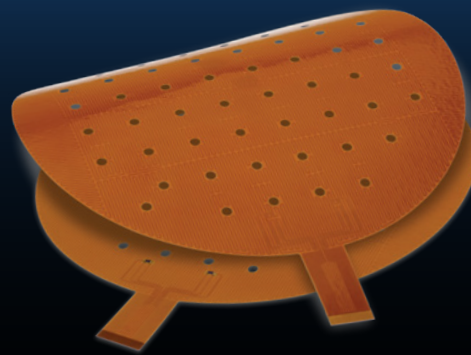


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a result, it could cause difficulties at the production.

In general, all FPC tolerances are more relaxed than PCB tolerances. All features listed in the production rules have lists of sub-requirements for tolerances for those same features. FPC designers have to take into account all the relevant tolerances. That will lead to smooth and faster production.

Collaboration with the assembly house is also important. My personal preference is working with those vendors that integrated both FPC production and assembly facilities. This combination of two industries under one roof provides an advantage of a collaborative effort of FPC production and assembly in creating comprehensive design rules, better and prompt customer support, and fast communication between departments in problem solving. In addition to this, the FPC handling and transfer are more reliable and accountable at these combined production houses.

Summary

This technical article has provided a brief overview of tips for the new flex designer, including important flex design techniques and must-list requirements for keeping FPCs flexible.

The flex designer should always collaborate with electrical, mechanical, production, assembly, test, and DFM groups for final product success. Specific requirements are applied based on applications, production specifics, flex materials and environmental requirements. Flex designers must understand and incorporate all production restrictions and limitations into their layout design rules. **FLEX007**



Olga Scheglov, CID+, is an electrical engineer with over 20 years of experience in rigid and flexible printed circuit board design and production. She has 11 years of teaching experience and is currently a CID instructor with EPTAC.

TNO at Holst Centre Taking Significant Steps Toward Enabling 3D Printing for Electronics

TNO at Holst Centre Taking Significant Steps Toward Enabling 3D Printing for Electronics

3D printed electronics is currently in the early stages of development and an emerging technology at the intersection of 3D printing and printed electronics. TNO at Holst Centre has created several proof-of-concept demonstrators in collaboration with partners like Signify, Bosch and Neotech in the Hyb-Man consortium.

This European consortium has developed and implemented methods to apply 3D printing to electronic products and consists of partners from every link in the value chain. Hyb-Man aims for complete, first-time-right processes that reduce waste and enable personalisation. The result? A significant step towards the design and manufacturing of customised electronics.

3D Printed Electronics

3D printed electronics combines structural and electronic manufacturing into a single

step. The electronic circuits are created using printed electronics technologies as part of the 3D printing production process, embedding them directly into structural components. In designing products, there is no longer a need for separate circuit boards or electronics layers, giving complete design freedom and inherent protection from dust and dirt.

Promising application areas include:

- Customized, lightweight smart wearables for the medical industry, the defence sector and consumers
- Small-series semiconductor packaging
- Free-form antennas for automotive, communications and defence

Partnerships

TNO at Holst Centre's role in the Hyb-Man project was the development of 3D printed electronics process and the manufacturing of demonstrators. Holst Centre wants to continue to explore the potential of this promising technology and are keen to hear from potential partners to help shape the technology roadmap. (Source: TNO)





Flex007 Highlights



Dale Smith and David Moody: Lenthor Pushing Limits of Flex Technology ▶

In this interview, Dale discusses his background and his responsibilities at Lenthor since joining the company in May. Dale explains his plans to continue implementing the company's Lean program, as well as pushing the technology limits for their flex customers. David addresses Lenthor's operations during the COVID-19, when the company stayed up and running with safety measures in place, and what the landscape might look like after the smoke clears.

EPTE Newsletter: Monocoque Printed Circuits, Part 4 ▶

Based on past columns where Dominique Numakura explored the basic concept of monocoque printed circuits, he received many inquiries and questions about this new circuit technology. In this column, he continues to explore alternative technology in flexible circuits.

Just Ask Happy: Ranking the Top Countries by Fab Technology and Production ▶

As part of our "Just Ask Happy" series, one of our readers asked Happy to rank the top countries that provide PCB fabrication services. How would you rank these countries? Check out the global fab trends now and in 10 years.

Merlin Flex Achieves Formal Global Approval by Thales U.K. ▶

Merlin Flex is pleased to announce that the company has been included in the Thales U.K. Approved Supplier Panel for PCBs as granted by the Thales global category manager.

Matrix Offering a Lamination Assist System for Flexible Circuit Lamination ▶

Matrix Electronics is promoting EuroPads press pads and EuroForm conformal release film as a system package for the lamination of flexible PCBs. Designed and offered as part of the new EuroAssist product line, EuroPads and EuroForm are exceptional alternatives to the many confusing and expensive competitive options currently available.

HARTING's Component Carrier Can Replace Flexible PCBs ▶

By harnessing this new HARTING development, electronic components can be fitted directly onto the component carrier, thereby replacing flexible circuit boards. The component carrier serves as a connecting element between the PCB and electronic components, such as LEDs, ICs, photodiodes, and sensors.

Nano Dimension Appoints LM Instruments to Market PCB/Hi-PEDs 3D Printers ▶

Nano Dimension Ltd. has signed an agreement with LM Instruments, which will represent Nano Dimension in the Mid-Atlantic states by marketing its 3D fabrication machines for high-performance electronic devices (Hi-PEDs).

Atotech Looks to Expand Product Portfolio ▶

When Barry Matties toured Atotech's facility in Feucht, Germany, last year before production, he spoke with Andreas Schatz, Atotech's global product manager of equipment, and Daniel Schmidt, Atotech's global director of marketing. Andreas and Daniel break down the global plating and chemistry trends they see, most notably around horizontal plating and smart factory automation.

Next-Generation Flex Circuits: Monocoque Printed Circuits

EPTE Newsletter

by Dominique K. Numakura, DKN Research LLC

Several weeks ago, I released a [short column](#) about monocoque printed circuits, a new 3D circuit technology using thermoplastic materials considered next-generation technology for printed circuits. The circuit traces are built on thermoplastic sheets and bent using a heating process. The new technology reduces wiring space in mobile electronic devices and eliminates flexible circuits and wire harnesses. I received many inquiries, specifically requesting detailed technical information. A few companies commented about their success with this same circuit technology. There is much interest from design engineers looking for practical 3D wiring material for compact electronic devices, such as smartphones and digital cameras. Let's take a brief look at this new 3D circuit technology.

More than 30 years ago, a flex circuit manufacturer in New England developed bendable

circuits and modified the standard technology for flex circuits. A plastic resin was introduced as a base layer for copper foil laminates. The laminates were chemically etched to generate copper circuits, and these circuits could be bent to form 3D wiring. Unfortunately, the base material was not stiff enough, so 3D circuits were eliminated in many applications.

Almost the same time 30 years ago, the basic concept for molded interconnect device (MID) circuits was created to build 3D circuits on plastic parts. The process of creating 3D components was already established through molding or injection using traditional plastic resins. Component manufacturers found it difficult to generate electronic circuits on plastic components. They tried with newer technologies (metalizing and laser scribing) but were unsuccessful due to the limited capabilities of these technologies.



THE NEXT BIG THING IS HERE



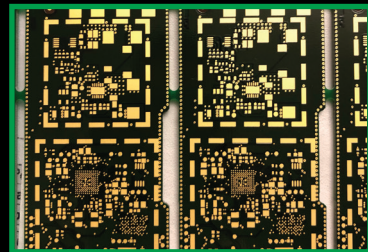
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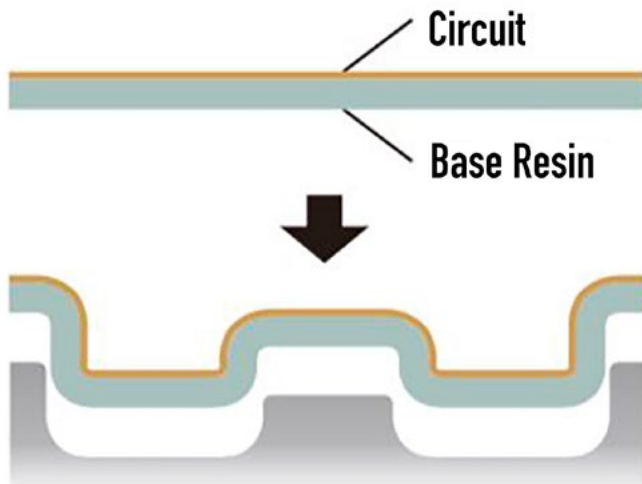


Figure 1: The basic manufacturing process of monocoque circuits (step 1: Screen print single-layer double-layer, and multilayer circuits with via holes; step 2: forming in the die set at the appropriate temperature and pressure).

An easy solution came to light using silver ink printing for thick-film circuit technology. It looks like a Columbus egg. The process is very simple (Figure 1). Silver-based conductive ink is screen-printed on a thermoplastic sheet to create electronic circuits. Single-layer circuits are easy to make. Double-layer and multilayer circuits are practical as they are made on a film base substrate with via holes. Through-holes are easy to make using a traditional thick film process. The baking temperature should be relatively low to generate a higher yield. Appropriate ink materials are selected for the thermal process. The second step of the pro-

cess is to place the work in a die set after preheating. A vacuumed forming could make a better shape for the thicker substrates. We are successful using PET sheets, PEN films, acrylic sheets, polycarbonate sheets, and more. There may be additional plastic resins available.

3D circuit technology is not universally available because of mechanical stresses during the forming process. The forming on the corners requires a radius greater than 2 mm, and the silver traces should be wider than 0.3 mm. We are preparing a design guide for 3D circuits.

The best feature of this 3D circuit technology is the wiring built-in plastic parts. The plastic parts will serve as mechanical framing and wiring—hence the name monocoque printed circuits. The use of supplemental flexible circuits and wire harnesses are not required; the space required for wiring is reduced without an increase in cost. There are no special technologies or manufacturing equipment required, but experience using specific materials is necessary. **FLEX007**

Editor's note: Read [Part 1](#), [Part 2](#), [Part 3](#), and [Part 4](#) on monocoque printed circuits.



Dominique K. Numakura is the managing director of DKN Research LLC. To read past columns or contact Numakura, [click here](#).

EHang Expanding Facility for Autonomous Aerial Vehicles

EHang Holdings Limited, the world's leading autonomous aerial vehicle technology platform company, announces it will build a new AAV production facility in Yunfu city in Guangdong, China with a planned initial annual capacity of 600 units and an RMB42 million (US\$6 million) investment supported by the local government in the facility. The EHang Yunfu facility is aimed to be established as an industry-leading AAV production center, including an R&D facility for air mobility solutions and a

training center for operations and technical talents.

The Deputy Mayor of Yunfu city, Donghong Shi attended the launch ceremony and commented that the Yunfu city government welcomes and fully supports the world's leading high-tech company EHang to establish its new production facility for the cutting-edge AAV products in Yunfu and it is expected to bring strong vitality to the local high-tech communities and create hundreds of new jobs for local talents.

(Source: Globe Newswire)





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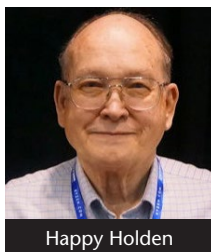
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1 Just Ask Happy: Stacked Microvia Reliability Issues ►

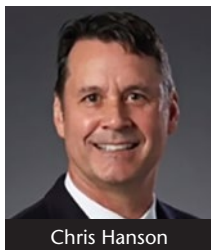
We asked for you to send in your questions for Happy Holden, and you took us up on it! The questions you've posed run the gamut, covering technology, the worldwide fab market, and everything in between. One of the topics that readers most often ask about is microvia reliability.



Happy Holden

2 Chris Hanson: New Ventec IMS Dielectrics Rated for Higher Temps ►

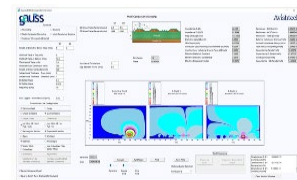
Andy Shaughnessy recently spoke with Chris Hanson, global head of IMS Technology for Ventec International Group. During their conversation, Chris discusses his group's recent efforts to create new IMS materials, with a focus on dielectrics.



Chris Hanson

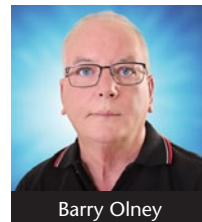
3 Avishtech Announces Gauss Stack and Gauss 2D PCB Modeling Software ►

Avishtech Inc.—a simulation-based design software provider, headquartered in San Jose, California—announced the introduction of its Gauss suite of software for the design and simulation of PCB stackups and transmission lines used in PCBs and semiconductors.



4 Beyond Design: Split Planes—Reprise ►

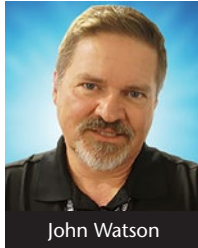
A high-speed digital signal crossing a split in the reference plane impacts at least three aspects of design integrity: signal quality, crosstalk, and EMI. Barry Olney reviews the two common solutions, plus introduce a third optimal solution for high-speed design.



Barry Olney

5 Elementary, Mr. Watson: PCB Components Naming Conventions ▶

How you accurately analyze and identify certain information has a direct connection to the overall success of your PCB designs. In this column, John Watson focuses on the conventional naming scheme for the schematic symbol and footprint to prevent headaches and ulcers later.



John Watson

8 Lightning Speed Laminates: High-Frequency Circuit Material App Notes ▶

High-frequency circuit materials are used in a variety of diverse applications. Due to this diversity, it is difficult to write an app note for a specific high-frequency circuit material. John Coonrod explains while exploring Rogers Corporation's app notes.



John Coonrod

6 AltiumLive 2020 Goes 'Virtual' ▶

Like most events in 2020, Altium is transitioning its annual flagship conference, AltiumLive, to an online experience this year. Altium will host its North American event from October 6–8, and the European event from October 20–22, 2020. Both events are free to attend.



9 Dana on Data: How Can the PCB Industry Improve From COVID-19 Responses? ▶

In response to the COVID-19 pandemic, the world transformed a very slow medical approval process into the equivalent of a concurrent NPI process by challenging some of the golden rules. Dana Korf shares his thoughts on four areas the PCB industry can re-evaluate and improve.



Dana Korf

7 Connect the Dots: The Power of Forward Thinking ▶

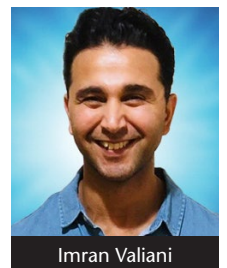
Innovation comes in many forms and from more places these days. Bob Tise and Matt Stevenson discuss how innovative electronic devices all contain PCBs, and share pro design tips for bringing new products to the market.



Stevenson and Tise

10 Time to Market: It's Crunch Time! ▶

After sharing a crunch-time scenario, Imran Valiani emphasizes the importance of solid communication on getting to market on time—especially if you're not using a one-stop-shop for design, fabrication, and assembly.



Imran Valiani

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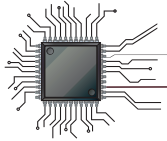
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Responsibilities

- Marketing research to identify target customers
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
 - Market and product
 - Circuit types used
 - Competitive influences
 - Philosophies and finance
 - Quoting and closing orders
 - Providing ongoing service to the customer
 - Develop long-term customer strategies to increase business

Qualifications

- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is a leader in flex and rigid-flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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Senior Process Engineer

Job Description

Responsible for developing and optimizing Lenthor's manufacturing processes from start up to implementation, reducing cost, improving sustainability and continuous improvement.

Position Duties

- Senior process engineer's role is to monitor process performance through tracking and enhance through continuous improvement initiatives. Process engineer implements continuous improvement programs to drive up yields.
- Participate in the evaluation of processes, new equipment, facility improvements and procedures.
- Improve process capability, yields, costs and production volume while maintaining safety and improving quality standards.
- Work with customers in developing cost-effective production processes.
- Engage suppliers in quality improvements and process control issues as required.
- Generate process control plan for manufacturing processes, and identify opportunities for capability or process improvement.
- Participate in FMEA activities as required.
- Create detailed plans for IQ, OQ, PQ and maintain validated status as required.
- Participate in existing change control mechanisms such as ECOs and PCRs.
- Perform defect reduction analysis and activities.

Qualifications

- BS degree in engineering
- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is the leader in Flex and Rigid-Flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

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- Ensure company is in compliance with legislative and regulatory requirements
- Supply technical support in all areas throughout the company in accordance with instructions of the operations director
- Collaborate with both quality and production departments to ensure the quality of the product
- Plan and manage the evaluation, introduction and acceptance trials of new equipment and processes
- CTO will manage the operational and fiscal activities of PCB engineering processes, procedures, technology, and the Somacis Process Engineering Team

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- Ten years' progressively complex technical experience in PCB manufacturing processes involving the latest state-of-the-art applications and techniques

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- Internal and supplier auditing
- Product audits
- Sign off on TEOs and MRBs
- Reporting KPI performance to operations manager
- PPAP
- FMEA, control plan
- Customer complaints, RMAs investigation and reporting
- Project lead
- MSA design and implementation
- Maintenance of approved supplier list (ASL) and approved parts list (APL)
- Supplier risk assessments
- CAPAs, including SCARs
- Product qualifications
- Maintenance of equipment list
- Control of non-conforming product
- Sign off on change management (minor)

REQUIREMENTS

- IT literate
- Excellent written and verbal communication skills
- Strong interpersonal skills
- Numerate
- Six Sigma green belt
- Core Tools trained and certificate held
- Experienced auditor to IATF standard
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- Several years' experience in a quality department within the automotive industry, including experience of IATF16949
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Career Opportunities



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Alpha Circuit Corporation is a manufacturer of printed circuit boards located in Elmhurst, IL. We are currently seeking an operator in our Image department.

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Responsibilities:

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Qualifications

Required: Bachelor's degree from a technical college/university in an associated field. Three years directly related experience, or equivalent combination of education and experience. Must possess a valid driver's license and have a clean driving record.

Preferred: Experience in control systems and electronic troubleshooting, as well as in general electrical and mechanical service tasks. Experience and knowledge in the PCB manufacturing process, with a focus on laser drilling and/or direct imaging.

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Career Opportunities



Process Engineering Director

Whelen Engineering Co., Inc. seeks full-time process engineering director in Concord, NH, to develop, plan and execute GreenSource Fabrication, LLC Div.'s process technology business strategy; manage process engineering activities, staff and compliance; improve process design, cost, quality and resource utilization; interact w/ customers and incorporate feedback; develop financial capital and labor projections; travel internationally for conferences, supplier and customer visits (15-25% work-time); write white papers, IP applications and give talks re. Division's products/processes.

Min. req.: U.S. Bachelor's or foreign equivalency in environmental science or engineering; min. 10 yrs. work exp. in: PCB fabrication process engineering; comprehensive and current experience in PCB fabrication/substrate markets w/ SAP tech; developing chemical and mechanical processes, chemistries and equipment for PCB manufacturing demonstrated by international experience implementing complex processes; ability to direct and troubleshoot PCB manufacturing problems; min. 5 years exp. leading, managing and training process engineering teams, developing and executing process technology business strategies and plans in worldwide PCB markets, including Japan, Taiwan, China, Europe; min. 3 years exp. giving talks, writing and presenting white papers; ability to travel internationally (15-25% worktime).

Send CVs to: Corinne Tuthill,
ctuthill@greensourcefab.com
or GreenSource Fabrication, LLC,
99 Ceda Road, Charlestown, NH 03603.

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Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
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Career Opportunities



APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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Development Chemist Carson City, NV

Develop new products and modify existing products as identified by the sales staff and company management. Conduct laboratory evaluations and tests of the industry's products and processes. Prepare detailed written reports regarding chemical characteristics. The development chemist will also have supervisory responsibility for R&D technicians.

Essential Duties:

- Prepare design of experiments (DOE) to aid in the development of new products related to the solar energy industry, printed electronics, inkjet technologies, specialty coatings and additives, and nanotechnologies and applications
- Compile feasibility studies for bringing new products and emerging technologies through manufacturing to the marketplace
- Provide product and manufacturing support
- Provide product quality control and support
- Must comply with all OSHA and company workplace safety requirements at all times
- Participate in multifunctional teams

Required Education/Experience:

- Minimum 4-year college degree in engineering or chemistry
- Preferred: 5-10 years of work experience in designing 3D and inkjet materials, radiation cured chemical technologies, and polymer science
- Knowledge of advanced materials and emerging technologies, including nanotechnologies

Working Conditions:

- Chemical laboratory environment
- Occasional weekend or overtime work
- Travel may be required

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Career Opportunities



SMT Field Technician Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

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U.S. CIRCUIT

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for
more information.

mfariba@uscircuit.com

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Career Opportunities



IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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This professional has done it all. Built new businesses and turned around hurting businesses and made them successful. A proven record of success. This candidate is a game-changer for any company. He is seeking a full-time leadership position in a PCB or PCBA company.

General Manager PCB and PCBA

Senior manager with experience in operations and sales. He has overseen a number of successful operations in Canada. Very strong candidate and has experience in all aspects of PCB operations. He is looking for a new full-time position in Canada.

Regional Sales Manager/Business Development

Strong relationship management skills. Sales experience focused on defense-aerospace, medical, high-tech PCB sales. Specializes in technical sales. Also has experience in quality, engineering, and manufacturing of PCBs. He is looking for a fulltime position in the South-eastern U.S.

Field Application Engineer (FAE)

Has worked as a respected FAE in the U.S. for global companies. Specializes in working alongside sales teams. Large experience base within the interconnect industry. He is looking for a full-time position.

Business Development Manager

Understands all aspects of interconnect technical sales from PCB design and fabrication to assembly and all technologies from HDI microvias to flex and rigid-flex. Has also sold high-tech laminates and equipment. Proven record of sales success. He is looking for a full-time position.

CEO/President

Specializes in running multi-million dollar companies offering engineering, design, and manufacturing services. Proven leader. Supply chain manager. Expert at developing and implementing company strategy. Looking to lead a company into the future. He is looking for a full-time position.

PCB General Manager

Forty years of experience serving in all capacities, from GM to engineering manager to quality manager. Worked with both domestic and global companies. Available for turn-around or special engineering projects. He is looking for long-term project work.

Process Engineering Specialist

Strong history of new product introduction (NPI) manufacturing engineering experience: PCB/PCBA. Held numerous senior engineering management positions. Leads the industry in DFM/DFA and DFX (test) disciplines. He is looking for either a full-time position or project work.

VP Sales Global Printed Circuits

Worked with a very large, global company for a number of years. Built and managed international sales teams. Created sales strategies and communicated them to the team. One of the best sales leaders in our industry. He is looking for a full-time position.

Plant Manager

This professional has years of experience running PCBA companies. Led his companies with creative and innovative leaderships skills. Is a collaborative, hands-on leader. He is looking for a full-time position.

National Sales Manager

Seasoned professional has spent the past 20 years building and growing American sales teams for both global and domestic companies. Specializes in building and managing rep networks. He is looking for a full-time position.

Global Engineering Manager/Quality Manager

Has experience working with large, global PCB companies managing both engineering and quality staff. Very experienced in chemical controls. She is interested in working on a project-by-project basis.

CAM Operators and Front-end Engineers

These candidates want to work remotely from their home offices and are willing to do full-time or part-time projects.



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