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ROADMAPS

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PAGE 78

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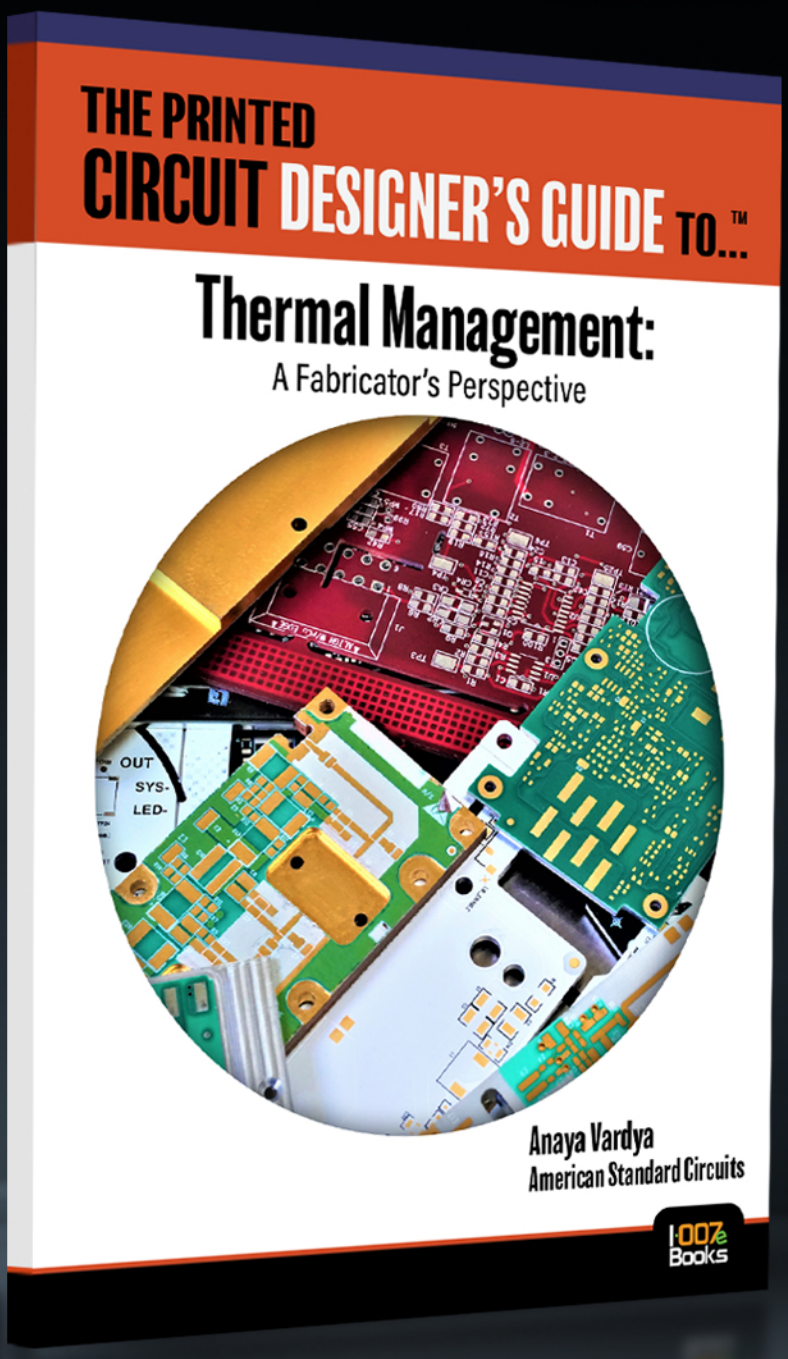

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Roadmaps: Into the Future

Even the most experienced hikers can get lost if they don't have a map. The same holds true in the world of PCB design and manufacturing—if your company doesn't have a technology roadmap, it's hard to know where you're going technologically. This month, we take a look at a variety of technology roadmaps related to PCB design, and some of the milestones that may be in our not-too-distant future.


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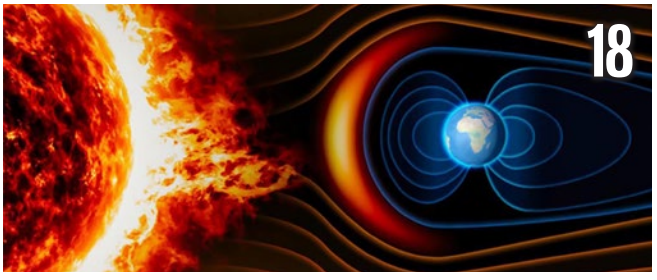

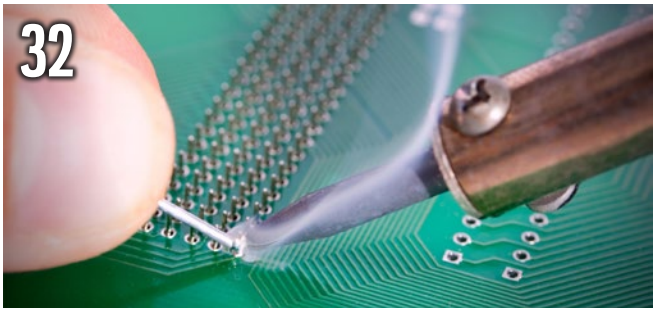

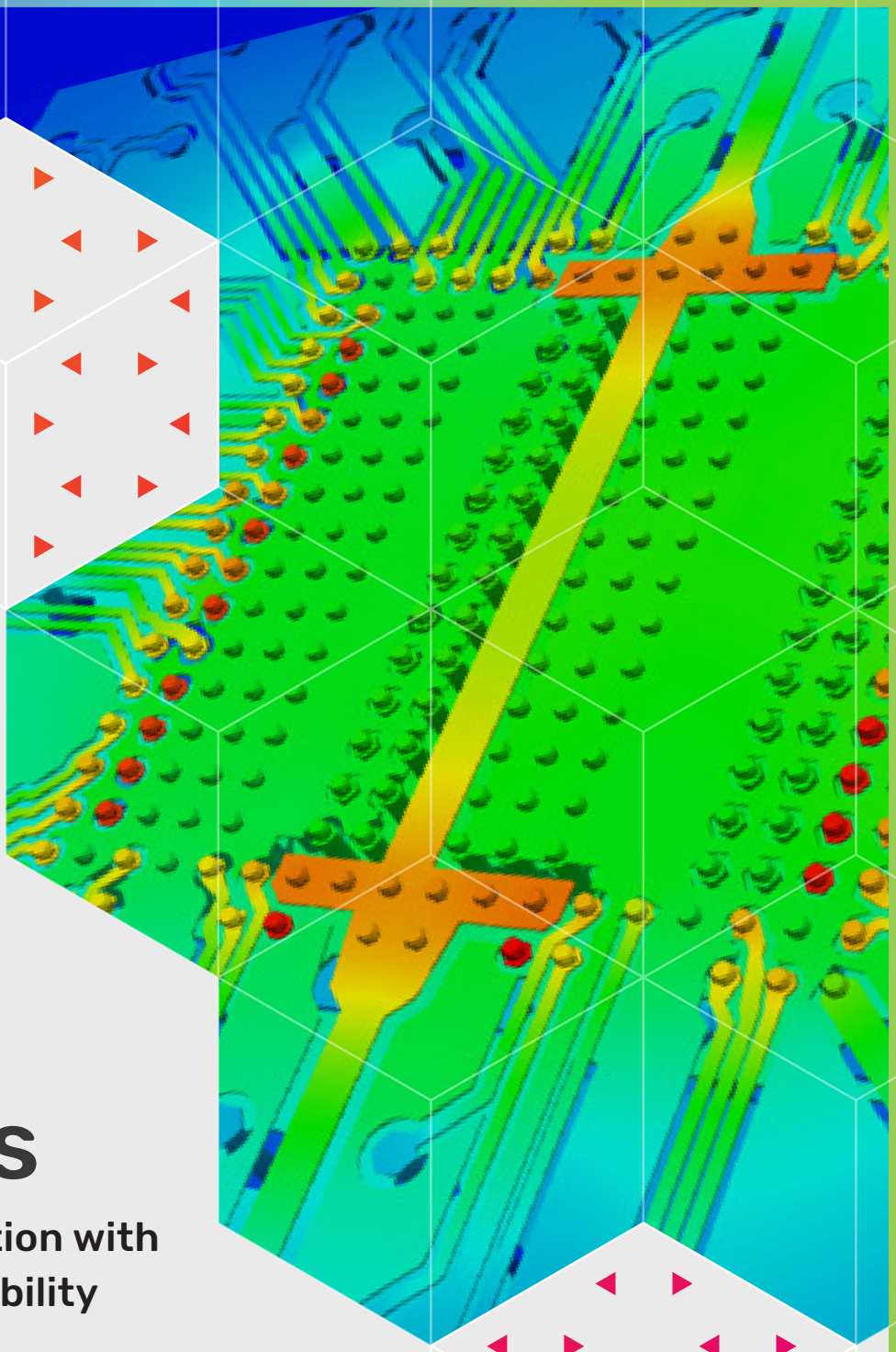

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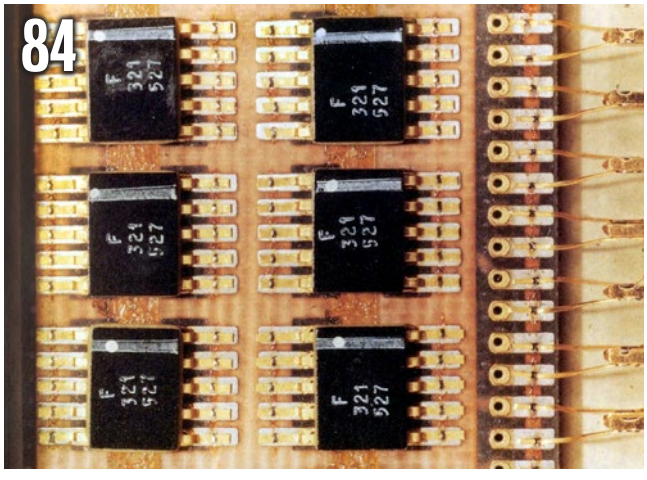
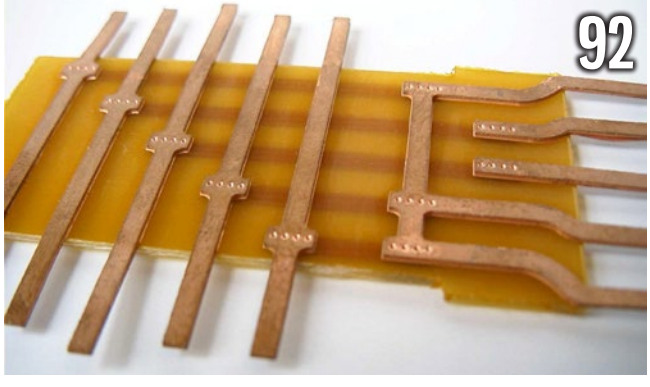
This Month in Flex

Creating a technology roadmap is never a simple task; companies and organizations often spend years editing and fine-tuning their tech roadmaps. This task is exponentially tougher for a segment like flexible and rigid-flex circuits, which seems to be evolving constantly. Would you care to hazard a guess about where flex technology might be in five or 10 years?





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The Future Is Now

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

Our technology roadmaps issue started with a question for Happy Holden.

A few months ago, we were planning content for the fall issues of our magazines. We had just launched the "Just Ask Happy" series, with readers sending him all manner of questions about HDI, automation, predictive engineering, TQM, markets—you name it.

But one question caught our attention: How will the PCB design process change to align with the IEEE Heterogeneous Integration Roadmap (HIR), and do you think this will happen? Good question.

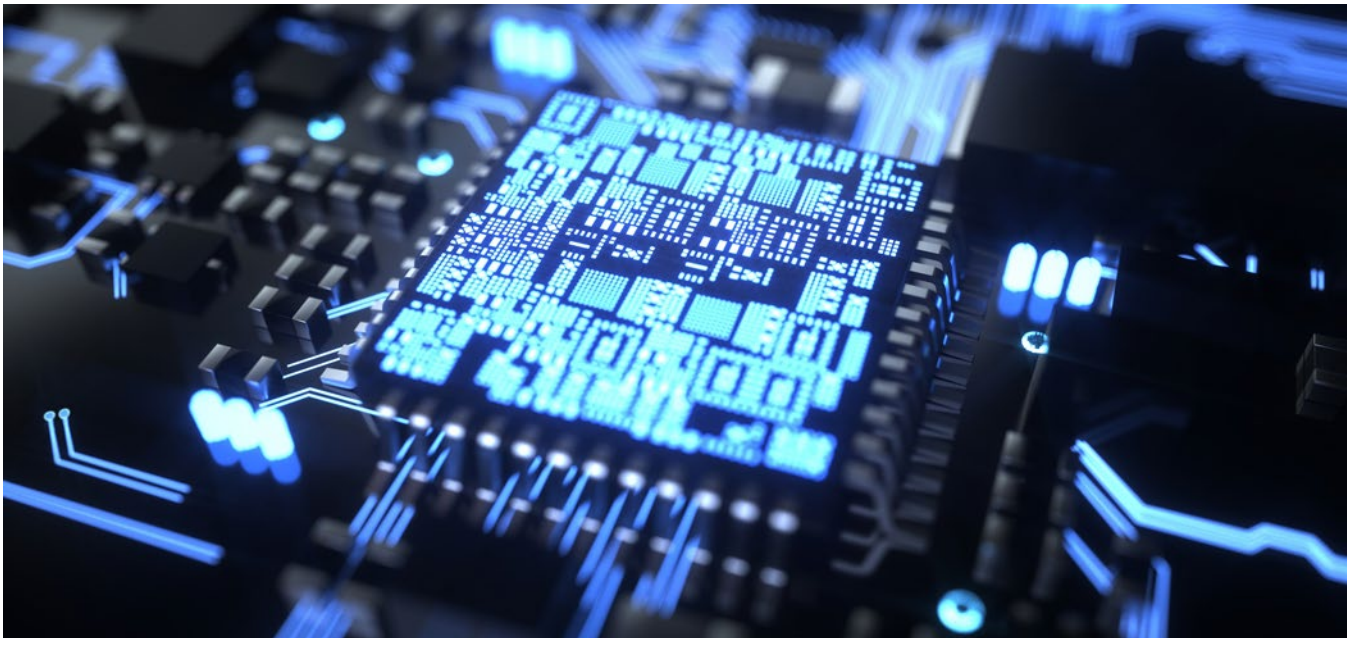
Happy explained that IEEE is now referring to chip-on-board (COB), multi-chip modules (MCM), and system-in-packages (SIP) as heterogeneous integrated modules (HIM). As Happy noted:

"Heterogeneous was chosen because the future modules will incorporate not just IC chips, but also power devices, passive discretes, photonics, MEMS, sensors, antennas, and batteries. Systems-on-chip (SoC) will continue to be an activity, but as Moore's Law has flattened out, using multiple-cores processor chips with memory is more cost-effective for greater computing power. As applications grow—and size, cost, and weight are more critical—heterogeneous integrated modules offer the best choice to move all of these elements closely together in a module."

In other words, these packages are becoming a lot like little circuit boards.

In the future, we'll be mounting small PCBs on traditional PCBs. My first thought is, "Cool! What will they think of next?"

But there are going to be ripple effects from this. What kind of thermal, signal integrity, and EMC issues will traditional PCB designers have to contend with 10 years from now when each board is essentially a system, comprised



of smaller, fully functioning PCBs? This takes DFM and DFT to a new level as well.

This is another example of the "blurring of the lines" concept that IPC President and CEO John Mitchell discussed in a recent installment of "Just Ask John Mitchell." The move to heterogeneous integrated modules won't be an overnight, quantum leap in technology development, but it will be disruptive.

For this month's issue on technology roadmaps, we bring you several interviews with HIR contributors. Rita Horner of Synopsys offers a great overview of the HIR and the effects of heterogeneous integration on the technology of the future. Paul Wesling of IEEE explains the creative process that leads to the development of the 584-page, 23-chapter HIR. Dr. José Schutt-Aine, professor of electrical and computer engineering at the University of Illinois, takes us through his chapter in the HIR and explains how PCB designers can facilitate co-design at the IC and package level. And Jeff Demmin of Keysight Technologies discusses the effects of heterogeneous integration on the military and aerospace segments.

We also have a conversation with Todd Westerhoff of Mentor, a Siemens Business, who details the company's plans for the high-speed design tools of the future. Michael Nopp of Cadence Design Systems discusses the company's move toward creating the next generation of more electrically-aware PCB designers, and Leigh Gawne of Altium provides a roadmap for the company and the Altium 365 platform, in particular. Carey Burkett and Mark Finstad of Flexible Circuit Technologies share their thoughts on the direction of the company and some of the trends and challenges likely to face flex designers and manufacturers over the next few years. And Joe Fjelstad explains why technology roadmaps are so vital to technologists working to develop the processes of tomorrow.

We also have columns from Barry Olney, Kelly Dack, John Coonrod, John Talbot, Jade Bridges, and Matt Stevenson and Bob Tise.

If you missed the virtual SMTA International 2020 show, don't worry. Visit Real Time with… SMTAI 2020 and check out our video interviews with the top engineers, managers, and executives who attended this event.

Stay safe, and see you next month. **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 20 years. He can be reached by clicking here.

Looking Into the Future With Progressive Design and Analysis

Feature Interview by the I-Connect007 Editorial Team

This month, we're focusing on technology roadmaps. We wanted to get a feel for the future of high-speed EDA tools, so we spoke with Todd Westerhoff, product marketing manager for high-speed tools at Mentor, a Siemens Business. Todd discussed the future of high-speed PCB design tools, as well as some of the many market forces that are driving the development of the company's tools and the overall EDA segment. He also details a new approach that Mentor is taking: progressive design and analysis.

Andy Shaughnessy: Todd, why don't you give us a look ahead at Mentor's high-speed tools and tie it in with what you see going on in the industry in the near future.

Todd Westerhoff: Thanks, Andy. When we met at DesignCon this year, we said, "It's the small stuff that gets you." We meant that if you look at what holds up design projects, it's often not the state-of-the-art problems you would expect. It's the stuff that you thought was straightforward that bites you in the end. As a design community, we're pretty good at the complicated stuff because we pay careful attention to it, but we get can be tripped up on what should have been easy.

Most companies see signal integrity (SI) as too time-consuming or too complicated for system designers, so analysis gets put into the hands of dedicated specialists to make the process "more efficient." SI analysis then becomes concentrated at the end of the design cycle. Good post-layout verification will find problems before fab-out and avoid wasting money on prototypes, but you're still finding errors well past the point where they were introduced into the design. That means parts of the design have to be ripped up and rerouted, and there's a schedule impact associated with that. We want to give system designers tools where they can find and correct those errors as early as possible.

We need a class of analysis tools that will allow system designers to effectively evaluate trade-offs and make design decisions without having to get the SI expert involved. The accuracy doesn't have to be as good as what the expert uses—something we call first-order analysis. The goal is to look at things more qualitatively. We don't need to compute system margin down to millivolts and picoseconds on an absolute basis; we want to know how a

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change will affect signal quality and timing on a relative basis. We want tools that let system designers make more informed decisions on their own because the SI expert's involvement generally has to be scheduled, but the need to evaluate design trade-offs is constant. Giving system designers good first-order analysis tools means the design will be in better shape when the SI specialist looks at it, which helps reduce design spins.

Shaughnessy: Are you talking about having an analysis run in the background during the layout process?

Westerhoff: Not necessarily. Analysis is more useful as a "checkpoint" process, particularly at the interface level. There's not much point in running analysis on half of an interface; it's better to get to a point where the design has reached some level of completeness and then produces results quickly. After each checkpoint, you continue to refine the design and add detail, gradually predicting the system operating margin more and more accurately.

We refer to this process as progressive design and analysis. We're trying to match analysis to the way design normally takes place. You start by figuring out the big stuff and then add details as you go, checking your design each step of the way.

For this to work well, you need several things:

1. A repeatable analysis process that produces a numerical metric for system operating margin.
2. An established pass/fail threshold for system operating margin.
3. An ability to dial design details and physical effects in and out of the system model.

Let's take a closer look at each of these individually.

Analysis Process

First, the analysis process and results have to be absolutely repeatable. Simulation isn't much good if you can't run the same analysis twice and get the same results. When you're assessing design trade-offs, you need to know that the simulation process you're using is rock solid, or you won't have much confidence in the design decisions you make. You want that process to be entirely automated so that you just define simulation parameters and the analysis process runs by itself, always producing the same results in the same format.

Pass/Fail Threshold

Second, you need well-defined criteria for whether a design passes or fails. System operating margin can be specified in millivolts, picoseconds, decibels, or something else, but it needs to be specific, defined, and numeric, and it needs to match what the analysis process actually produces. That way, there's no ambiguity about success or failure and no ambiguity over which design alternative provides more margin.

Variable Modeling Accuracy

Third, when we add more detail into a system interconnect model, the model takes longer to generate, and the resulting simulation runs slower. We don't need ultimate accuracy early in the design process when we're just roughing the design in; it slows the process down without adding much value. Matching the model detail to the task at hand will make the process more efficient. Equally important, being able to dial design details and physical effects in and out of the system model allows us to numerically quantify the impact they have on system margin. It doesn't make sense to spend a lot of time optimizing something that has a negligible impact, and the things that matter most will change from design to design. During active design, we want to focus on what matters most and optimize the design accordingly.

Progressive design and analysis means we use basic models at the start and add detail as we go. The level of detail in our model increases as the design progresses. Because we know there are things we're not modeling at any given point, there's an ambiguity, or "error band," in our analysis that's large at the start

and small at the end. Thus, an analysis that exceeds the pass/fail threshold by a small amount at the start of the cycle might fail with a more detailed analysis. It's important that we have a sense of how big that error band is, so we can interpret the results of any particular analysis appropriately. Generally speaking, we group analysis results into three categories:

Todd Westerhoff

1. Green: The design has a significant positive margin, even after accounting for the error band in the model. We could perform a more accurate analysis to get a better assessment, but we may not need to. The design might be ready to fab-out as-is.

2. Red: The design has a significant negative margin, even considering the error band. The chances are that the design is broken, and something needs to change. Even though we could perform a more detailed assessment, it's probably best just to figure out what's wrong with the design and fix it.

3. Yellow: The degree of positive or negative margin is within the error band, so we're not really sure whether the design will work or not. A more detailed analysis is needed to be sure.

Process efficiency rises when the analysis result is green or red. In either case, the need for a more detailed analysis has been delayed, and design work can continue in the meantime.

This doesn't eliminate the need to perform a complete post-layout verification before fab-out, and to have that verification performed by a SI expert. This final "gate" to fab-out is proven and valuable. The goal is to improve the quality of designs being passed to SI experts for verification so that fewer design changes are needed.

Shaughnessy: Are you saying you shouldn't have to be an analysis specialist to perform SI analysis?

Westerhoff: Exactly. Let's look at what happens in actual practice with DDR4 as an example. A lot of companies lay out their DDR4 designs based on the controller manufacturer's recommendations and then pass the layout back to the silicon vendor for review. Silicon vendors can't afford to set up and run detailed post-layout verification for all the designs customers want to pass their way, so they need to develop good design "screening" to find common problems. Think of it as trying to find 95% of the problems with 10% of the effort of a full post-layout analysis. Those screening efforts typically take one of two forms:

1. Automated electrical rule checks: These go beyond simple physical rule checks to include things like trace impedance, the proximity of return path vias, etc. The silicon vendors configure rules for their specific device technologies, allowing them to do the same screening an experienced designer might do, but much faster.

2. First-order simulation: Design volume and turnaround time make this simpler than what the vendor would use internally for sign-off. For example, the process might simulate data nets with generic technology models, computing a delay and figure of merit for each signal's quality. This simulation can be run quickly to identify any discrepancies between signals in a data bus.

The question becomes, "If the silicon vendors are already doing this type of screening on the designs customers give them for review, why not put those same processes directly in the hands of customers themselves?" That's what we're looking to do.

We already offer comprehensive electrical design rule checking, and we're bringing out a first-order pulse response analysis patterned after the techniques some of the silicon vendors use. You don't need any simulation model at all. You load your design, set up the analysis

parameters, and run. You can have simulation results within five minutes that give meaningful insight into what, if anything, you should change in your design.

As an industry, we keep getting caught up in the idea that an analysis tool has to do everything with maximum accuracy to be useful. We think that if a tool can meet the needs of the most demanding experts, it will work for everyone, but that's not really true. The "expert" tools are often standalone applications that users string together to form their own analysis flows. The typical system designer doesn't have the time to learn yet another complex tool, let alone multiple tools and a way to string them together. We need focused toolsets that let designers perform basic analysis quickly and that don't have a huge learning curve.

We need focused toolsets that let designers perform basic analysis quickly and that don't have a huge learning curve.

Five years ago, 25-gigabit serial links were the hardest thing going, and you needed the best people in your organization working on them. Today, we're trying to put them in mass production across scores of designs. How are all the teams trying to deploy this technology supposed to get their work done? The experts have all moved on to 112-gigabit links, and they're busy doing that. I think the real challenge is, "How we deploy these advanced technologies once they've been proven?"

Shaughnessy: Do you see your typical users being degreed engineers?

Westerhoff: Let me change that question a bit. I think the challenge is, "Are the people running SI analysis dedicated specialists?" The unfortunate truth is the majority of designs still don't get simulated in any significant way. HyperLynx has enabled a lot of people who aren't SI experts to run their own analysis. Our goal is to expand that pool of people because that's what the industry needs; the shortage of SI experts isn't going away anytime soon.

Happy Holden: Todd is preaching the gospel, based on the time that I spent at Mentor earlier in my career. But this is everything from modeling to simulation to the trade-offs. It was tough 20 years ago, but it's much tougher now.

Nolan Johnson: I spent my time in Mentor championing what we now call the digital twin—a brilliant design advisor that allows the user to make some high-level trade-offs between costs, productivity, thermal, SI, etc. early enough to keep you from running down the wrong alley. Whether or not you know anything about SI, Mother Nature is conspiring against you with very fast transistors. You can set the clock, but you can't change the fundamental characteristic of that transistor, which is going to turn on and off pretty fast.

Westerhoff: The phenomenon of high-speed behavior on slow-speed signals is very real. One of the common rules of thumb is that you need to consider a net as "high-speed" whenever the delay of the net exceeds one-sixth of the driver's edge rate. Consider what that means for a driver with a 250 ps edge rate, which is pretty slow by today's standards. The longest a net could be and not be considered high-speed would be about 42 ps or roughly one-fourth inch. That means pretty much everything is high-speed unless you're dealing with old driver technology on an old process node.

Johnson: And you can't escape it because, like death and taxes, Mother Nature is going to keep making things smaller and smaller, which favors SI, and we can't breed the SI gurus fast enough. We have to figure out how to simplify the first order to get you 80% there.

Westerhoff: We've been talking about simulation and modeling for as long as EDA has existed, assuming that the design community

would keep pace if we could provide tools with the right capabilities. In the SI space, at least, the shortage of experts isn't getting better, and it's time to do something different. We have tools for the experts; now, we need tools for the broader community and examples of how to apply those tools to common design problems.

We provide user workshops that show how to apply HyperLynx to a typical design problem. My point here is that training and education are just as important as the tool capabilities themselves, especially when we're talking about a broad audience. We've been conditioned to think about which things are critical when analyzing a high-speed serial link, but most of our input has come from people practicing at the state of the art. In our 25-gigabit serial link workshop, for example, the effect of surface roughness just doesn't matter that much. It's case-dependent, of course, but that's the point. Showing people how to isolate and quantify the different things that affect system margin is every bit as important as having the capability to do that analysis. How are people supposed to know what to do if you don't show them?

We all have these ideas about what matters and what doesn't based on what we've been told, but sometimes the actual results are quite surprising, providing additional opportunities to optimize a design.

Holden: The overall truth is that two things are conspiring against us. The first one is the schedule. Nobody's going to let us expand the schedule. They constantly seem to shrink because of time to market and who gets there first. The second thing is complexity. To attract customers, everything has to have more features and be more complex.

Johnson: You're absolutely right in terms of schedule. If you bring basic analysis to the desk of the engineer, you helped your schedule by a large amount. If you can put basic tools in that designer's hands, they can make a lot of those decisions. You'll actually win some on schedule there.

Westerhoff: I think it's a diminishing return problem. How much can we accomplish if our analysis accuracy is at the 90% level? A lot. If we defer all analysis until the end of the design, we run the risk of finding mistakes that will blow the schedule. When it comes to design analysis, we're saying less is effectively more.

Shaughnessy: Less information available quickly is better than 100% of the info two weeks from now.

Westerhoff: Exactly. Let's be clear; we're not saying that we don't need SI experts doing what they're already doing because we do. We're arguing that most designs have an "analysis valley" in the middle of the design cycle, where systems designers can't get the feedback that they need. Putting design-oriented analysis tools in their hands will enable them to make more informed design decisions and help offload the SI experts from what is probably the worst part of their jobs, running post-layout verification on other people's designs.

Holden: Mentor and Siemens have access to much of the electronic design space. Do you work with the thermal analysis or placement and routing side teams to help designers juggle the multiple balls that have to be kept in the air?

Westerhoff: Absolutely. That's a natural extension of everything that we've discussed here. The problem isn't unidimensional anymore; it requires balancing electrical, mechanical, and thermal trade-offs. How do you extend this design-oriented analysis strategy to play across all those disciplines? That's where we need to go next. Perhaps we can talk about that the next time we meet.

Shaughnessy: This has been really interesting, Todd. We appreciate your time. Maybe we'll see each other "live" again.

Westerhoff: Thanks for the discussion. This has been great. It will be nice to talk in person again. **DESIGN007**

Fringing Fields

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Electromagnetic energy is all around us from TV to radio and communication waves and the Earth's magnetic field and plasma shield that protect us from the sun's solar flares (Figure 1). This activity is driven by the sun's magnetic field. Like all physical phenomena, they tend to follow the same rules.

A parallel plate capacitor (or a planar pair) has two conductors separated by a dielectric layer. Most of the energy in the structure is concentrated directly between the plates. However, some of the energy spills over into the area outside the plates. The electric field lines associated with this effect are called fringing fields. In this month's column, I will look at how electromagnetic radiation can be emitted from the edges of planes in multilayer PCBs by the fringing fields, possibly causing electromagnetic compatibility (EMC) issues.

Fringing is the bending of the electric flux lines near the edge of the parallel plate capacitors. Fringing is also known as the edge effect. Normally, the flux lines inside the capacitor are uniform and parallel. But at the edges, the flux lines are not straight and bend slightly outward due to the geometry. Also, in a plane pair, signals passing through the cavity may intensify fringing fields (Figure 2).

When the return current flows through the impedance of a cavity between two planes, it generates voltage. Although quite small (typically in the order of 5 mV), the accumulated

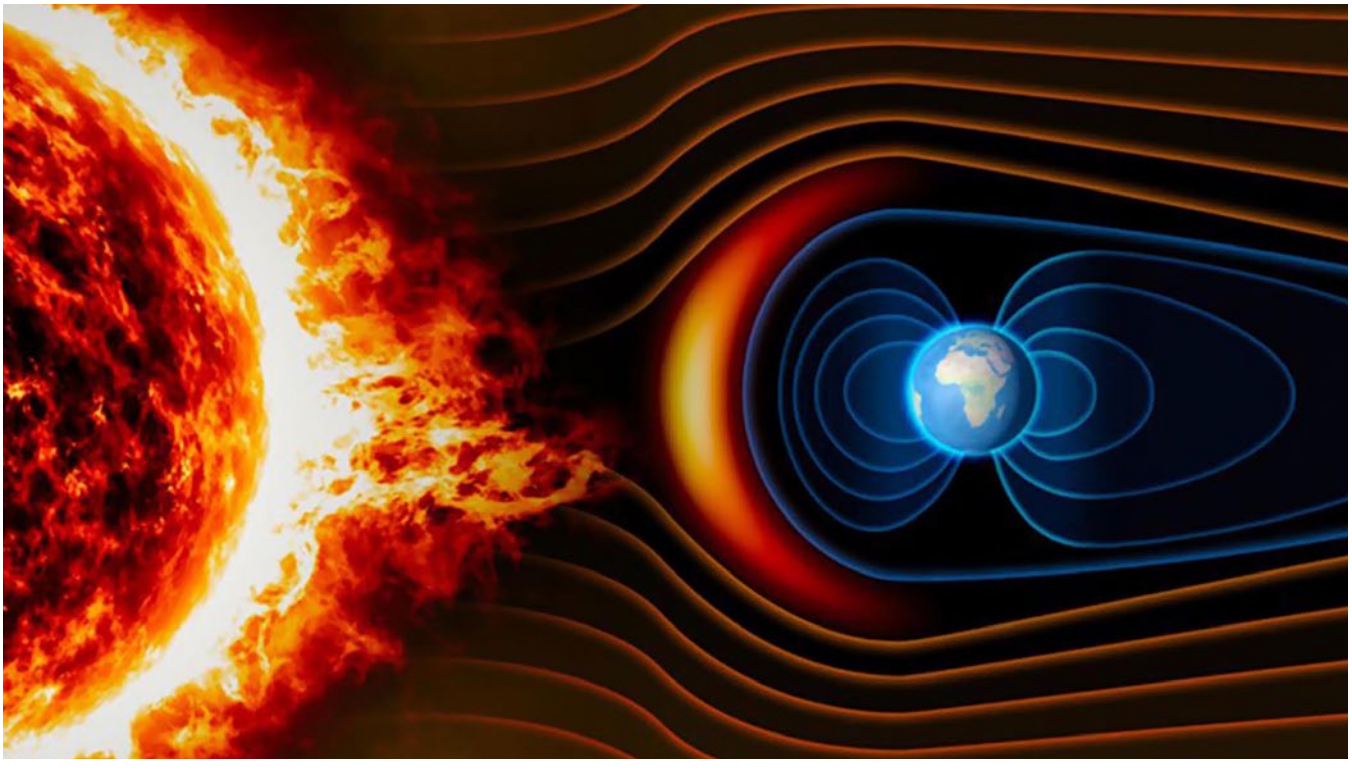

Figure 1: The sun's corona discharge (solar flare) and Earth's magnetic field.

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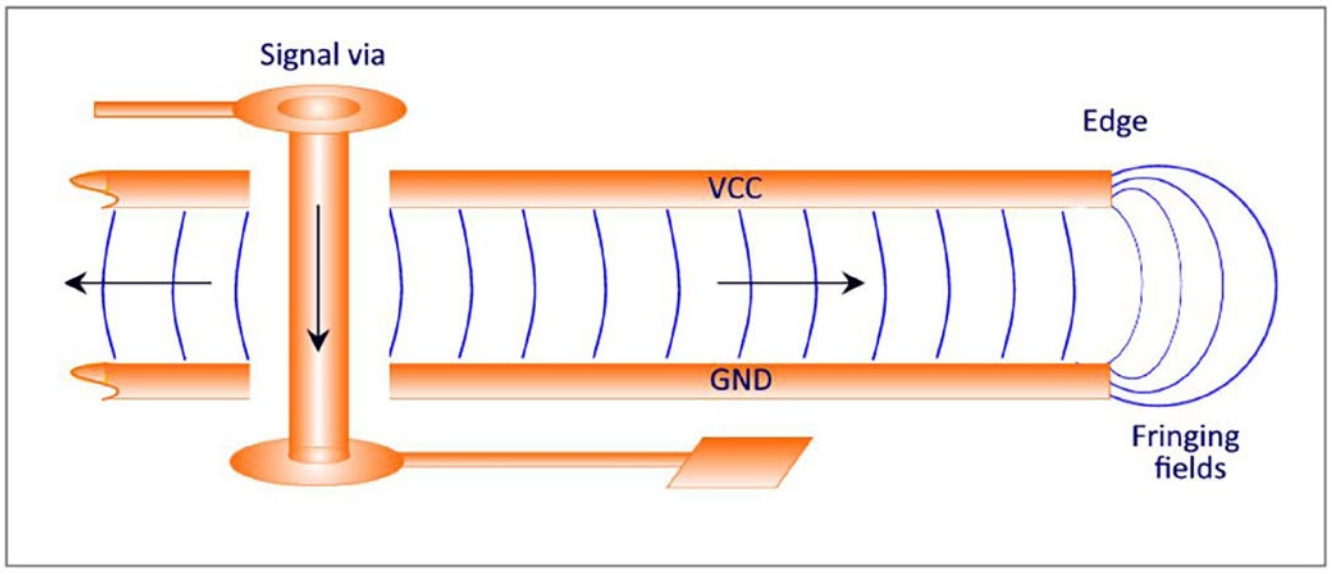

Figure 2: Signals passing through a plane cavity intensify fringing fields.

noise from simultaneous switching devices can become significant. Unfortunately, as core voltages drop, noise margins become tighter. This voltage, emanating from the vicinity of the signal via, injects a propagating wave into the cavity, which can excite the cavity resonances or any other parallel structure (for instance, between copper pours over planes). Other signal vias, also passing through this cavity, can pick up this transient voltage as crosstalk. And when the wave meets the PCB edge, the two reference planes form a slot antenna and will radiate noise with the potential to generate electromagnetic interference (EMI) to nearby equipment.

The more switching signals that pass through the cavity, the more noise is induced into other signals; it affects vias all over the cavity, not just the ones in close proximity to the aggressor signal vias. This cavity noise propagates as standing waves, spreading across the entire plane pair. This is the primary mechanism by which high-frequency noise is injected into cavities by signals transitioning through cavities, using each plane successively as the signal return path.

Cavity resonance also affects the power/signal return layers at the edges of the PCB. Edge effects can be particularly problematic since it is the board edges that are in such close proximity to the chassis; hence, the radiation fields can induce currents into the chassis frame.

When the cavity has open end boundary conditions, resonances arise when a multiple of half wavelengths can fit between the ends of the cavity. Figure 3 shows the cavity resonance of a plane pair with a resonant frequency of 1 GHz. If the signal clock frequency (or harmonics) are multiples of 1 GHz, then noise can be injected into the plane cavity. When the clock or data harmonics overlap with the cavity resonant frequencies, there is the potential for long-range coupling between any signals that run through the cavity. This is one reason

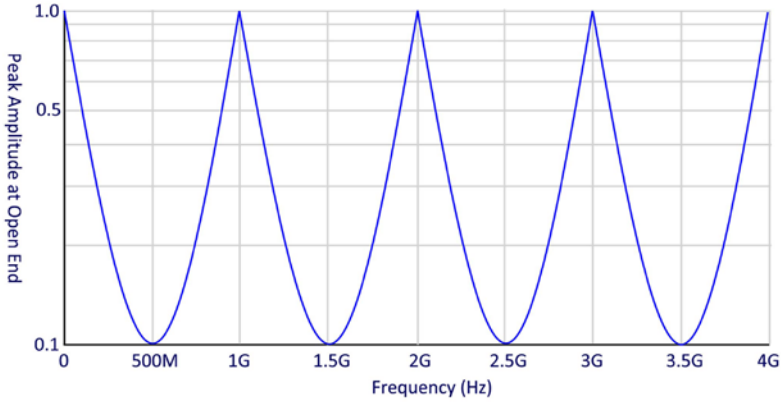

Figure 3: Amplitude at the far end of planes as input frequency is swept. (Source: Eric Bogatin)

why all return planes should be GND layers so that stitching vias between GND planes can be placed adjacent to each signal via transition to minimize the possibility of exciting the cavity resonance.

Cavity resonances are (at first) a signal integrity issue, but the amplification of cavity resonance excited by fast rise time signals at high frequencies can also contribute to electromagnetic emissions. The frequency components of the voltage noise are related to the peak impedance of the cavity and the frequency components of the return currents. In any complex system, with typical interconnect density, avoiding signal layer transitions is not practicable and is an issue that designers must live with. However, one can learn to avoid injecting excessive noise into the cavity or at least minimize the impact.

Figure 4 gives an example of a signal trace on the top microstrip layer routed outside the reference plane area. I see this all the time when I analyze PCBs. The signal path is very close to the edge of the PCB, and the reference planes are not located directly under the trace to provide full field coverage. The electric fields (blue) tend to couple to the plane edges, whereas the magnetic fields (red) radiate outward omnidirectionally. The fringing effect

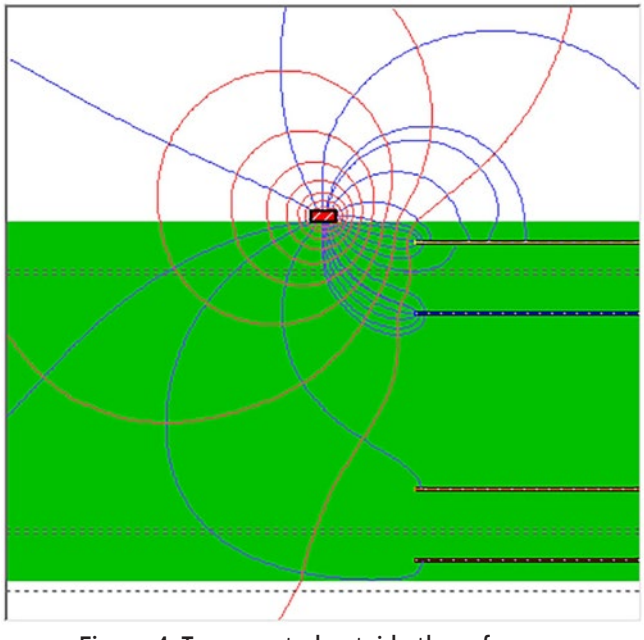

Figure 4: Trace routed outside the reference plane area (simulated in HyperLynx).

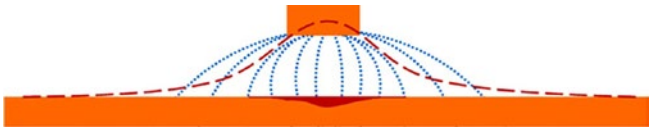

Figure 5: Microstrip plane return current distribution.

creates a very "hot" area and will radiate and possibly create coupling issues to nearby circuits, cables, and slots in enclosures.

Figure 5 illustrates the cross-section on a microstrip trace, and its associated plane return current distribution (red). Where the electric fields (blue) are more tightly coupled to the plane directly below the trace, the return current also exhibits tighter coupling. But where the field spreads out from the trace, the larger loop area between the signal and the return current path increases the inductance.

Return current tends to couple to the signal conductor, falling off in intensity, with the square of increased distance. A stripline (inner layer) return current distribution is narrower with the fields more intense above and below the trace. The electric field spreads out to approximately three times the width of the trace (on both sides), so it is important to ensure there is enough plane coverage to prevent radiation.

To reduce emissions and increase immunity, when routing a PCB, try to avoid positioning critical signals close to the edge of the board. This creates a more robust system for electromagnetic compatibility.

There are various approaches pertaining to reducing radiation edge effects from the PCB. In many cases, energy can be reflected, possibly creating additional internal cavity resonance effects and coupling to internal vias, also resulting in increased radiation. When plane pairs resonate, their emissions come from the fringing fields at the board edges. With ground/power plane pairs, edge-fired emissions can be reduced by reducing the plane separation and lowering the AC impedance. Alternatively, make the power planes slightly smaller (~ 200 mils) than the GND plane. This modifies the pattern of the fringing fields, pulling them back from the edge, and may help reduce emissions to some extent.

Edge plating, as the name suggests, is the process of plating the edges around the PCB. I first saw this technique used at NEC back in 1994. This is an elegant (but expensive) solution to prevent emissions from extremely high-speed SERDES signals on terabit routers, etc. but is an overkill for a typical high-speed design.

Another way to mitigate this problem is to create a via fence stitched to ground around the perimeter of the PCB. If the spacing between the stitching vias is less than or equal to one-eighth of a wavelength, the via fencing will appear as a short circuit, causing the propagating wave to be reflected back to the source rather than being launched from the PCB edge.

A post-production solution is to employ cavity resonance absorber material applied along the edge of the PCB, which dissipates the edge radiation from the PCB without using additional board real estate. It also reduces the possibility of board resonance problems by dissipating the energy and not reflecting the energy back into the interior of the board. However, it is always best to fix the problem at the source rather than applying as a quick fix after production.

Key Points

- Fringing is the bending of the electric flux lines near the edge of the parallel plate capacitors.
- A signal passing through a plane cavity may intensify fringing fields.
- As core voltages drop, noise margins become tighter.
- Signals passing through a plane cavity inject propagating waves, which can excite the cavity resonances.
- When the wave meets the PCB edge, the two reference planes form a slot antenna and will radiate noise.
- The cavity noise propagates as standing waves spreading across the entire plane pair.
- When the cavity has open end boundary conditions, resonances arise when a multiple of half wavelengths can fit between the ends of the cavity.
- Return current tends to couple to the signal conductor, falling off in intensity with the square of increased distance.
- Avoid positioning critical signals close to the edge of the board.
- Edge plating is an elegant (but expensive) solution to prevent emissions from extremely high-speed SERDES signals.
- GND stitching vias are placed at one-eighth of a wavelength as a short circuit, causing the propagating wave to be reflected back to the source.
- Edge radiation should be eliminated at the source. **DESIGN007**

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- Barry Olney, "Beyond Design: Plane Cavity Resonance," *The PCB Design Magazine,* September 2017.
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- Barry Olney, "Beyond Design: The 10 Fundamental Rules of High-Speed PCB Design, Part 3," *Design007 Magazine,* November 2018.
- Basu (VU2NSB), "Solar Activity and Ionosphere," VU2NSB, November 19, 2019.
- Arturo Mediano, "Avoid Critical Signals in Edges of the PCB" In Compliance, December 27, 2018.
- Bert Simonovich, "Controlling Electromagnetic Emissions From PCB Edges in Backplanes," *Signal Integrity Journal,* January 18, 2017.
- Mast Technologies, "Reducing PCB Edge Fringing."
- Larry D. Smith and Eric Bogatin, *Principles of Power Integrity for PDN Design—Simplified,* Pearson, March 2017.
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Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at icd.com.au. To read past columns or contact Olney, click here.

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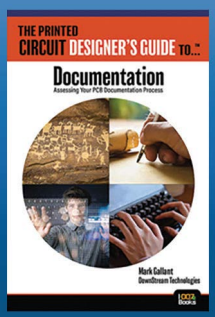

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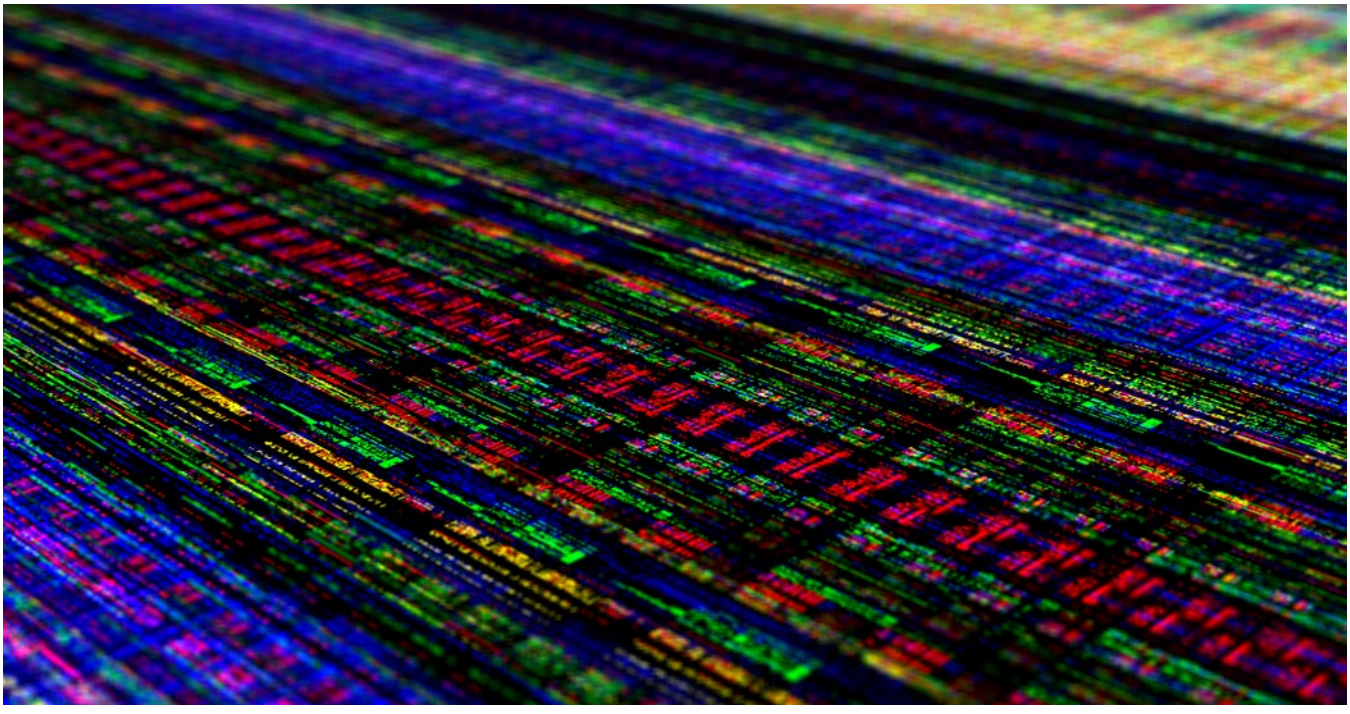


How Designers Can Help Facilitate Co-Design

Feature Interview by the I-Connect007 Editorial Team

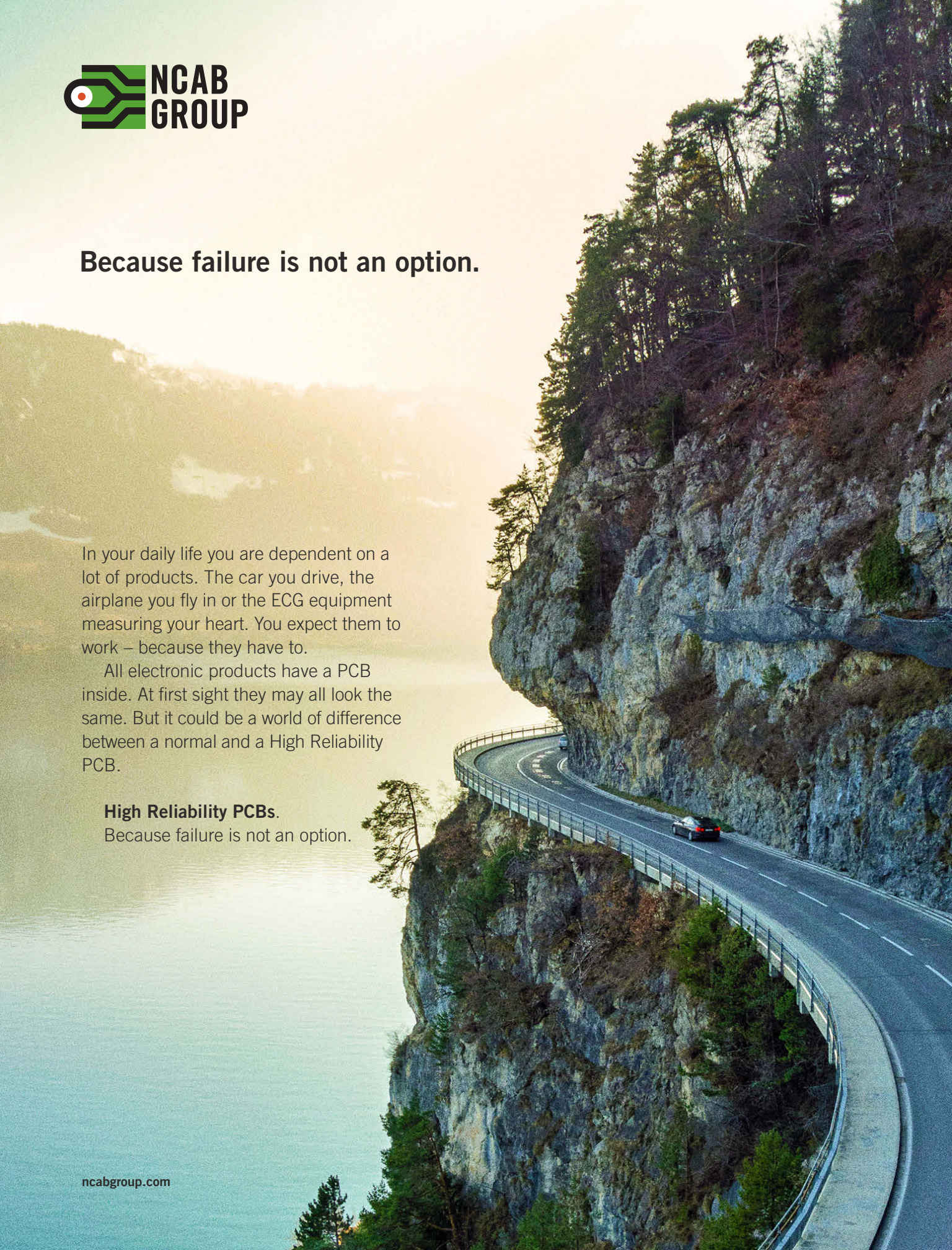
José E. Schutt-Ainé is an electrical and computer engineering professor at the University of Illinois, Urbana-Champaign, and a contributor to the Heterogeneous Integration Roadmap (HIR). In this conversation, José gives Nolan Johnson and Andy Shaughnessy an overview of the co-design chapter he co-authored in the HIR, the motivations behind advances in co-design, and why designers are the real drivers who must decide what is needed in EDA tools to facilitate the process of co-design.

Nolan Johnson: José, start by telling us what chapter of the HIR you were involved with.

José Schutt-Ainé: I was involved with Chapter 13, which is the co-design chapter, and that is supposed to be an extension of the modeling and simulation chapter. Initially, the co-design effort was part of the modeling and simulation, but we decided that in the context of heterogeneous integration, it had to be taken separately.

We look into the traditional methods that have been in use for co-design. We need to think about what's going to happen in the next 10–20 years and how co-design will affect future types of designs like neuromorphic computers or quantum computing, etc. We start with the traditional co-design methods, and we discuss what the challenges are. Co-design involves putting together different types of simulation tools. Placement and routing are very different than electromagnetic instruction, which is very different from circuit simulation.

How do you get these tools to talk to each other in optimizing a design? We also look at the domains, the chip, package, and board. How do they coexist? How do you transmit information from one domain to the other in a seamless manner? And how is it done traditionally? We looked at that, and then this led to pathfinding, which is considered as the ultimate method for doing co-design. Pathfinding not only optimizes the design itself, but it also looks at other considerations, such as cost and performance. We had a section devoted to that. We also looked at the impact of co-design and architecture. How do you want to design your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computer in the future? How do you want to manage issues related to cache, memory, and processing? For each of these sections, we had different experts write various sections.

After that, we move to the future technologies like silicon photonics. How is that going to be affected by co-design? How can co-design improve silicon photonics? The more futuristic stuff was at the end of the chapter, where we addressed things like neuromorphic computers and quantum computing because they definitely will necessitate some type of co-design for their inception.

Shaughnessy: In the co-design chapter, you all talk about how EDA tool vendors now offer PCB design tools with packaging design functionality. Do you see that more often?

Schutt-Ainé: It all depends on who you talk to. What is heterogeneous integration? People think that Moore's law is going to run out of steam eventually. This whole idea of getting a new node every 18 months, people anticipate that at some point, it's going to come to a halt. Instead of cramming more components into one chip, you're going to have more creative methods for combining not only the different domains but also various levels—namely package, chip, and the board—and technologies. How do you combine them?

What is heterogeneous integration? People think that Moore's law is going to run out of steam eventually.

What happens in optics is not necessarily compliant to Moore's law. At the same time, when you look at what happens at the PCB level, the components will scale according to the wavelength but not the technology. Things get smaller only as the frequency goes up. It's like you're dealing with different rules, and that's the whole idea. That's the impetus behind heterogeneous integration.

However, last December, I was at a conference in Taiwan, and that's where TSMC is. They don't seem to buy into HIR with the same level of enthusiasm as people do in other places, like they do in the U.S. In Taiwan, people really believe in Moore's law. According to them, when Moore's law stops, the impact on their economy will be quite visible.

Shaughnessy: One section explains how simulation has to move from a 2D view to 3D.

Schutt-Ainé: For instance, with 3D chips, there's a whole host of issues coming as a result of the third dimension. The thermal issues are going to become more serious. In the first version of our chapter, we did not have the electrical-thermal aspect included, but we just included that last month. The next version of the chapter will include a whole section on electrical-thermal co-design, and it touches on issues related to 3D. Removing the heat on the treated chips is a big challenge. Modeling is also a challenge.

Johnson: Depending on what you load inside, the package is going to change the thermal characteristics, which you then need to accommodate on the PCB. There's a lot happening.

Schutt-Ainé: I look at co-design as an enabler of heterogeneous integration. Our focus is more on what the EDA companies should be doing. What kind of tools should they be making available to the designers? It's a difficult task because you're looking at combining very different types of algorithms. There's also the database. How do you manage the information? The chip information is managed in one way, and the database is usually managed in a certain format. The package level is in yet a different format, and then there's the board level. How do you make all of that? How do you ensure good communication between the three different levels?

On the circuit side, you start with Maxwell's equations to help predict how the waves are

going to be interacting with the components. On the other side, you have placement and routing algorithms that have nothing to do with physics, but rely more on math principles such as statistics and graph theory. How do you optimize the placement? All of those things have to work together, which is the challenge.

In the end, you have your package that you place on an EDA tool. You put it on a tool like the major vendors. They get that. As of now, they have some offerings, but we're working on the roadmap. We're trying to figure out what it is that's going to be needed in the next 10–20 years. What they're doing now is more to satisfy the current needs of their customers.

Johnson: That's one of the places where the roadmap makes sense. That may not be the best way to frame the question. But one of the reasons for the roadmap is to give a long-term vision to part of the industry, such as the CAD tool sector, to help them understand what it is they need to put in with staff for development. What has the response been so far?

Schutt-Ainé: My experience is limited as far as my interactions with the EDA people, but they are very customer-driven. If you come up with a new idea, such as, "Here is this thing that you could use to design a quantum computer," they probably would not be excited by something like that because they don't have any customers right now that have that demand. They are always more excited by what customers are asking for. I don't know how you fix that, but most of what they put out is based on customer demand.

For instance, machine learning is a very exciting discipline right now in academia, especially for design. But it's a difficult sell to the EDA vendors because they're not getting that request from the consumers, from the customers. They tend to want more traditional things. It has always been my experience. Usually, that comes from the demand that they get from the customers.

Johnson: The readership that should create the demand for your audience is probably reading Chapters 5, 6, and 7 around the application. This is where things start to dovetail. How do you coordinate those messages in the roadmap with your messages?

Schutt-Ainé: What would trigger the EDA vendors to get more on board is if you had the actual manufacturers and designers of these futuristic systems putting things together, saying, "We need a tool to do that." Let's say you want to do an optical SerDes working 56 gigabits per second or even higher. They're talking about 128 gigahertz per second. I don't think that you have a commercial tool that can do that, especially if it combines optical with electrical components. But if you have an active program or designer looking into doing it and there's a budget for it, that would get the EDA vendors on board.


José Schutt-Ainé

Shaughnessy: One thing you pointed out was that everything, including simple things like the data formats and types for packages and boards, is completely different than those used at the IC level.

Schutt-Ainé: PCB designers also have to learn about electromagnetics. The clock rates are getting faster, and the end result is that the signal that goes to your PCB is more like a microwave signal. Component dimensions are comparable to the wavelength, which means that the wire is not just a simple wire; it's a transmission line. The physics are completely different because it behaves like a wave. In the mid-'90s, I traveled a lot, giving basic electromagnetic courses to PCB designers. They didn't worry about that in the '70 or '80s because the clock rates then were relatively slow. Things started changing in the late 1980s. At the same time, they were working on things where the clock rates were approach-

ing the gigahertz range. You had to think of everything as transmission lines.

Shaughnessy: When top PCB design instructors like Rick Hartley, Lee Ritchey, and Eric Bogatin teach, they say every wire and every trace is a transmission line, and you have to put it that way, or you'll be out of luck. With the rise times and speeds, everything is so fast, and there is no leeway.

Schutt-Ainé: But that's more at the PCB or package level. The chip is a different story because everything is so small. You don't worry too much about inductance or radiation or antenna type problems. The chip is going to be mounted on your package, and the chip is going to be running really fast.

Shaughnessy: It seems like it's even more of this system-level awareness. Almost everybody involved in designing or building a circuit board must have a system-level outlook, or they're not going to be able to make all the right decisions.

Schutt-Ainé: And it's going to become harder. In the course I teach, I always give the student this perspective. Look at a cellphone, for instance. With a typical design, back in the day, the voltage was 12 volts, and then it went to five volts, then to 3.6, 1.8, and 1.2. Now, it's coming down to even lower than one volt. The reason you're lowering the DC supply voltage is that you want low power, long battery life, and low power dissipation. But it makes the job a lot harder for the designer because the voltage budget is now very small. You need to have everything done within one volt. Even with a 0.6-volt drop, just running from the power supply to the power rail is bad news.

Johnson: Let's transition to talking about your presentation.

Schutt-Ainé: Sure. This is a modified version of the webinar that I gave two months ago as a chapter overview. We've had some discussions about the motivations for co-design, and as we outline the application, the designers are the drivers. They have to decide what is needed in those tools to somewhat facilitate the process of co-design, such as data centers, IoT, automotive, etc., and especially things like SerDes and high-speed links. I highlighted those two because a lot of what I do in my research relates to these applications. The way our technical working group was structured is we wanted the chapter to address some of the questions listed. What is the state of the art in co-design? What will drive the creation of these tools? What will the challenges be? How much value will having co-design tools add to HIR? How will all of this happen in the next five to 10 years?

Traditionally, co-design is how you manage the chip, package, and board together. The chip level is very different than the package or the board. At the chip level, you worry about transistors, and their operation is highly nonlinear. MOSFETs are nonlinear devices, and with the tools used for verification like SPICE, it's important to notice that the scaling takes place with technology. Essentially, they follow Moore's law. By contrast, with the package into the board level where things don't follow Moore's law, the scaling happens with the electromagnetic wavelength.

Going to the board level, it is very similar to what you get at the package level, but you get additional tools because the dimensions are higher, so the electromagnetic extraction tools become more important. Given the fact that you may be dealing with different types of chips from different vendors, you need to have a way of handling the nonlinearities. For instance, the IC's form has come into play.

The goal is to combine all these domains and develop a successful flow. People talk about vertical or horizontal co-design, but the vertical one is when you go from one domain to the other. Co-design is when you make sure you are aware of many different constraints. You're going from chip to package to board, but you are also incorporating constraints related to security, test, and thermal. All of those also have to be integrated, which will make the process a lot more complicated.


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Traditional co-design requires trade-offs. You need to be aware of what those are, and you need to understand the trade-off at the chip level, as well as how it will impact the implementation at the package level. I've talked about formats, translations, and domains, which are important, too. How do you propagate information? If you have mapping at the chip level, what is that going to correspond to—the package or the BGA? Being able to propagate the information properly is part of the challenge. Managing connectivity is somewhat related. We also talked about the database format. We're looking at the board, package, and chip, all of that has to be done in a seamless fashion.

We're looking at the board, package, and chip, all of that has to be done in a seamless fashion.

We also identified other challenges, such as multi-physics, thermal awareness, and mechanical constraints. Sometimes, you combine electrical with optical. The idea is that these are different domains where the scales and resolutions related to physics are very different. What's big in the optical domain may end up being very small in the microwave or electrical domain. And the design rules are different. One thing you will observe is that the tools are old and slow, meaning how long it takes to develop new algorithms is a lot longer than how quickly new technologies come into play. Some of the proposed solutions have been somewhat successful, such as behavioral and macro modeling. I talked a little bit about that earlier when I mentioned model order reduction. This has been quite successful in reducing complexity.

Statistical modeling is also helpful because, given the fact that the performance of these systems is highly sensitive with respect to small variations, the best way to handle those is really to perform statistical analysis. We talked about AI, and although we're looking at quantum computing as a potential application to co-design, if quantum computing ever becomes a reality, it could facilitate co-design.

One slide shows how things have evolved over the past 20–30 years. In the old days, wire on a PCB used to be considered as a simple capacitor. But as the clock rates increased, you had to use that same wire at that same channel that had to be treated differently. Over the years, the tools had to implement transmission line simulators in order to describe how a signal travels from point A to point B. Today, a channel is even more complicated because, in addition to transmitting the information from point A to point B, you also have to provide equalization.

When you clock in at a very high speed, the nature of the channel is much more complex than the simple wire. A good example is the SerDes. Imagine having two chips that are mounted on the board, and the two chips both have 256 pins. You're not going to be able to connect 256 pins from one chip to the 256 of the second chip. What do you do? You need to use a SerDes, and you need to somewhat select those wires and serialize them. You take them 16 at a time, and you use only one wire to transmit the information from those 16 pins. This means that you need to multiplex the information, serialize it, transmit it, and then de-serialize it when it arrives at the other end. Consequently, transmission must be done 16 times faster. That's a design of SerDes that is a very complex and demanding operation. Yet people have them working at these speeds, like 12.8, 4.4, and 25.6 terabits per second for the optical implementation. It's very ambitious.

Then, there's placement and routing. Again, this is a very different world because it has nothing to do with modeling and simulation; it has to do with optimizing how you're going to lay out your system. Where should the bumps be placed? Where would we expect to put the gate, and what's the best way of rerouting the wires? Placement and routing are very differ-

ent for me, and modeling and circuit simulation are a different game. We're talking about using Maxwell's equations to extract the electrical components of the system, as well as using circuit theory to predict how the voltages and the currents are going to behave on a circuit that typically may have tens of millions of transistors. That's the challenge.

That's where pathfinding comes into play. Pathfinding is the solution to co-design in the sense that once you put everything together, you have something that you can refer to as a pathfinding methodology. Some of the things it will do include unified workflow, partitioning, floor planning, the capability to create the abstract package models, etc. As you optimize the process, you also optimize the cost. Somehow, the cost has to be thrown in, and the knowledge of the existing technologies that are available to you must be implemented in the pathfinding methodology, as well as enabling the interaction of the design tools from the different EDA vendors.

Those are the key components that we examined. There's also a new section added for thermal-aware co-design. We have a section on co-design for architecture and silicon photonics. We also have this matrix that describes the interaction between the different chapters, which is very important.

The presentation also shows what the priorities are. We come from the simulation group, so co-design must have a tight interaction with simulation, and then there's IoT, 5G, and RF. Automotive co-design can play a major role.

Shaughnessy: This has been very helpful. Thank you for your time and insights, José.

Schutt-Ainé: I'm glad to know you find it useful. The difficulty with putting this together is that most of us are experts in only one discipline, so trying to assemble a group of experts to write on co-design is hard. In my case, I don't know much about placement and routing, so I had help from co-writers. **DESIGN007**

Purdue Team's PCB Design Improves Electric Guitars

What makes a guitar electric? With a skilled person playing, any performance can be powerful, but for the moment, consider the mechanical aspects of the instrument itself.

Traditional electric guitars have a "pickup," a magnetic transducer made with miles of copper wire coiled around magnets via a tedious, time-consuming process.

Purdue Polytechnic's Davin Huston and Mark French, along with Kathryn Smith, a former graduate student in Huston's lab, have been studying ways to improve the process, making the finished products better for both players and manufacturers. They created a flexible, printed circuit board that imitates the conventional copper wire configurations inside electric guitars.

"We came up with a new approach to the electric guitar pickup, the magnetic transducer that helps create the musical sound," said Davin Huston, assistant professor of practice in engineering technology. "Our circuit boards can be printed in large quantities and fit inside just about any electric guitar, which simplifies the manufacturing process but keeps the sound quality and reliability."

With a conventional electric guitar pickup, string vibrations cause the electromagnetic field to oscillate, induce a voltage in the coil, and generate an electric signal. The team's circuit board works the same way.

"With typical pickups, the wire coils often produce undesired feedback and need to be potted with wax or a polymer," said French, professor of mechanical engineering technology. "Our circuit board provides an alternative that is easier to produce with manufactured consistency."

Davin, French and Smith worked with the Purdue Research Foundation Office of Technology Commercialization to patent the technology. A U.S. patent has been granted. (Source: Purdue Polytechnic)

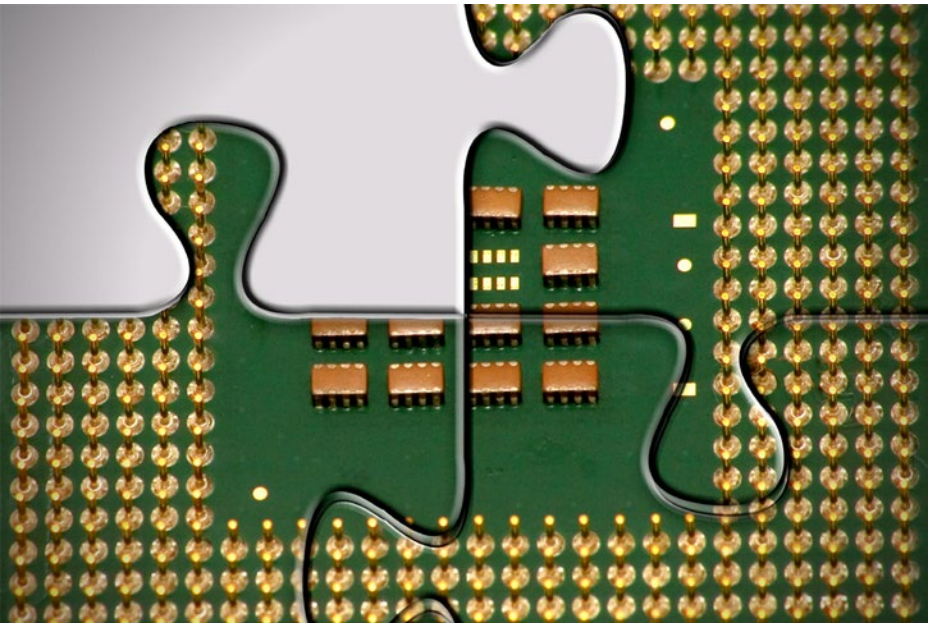
Unraveling the Mysterious BGA Routing Mess

Connect the Dots

by Bob Tise and Matt Stevenson, SUNSTONE CIRCUITS

A ball grid array (BGA) device can be a daunting component to route, especially in fine-pitch arrays featuring solder ball counts in the hundreds and pitch values as tight as 0.5 millimeters. With so much new technology requiring high-functioning processors and boards in increasingly miniaturized devices, it's safe to say higher pin density, reduced lead inductance, and finer-pitch BGA devices will become even more common in our industry.

That means the foreseeable status quo will be less and less space to route traces and vias between pins. BGAs represent a challenge from design through prototyping and manufacturing, but with some sharp attention to detail and a plan focused on best practices, this is by no means an impossible task. Let's look at how you can take the mystery out of BGA routing and create a PCB design that can handle all those pesky narrow spaces.



Start With a Little Research

BGAs have been around a while, so there are many resources available to provide some guidance and help you not to reinvent the wheel. There are some good online resources that can be very helpful, such as YouTube videos, blog posts, and technical papers. Most of these resources are free to access, leaving you to sift through the marketing noise and extract available learning that will be useful to you.

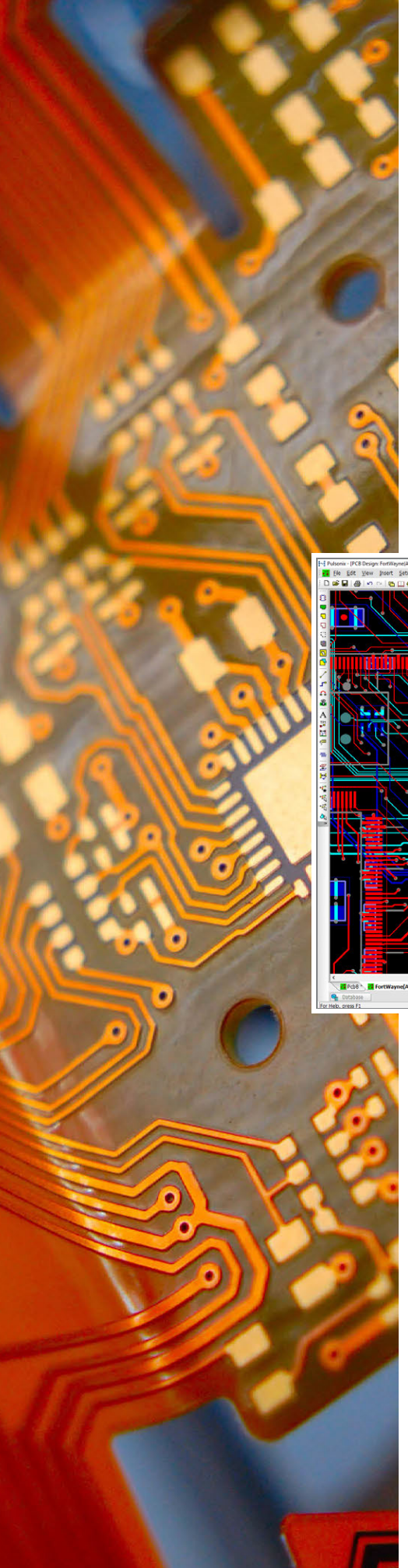
Know Where Trouble Can Lurk

Solder joints are where you really need to mind your Ps and Qs. Smaller surface areas reduce the strength of the solder connection and increase the risk of fracture. Thermal issues can create flex between the component and board and put additional stress on the solder joints. Keep this in mind as you conduct research into BGA best practices.

Vet Your Information Sources

Device manufacturers will often have helpful information on their websites, such as routing examples and land patterns. Typically, the part manufacturer's footprint is optimized for soldering the part to the board but can leave you with an impossible routing solution. It's important to learn when to follow their guidance and when to improvise in the name of manufacturability and functionality.

In most cases, it's acceptable to reduce the BGA pad size sufficiently to allow for vias between



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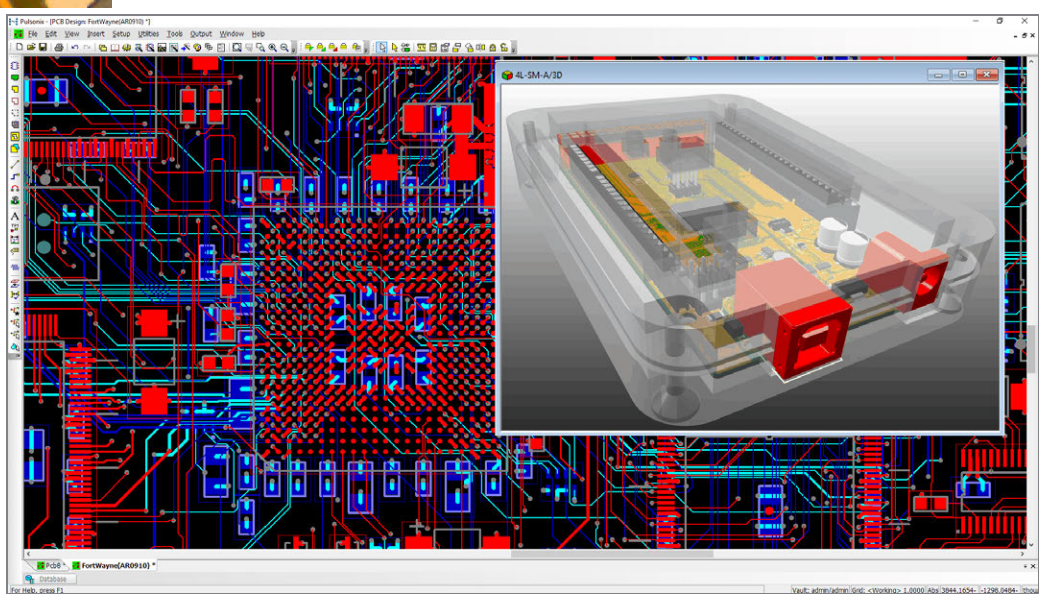

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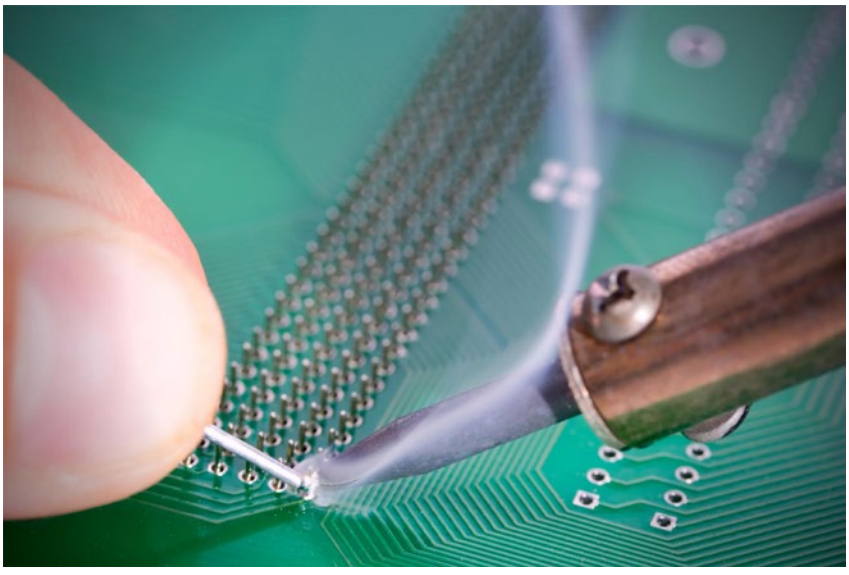


Figure 1: BGA solder.

the BGA pads. Typically, the BGA pad can be reduced to the same diameter as the BGA ball (nominal dimension) shown on the component datasheet.

Planning Is Key

BGAs of any size require a lot of room around them for all the wires and vias you will need to effectively make all the desired connections. Different board patterns will need optimal fan-outs or escape routing tailored to fit them. Examine each pattern carefully, scrutinizing spacing between solder balls, confirming whether they are parallel and equidistant or have greater spacing in one direction, and establishing minimum trace width and spacing (Figure 1).

Make sure that the critical signal paths and decoupling capacitors are well situated to maintain signal integrity and reduce inductance. Starting with the via escapes and fan-outs, keep some tried and true tricks in mind, such as high aspect ratio vias, micro-vias, or buried vias that will allow you to utilize real estate on all layers. These can be especially critical in the very large and fine pitch devices. Traces required to route between these pads and vias also can be reduced to provide an escape. You may need to use traces and spaces considerably smaller than the rest of the board in this case.

Adding signal layers is another trick to effective routing. Typically, one signal layer is needed for every two rows of pins, but if the BGA pitch is below 0.8 mm, you will need one signal layer per row. Keep in mind that increasing layers can be a relatively simple way to route the traces, but it can also increase the cost of the board and open the door for reliability issues. In many cases, it's probably worth evaluating whether a change to your layout can reduce the layer requirements.

Pro Tip

Make sure that you are working with a PCB manufacturer up front and understand their capabilities, especially as it relates to these aspects for the BGA routing. It is never fun to spend a lot of time on a design and then find out your preferred vendor simply cannot manufacture it.

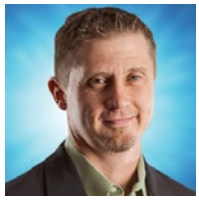
Use Your Design Tool

Many of the design tools today have functions to help make you more successful in your design efforts. Explore some of these functions and use them when they make the most sense for your design. Often, you can assign specific rules around your BGA that may differ from the rest of the board, saving you the time and effort of doing it on a trace by trace basis.

Good luck! Remember these best practices, and you too can make friends with the mysterious BGA. **DESIGN007**

Bob Tise is an engineer at Sunstone Circuits, and **Matt Stevenson** is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Tise and Stevenson, click here.

Bob Tise



Matt Stevenson

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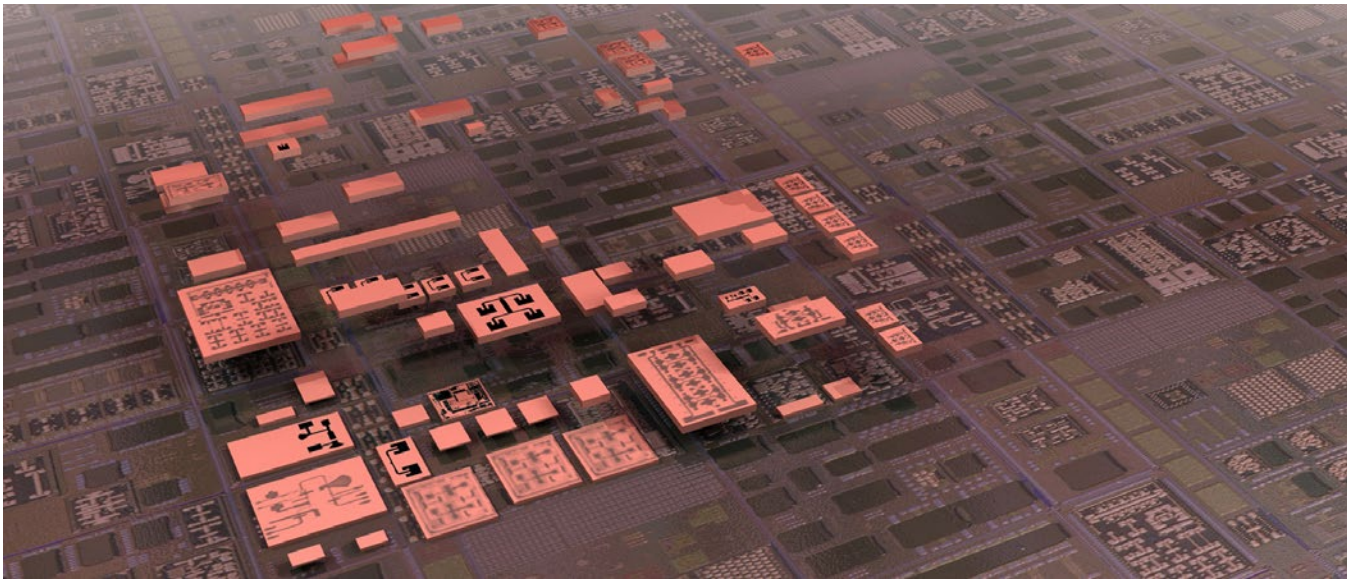


IEEE's Heterogeneous Integration Roadmap, Part 2

Feature Interview by the I-Connect007 Editorial Team

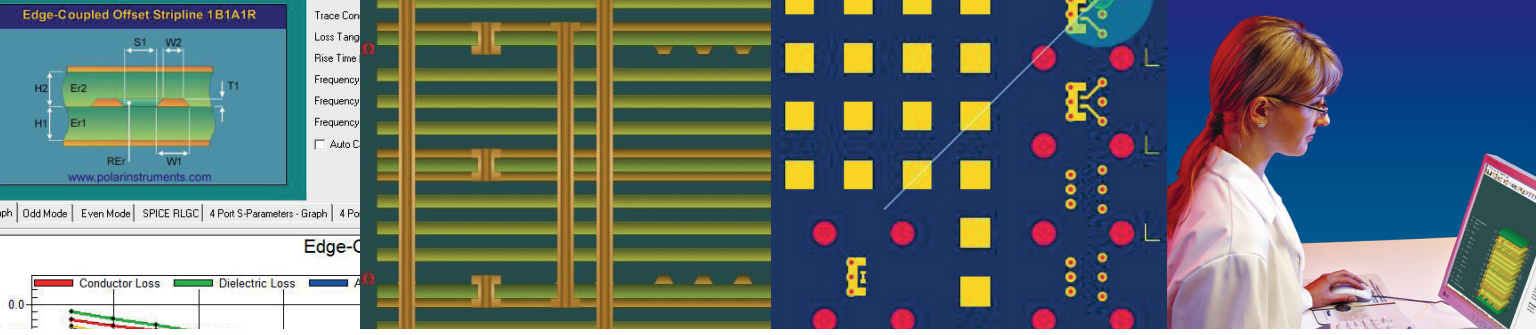
In Part 1 of this conversation from *SMT007 Magazine,* Rita Horner of Synopsys provided a general overview of the IEEE Heterogeneous Integration Roadmap (HIR)—a document that provides guidance for IC, PCB, and package designers, broken down by industry segment and performance requirements. In Part 2, Rita shares her perspective from the IC side, as well as how the HIR might affect what happens on the PCB design and manufacturing side in the next few years.

Nolan Johnson: You're working at Synopsys on multi-chip integration in a package EDA product. Compare and contrast the difference between multi-chip products today and where the HIR will take us. How is it different?

Rita Horner: As you mentioned, the HIR covers many grounds, and it's not just one market or application space. It's hard to just generalize that. I talked about technology limitations, but there is an economic aspect of it because it's not cheap to make these devices. Even a monolithic die in a package is expensive when it's complex and large in the advanced technology nodes today, such as five nanometers or smaller. When you're not getting the yield, it's going to make it even more expensive. Very few people can afford to design in the advanced technology nodes. Heterogeneous integration in a package would enable an entry path to the high-end markets much more easily. They don't have to design everything in the most expensive technology nodes to achieve high levels of integration.

Johnson: Just because a small function of the design needs high density doesn't mean the entire design has to be that way.

Horner: Five-nanometer technologies may not be optimal for the high performance I/Os that may be needed. With the thinner oxide layers in the smaller technology nodes, the threshold voltages are lower and more challenging to design high speed I/Os. These are the physical layers. High-speed SerDes may be more optimal in older technology nodes, whereas the rest of



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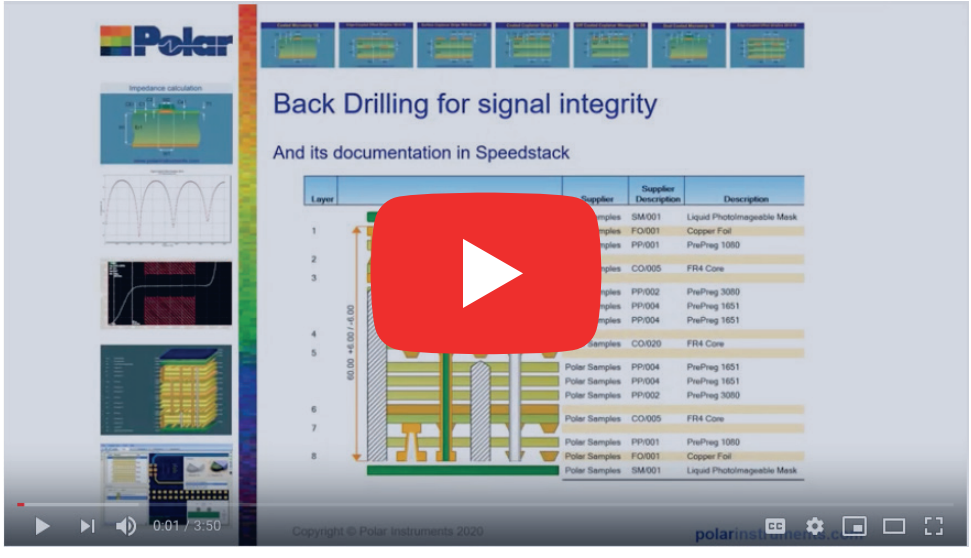

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the computing may be better off in a smaller technology node that would offer higher densities.

By doing heterogeneous integration, you can mix and match devices from different technologies and maybe allow devices to be implemented in their more optimal process nodes, instead of having to be in the same single die. It gives a lot more flexibility for optimization. Even filtering devices can be integrated within the package for smaller form factors. The package is becoming a miniature PCB.

Rita Horner

Johnson: Is that where things get different with the HIR compared to traditional multichip modules? It seems there is a much greater demand on the interconnect part of the technology.

Horner: HIR has bucketed multiple market spaces. They have 5G, computing, and high performance, and they're identifying every one of these, like automotive, aerospace, and different market needs. The PCB traces that used to be 100-micron trace and spaces are shrinking further. On the multilayer PCB, the traces and spaces are about eight microns today.

Happy Holden: Eight microns was the leading edge of people I worked with in Asia, and it's relatively high volume. They'll make 60–100 million of these 50-millimeter by 50-millimeter interposers on an 18- by 24-inch panel. It's very advanced printed circuit technology.

Horner: That's almost the same as the cutting edge in package traces. Packaged substrates used to be 10-micron spaces and width, and the cutting edge is about eight microns right now. The silicon is smaller than one micron. The silicon interposers that are available in the market right now, there is less than one micron, width, and space traces. They tend to be much older technology silicon material. The smaller the width and spacing for die-to-die connection, the more optimal widths and spaces. But it's good and optimal for lots of trace connections, like two or four gigabit-per-second types of frequency.

But once you start going to higher data rates, you cannot maintain using silicon interposers. That's why people are moving more toward the organics, which have a lower loss, but then you're talking about much wider width and spacing traces. Effectively, people are approaching things both on the silicon side and on the packaging side, and trying to address die-to-die connection.

Johnson: Looking into the HIR, I see reference to the organic interposer.

Figure 1: Six application spaces undergirded by AI, VR and AR. (Source: ASE)

Materials	Application	Features (µm)	2018	2019	2020	2021	2022	2025	2028	2031	2034
Organic laminate	FC-BGA	Min. Bump Pitch	110	100	100	90	90	80	80	70	70
		Min. Line width/space	9/12	9/12	9/12	8/8	8/8	5/5	5/5	5/5	5/5
		Min. µVia diameter	50	50	50	40	40	30	30	20	20
	Chiplet (Fan-out, Organic interposer)	Min. Bump Pitch	50	50	50	45	45	40	40	30	30
		Min. Line width/space	2/2	2/2	2/2	1.5/1.5	1.5/1.5	1/1	1/1	0.5/0.5	0.5/0.5
		Min. µVia diameter	30	30	30	20	20	10	10	5	5
Silicon	Chiplet (Si Interposer, 3D)	Min. Bump Pitch	40	40	40	35	35	30	30	20	20
		Min. Line width/space	0.6/0.6	0.6/0.6	0.6/0.6	0.6/0.6	0.6/0.6	0.5/0.5	0.4/0.4	0.3/0.3	0.2/0.2
		Min. µVia diameter	0.6	0.6	0.6	0.6	0.6	0.5	0.4	0.3	0.2

Table 1: Substrate interconnect scale roadmap (micrometers). (Source: HIR, 2019)

Horner: These are the RDL layers that I was describing around two microns. The package substrate material is also referenced as organic, but that is different than an interposer organic, which tends to be referenced to more of an RDL layer that is used for die to die connection.

Johnson: We're now talking about having a semiconductor package that has multiple chips of different capabilities, plus an interconnect using different kinds of interposers. The interposer design is essentially a PCB that goes in the middle of the package. Is this interposer considered an IC design item, or is this a PCB design that then ends up inside the chip?

Horner: There are different materials used for the interposer. The most used interposer today is the silicon interposer. There's also glass that was mentioned earlier. Historically, a package did not have to deal with a lot of the complexities needed in today's multi-die integration. That's why a lot of these tools that were typically used for package substrate design are running out of bandwidth and capabilities for complex multi-die designs. Using EDA tools optimized for complex SoC design is more optimal in addressing silicon interposer design needs. Some vendors are trying to approach it from the package side, and they get a lot of complaints from customers and the people that we're interfacing with, saying, "They're out of juice. They don't have the bandwidth."

How do you do the modeling for your signal integrity analysis? How do you do your modeling in terms of power integrity analysis? How do you bring the information together from different technologies? Even the silicon EDA tools are not capable of doing that because, usually, when you design one IC, you deal with one technology at a time. It's 14 nanometers. You need a more enhanced tool environment that allows you to integrate multiple technologies now to be able to model them, analyze them, do analysis, and validate them in the multi-die environment.

Johnson: This inserts a different domain of knowledge into the IC design team's area of responsibility.

Horner: That's why I was mentioning the need for a collaborative environment. It's not just IC design's problem. It's not only the packaging design person's problem or a signal integrity problem. All disciplines have to work together to make this problem be more optimally addressed.

Johnson: Is this where PCB design experience becomes valuable to the IC team? Is this a place where you'd want to start bringing in

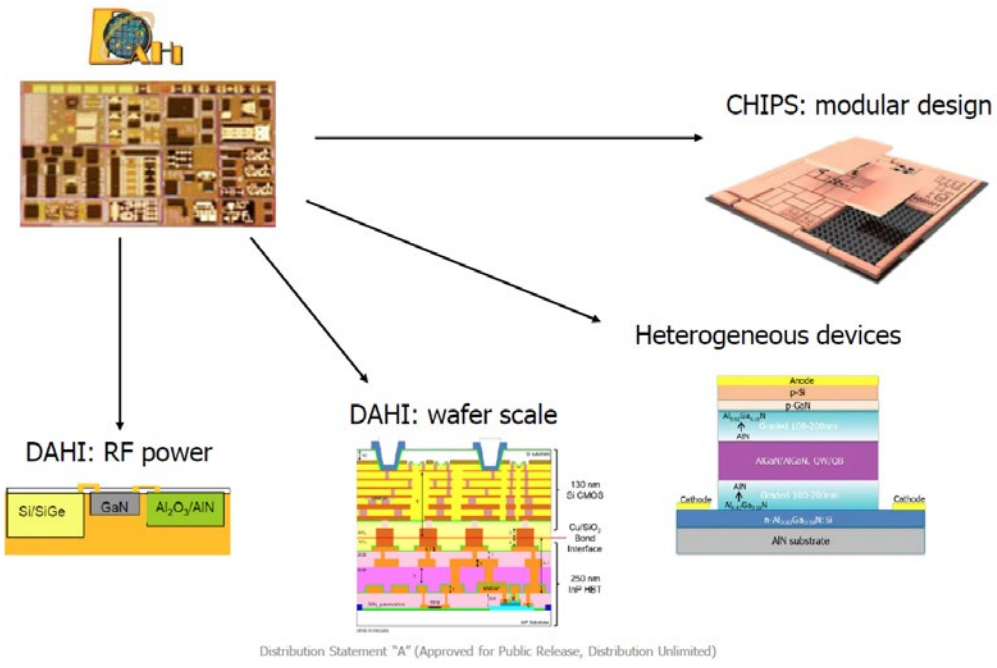

Figure 2: Heterogeneous integration. (Source DARPA)

somebody with board experience to work on the interconnect inside the chip?

Horner: It's not so much board experience. You need to involve the board designer, though. You should not think about PCB design as an afterthought because you want it designed effectively. You're talking about these packages getting to 100- by 100-millimeter dimensions. This is almost a PCB by itself. There will be a lot of balls on that to connect, which may mean lots of layers of board and make the end-product very expensive. When you have all the information, you can create a more optimal environment by collaborating for further optimization of each design layer.

Johnson: I'm imagining how this would work for multiple manufacturers of sensors for autonomous vehicles, all relying on a chip from one or two manufacturers. If there is design-specific collaborating with the PCB, that changes how chip manufacturers provide application notes and instructions to a customer. Do you see that happening?

Horner: That is what's happening in the market. If you own all the pieces that go into a package, that's one thing. But then when you're talking about mixing and combining things, you need some standards. You need some definitions to create chiplets. If I am a chiplet manufacturer that has a niche capability and want to enable other people to use it in their multi-die, I have to have a standard interface.

We need more standards to define interfaces that can be used at the same time. The Open Compute Project (OCP) has gone one further step doing some proof of concept, making sure that it's not just the definition of the die-to-die interconnect; it also has to work. OCP focuses on the high-end computing and ensures that the needs are all met, even going up to the protocol stack.

One member is organizing regular meetings on cataloging and what information is needed for different chiplets for smooth integration. As this organization is driving the initiative, we are asking, "What level of detail does every chiplet need to provide to enable this cataloging and end-user integration? How much detail do you have to provide?"

If I'm getting one part from one vendor and another part from a different vendor, when I'm doing my power analysis, I need some level of detail from every device to do my analysis just for the die-to-die. Forget about going to the package, board, or high level and just making the connection. Ensure that the connection is done correctly and has the right width and spacing for the most optimal performance of the connection. **DESIGN007**

Editor's Note: Stay tuned for Part 3 in October's PCB007 Magazine.

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Managing Information Is Key for Altium's Next Generation of Tools

Feature Interview by Andy Shaughnessy

I recently spoke with Leigh Gawne, the chief software architect for Altium 365, about the future of the company's PCB design tools. We also discussed some of the market drivers in this segment, as well as the challenges that PCB designers are likely to face over the next few years.

Andy Shaughnessy: Leigh, give us an idea of what you see happening with Altium's tools, especially Altium 365, over the next few years.

Leigh Gawne: They'll keep getting better and better! From the PCB design tool perspective, you will continue to see large investments in terms of both breadth and depth of capabilities. Areas such as PCB routing with improved trombone and sawtooth tuning for high-speed layout, through to all new SPICE simulation and constraint management system, will all combine to deliver a promising PCB design experience. Altium 365 will continue to evolve to support the collaborative needs of our customers and will expand well beyond the design domain to bring together supply chain and manufacturing, uniting all the stakeholders in the value chain of electronics design in a way that has not been possible before. You will see big advancements around supply chain intelligence, with proactive health monitoring and customer-specific information that will ensure relevant and actionable insights.

As the platform extends further into the manufacturing domain, customers can expect to benefit from the ability to design with their manufacturer with drastically shortened design cycles and a "right the first time" outcome. With a continuous release philosophy, customers are benefiting from updates to the Altium 365 platform on an ongoing basis. The most recent updates deliver new features, including the component library health dashboard, project history, and 3D assembly variant support. In the near term, expect new comparison and measurement tools for schematic, layout, and 3D native to the browser, making it easier than ever for collaborators to inspect and review.

Shaughnessy: What are some of the biggest market drivers that you see influencing the development of PCB design tools in the near future?

Gawne: The business of our customers is under constant pressure from competition and their customer base. Our customers have to con-

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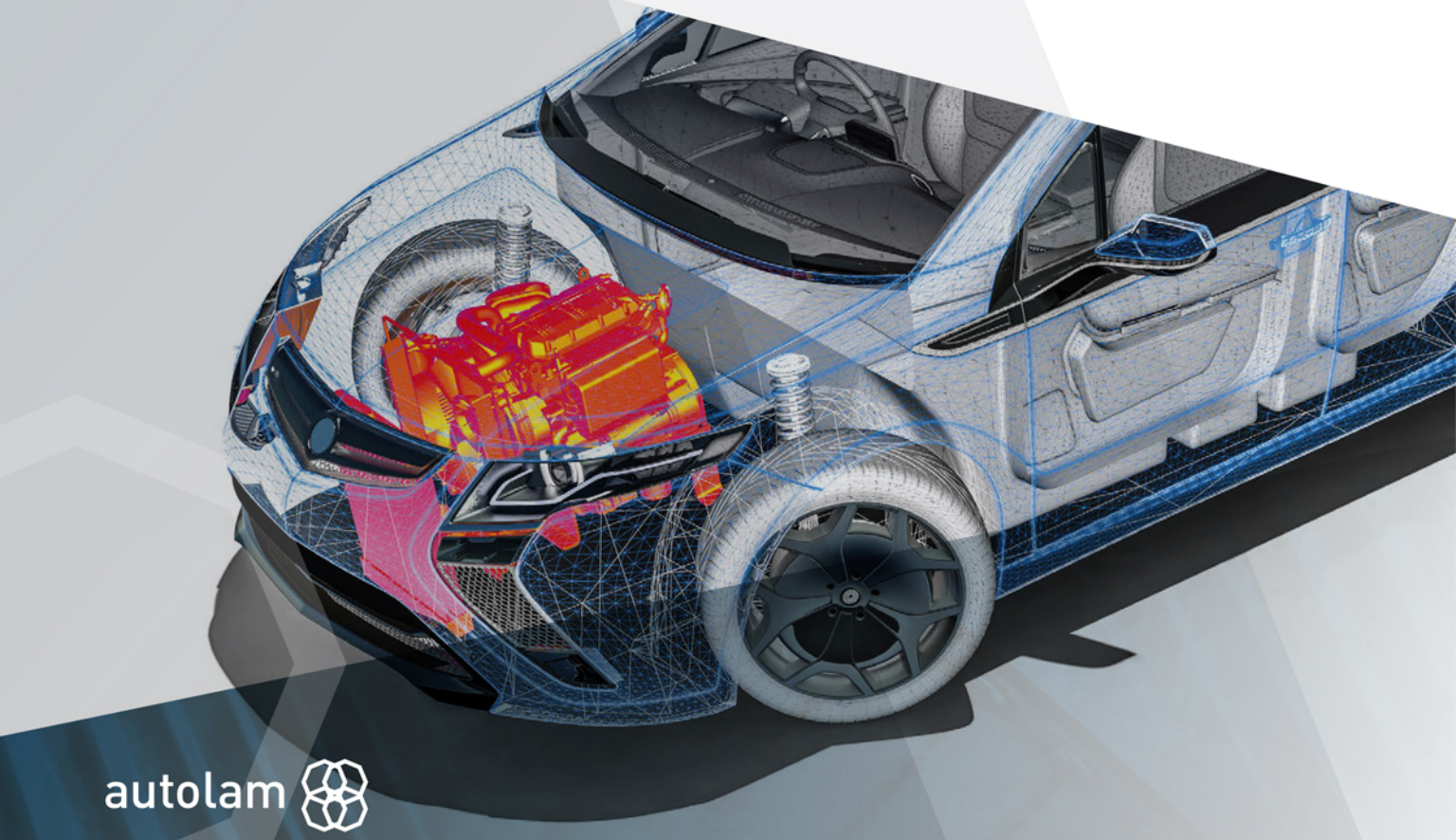

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tinue to innovate and advance to win in their respective domains, which means that their tools have to make it possible for them to work faster and smarter every day.

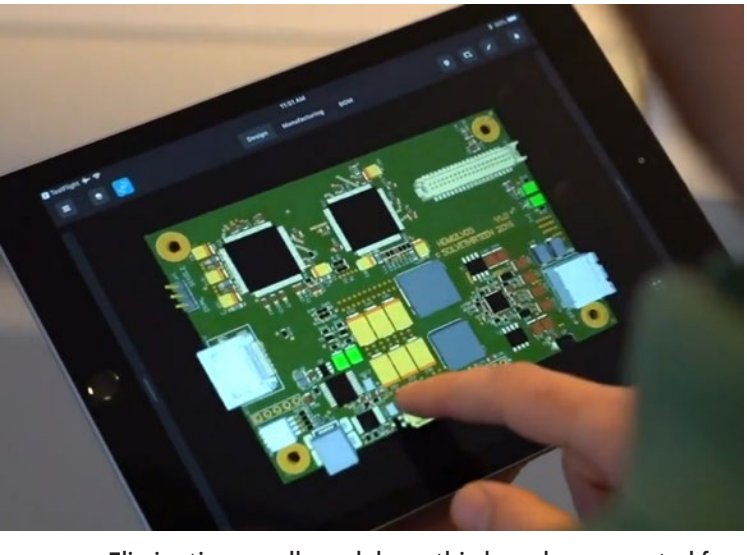
There is a lot of uncertainty in the world today, and our customers are having to react quickly to all sorts of changing and challenging conditions, from geopolitical to macroeconomic. Some of these forces can bring changes to the environment more or less overnight. This means that our customers and we have to be in a position to not only deal with these conditions but flourish in them. Therefore, PCB tools and related services must bring flexibility, productivity, and dependability in a way they have not had to in the past.

Leigh Gawne

Shaughnessy: One thing we've seen is that even veteran designers have issues with handling all of this data. Altium 365 seems to make this part of the process a more user-friendly experience. Do you see data management as an ongoing challenge?

Gawne: Absolutely. There is no silver bullet for it, and it will continue to be a challenge as we innovate. The key is to stay in front of the curve as much as possible, providing our customers with not only the tools and services for data management that they need, but also to support the education and training for how to best approach what can be complicated and challenging problems to solve.

Altium 365 starts to remove a lot of the pain points that customers would have had to suffer in the past, whether that is provisioning and maintaining infrastructure, ensuring robust data backup and disaster recovery strategies, network configuration and security for accessibility, or any other of the plethora of challenges that come with traditional data management solutions. From the outset, we try to help people get organized without forcing them to be organized, delivering that user-friendly experience and value out of the gate without relying on people to change the way they work.



Eliminating needless delays, this board was created for the Open Source Ventilator Project utilizing Altium 365.

Shaughnessy: With so many designers working from home now because of COVID-19, what lessons do you think that EDA companies will take away from this when it's over? I'm assuming it will be over one day, of course!

Gawne: I've always felt that while the EDA industry supports such a fast pace of change and innovation in many industries, and in many ways, our industry has been slow to embrace the very technological advancements and achievements it has helped to bring about.

This is a wake-up call for our industry to reflect and ask whether it is laying the foundation for our customers to continue to be successful in such unprecedented and unpredictable times. There are many lessons to be learned and much inspiration to be drawn from COVID-19. We should see it as a collective opportunity to accelerate toward making the vision of tomorrow a reality today.

Shaughnessy: Thank you, Leigh. I appreciate your time.

Gawne: Thank you. **DESIGN007**

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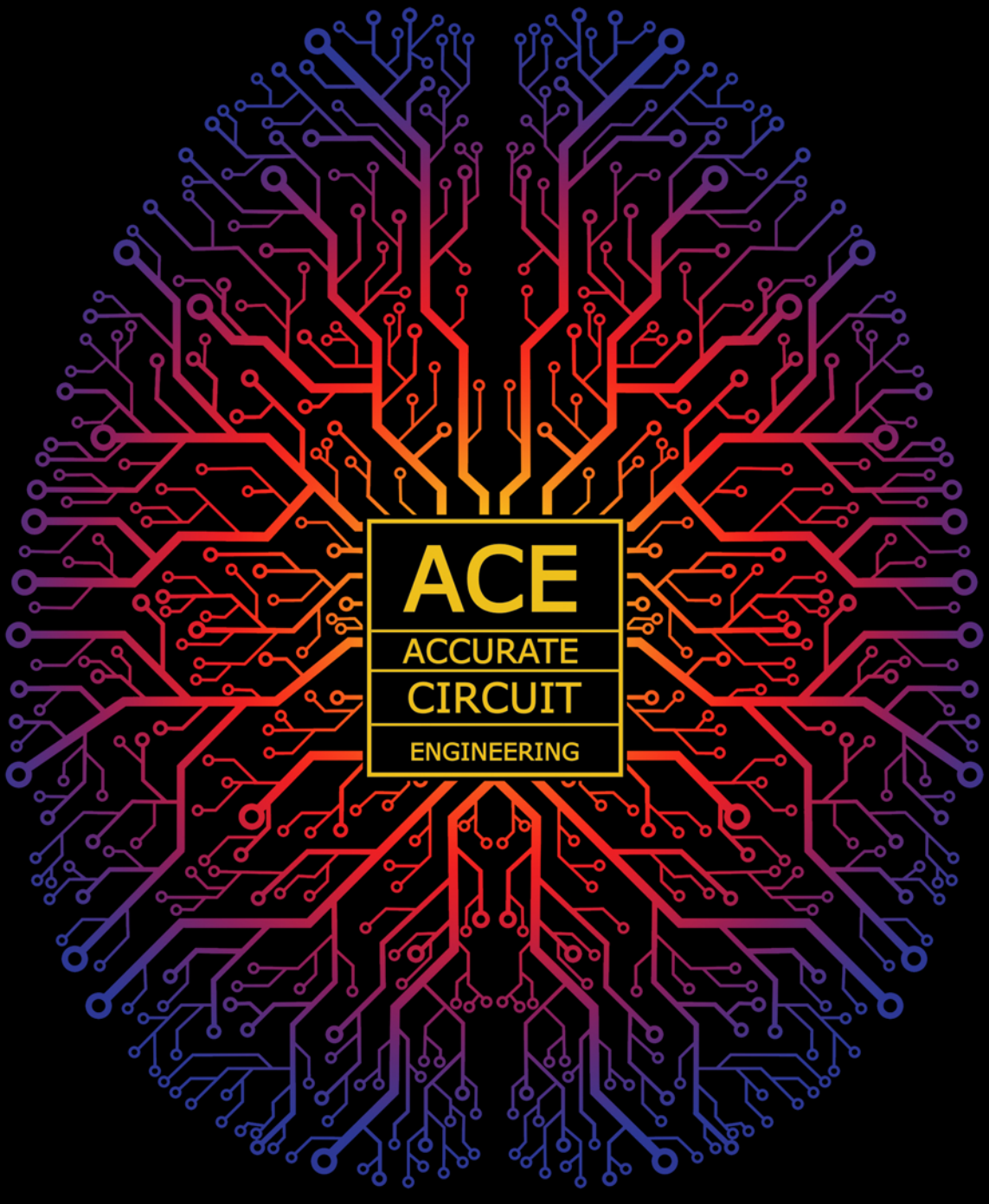

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Local Chapters: You Can Distance This Body But Not These Senses

The Digital Layout
by Kelly Dack, CIT, CID+, PCEA

Introduction

This month, I share a few thoughts on the formation of PCEA chapters as far as where they're at and where they need to go. Next, PCEA Chairman Stephen Chavez offers some encouraging words for these extended times of COVID-19. Finally, I include the list of professional development opportunities and events, as well as a preview of what is in store for next month's column.

PCEA Updates

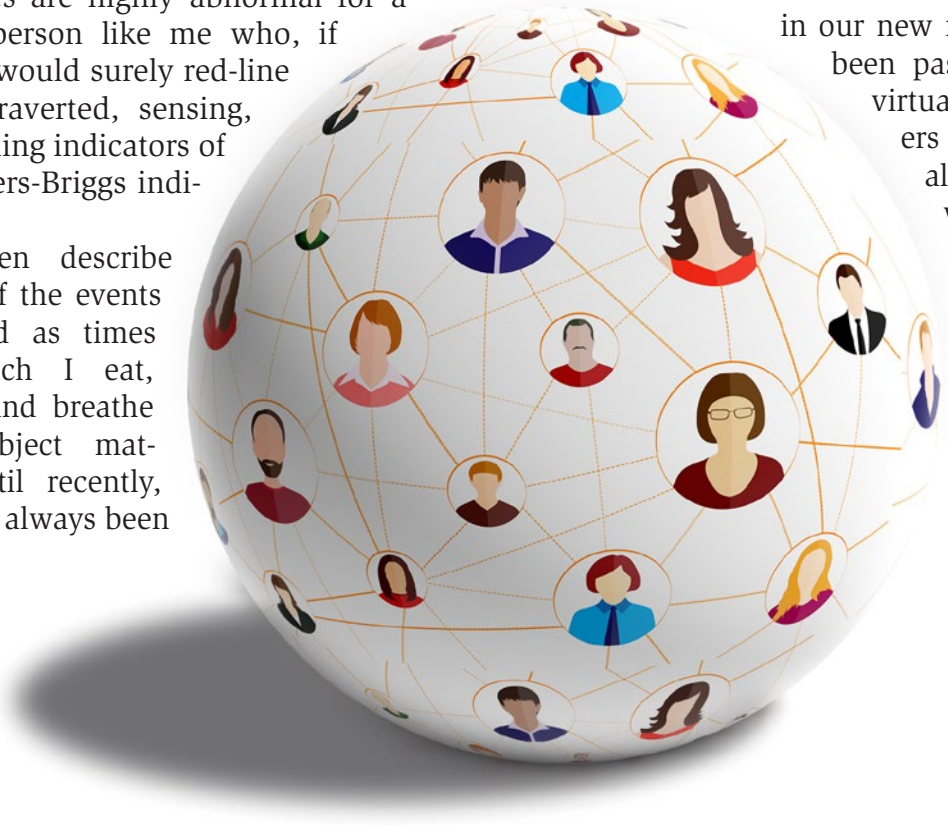
Like you, I need to find ways to engage in normal activities without the comfort of normal surroundings. The surroundings are normal—I've been working at home—but my activities are highly abnormal for a social person like me who, if tested, would surely red-line the extraverted, sensing, and feeling indicators of the Myers-Briggs indicators.

I often describe many of the events I attend as times in which I eat, sleep, and breathe the subject matter. Until recently, this has always been based on my body and its senses being less than six feet (1.8288 meters) from what I am consuming, dreaming about, or breathing in.

Many of you are the same way. We're attending virtual conferences and tuning in to online webinars more often than ever, but we don't seem as happy as when we used to get together physically. Do you realize what is missing?

During a Zoom meeting, an "Aha!" moment struck me. As our industry struggles to reach out and fill in the blanks of normal business routines using virtual means, we are only stimulating two of our five general senses. Of the five general senses—taste, hearing, smell, touch, and vision—only hearing and vision are activated during online meetings.

It almost seems this character flaw in our new meeting protocol has been passed over by novice virtual meeting organizers on purpose. After all, not having to deal with three of the five senses means it is virtually impossible to present an online meeting that is in poor taste, doesn't touch the audience, and downright stinks, right?



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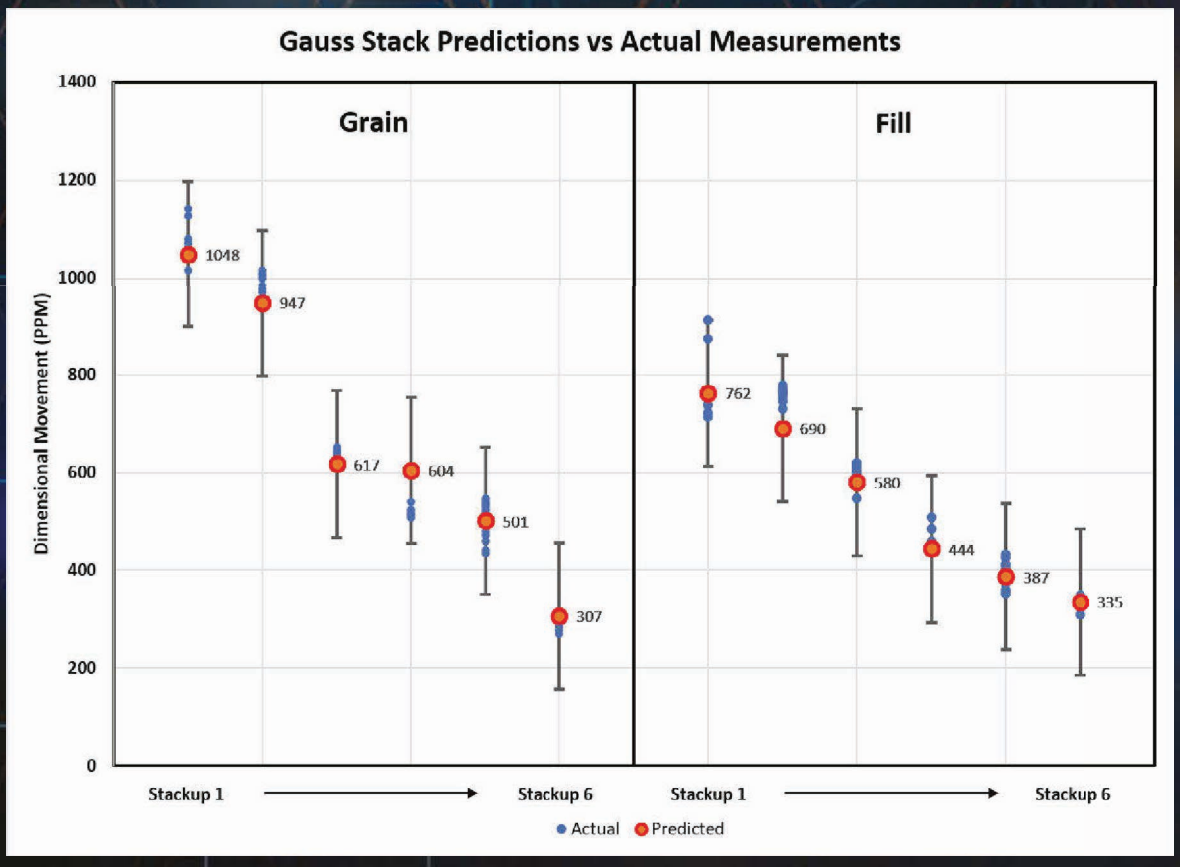

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Presently, I suppose we are doing the best we can. I applaud all of the individuals and organizations in our industry creating outstanding virtual content. In the meantime, PCEA chapter leaders are looking forward to planning chapter meetings that will again address all of the senses for more inspiring, collaborative, and educational experiences. Here's a taste of what they are thinking.

I recently met with Stephen Chavez, PCEA chairman and member of the PCEA Phoenix chapter, as well as three PCEA chapter presidents: Scott McCurdy (Orange County), Tim Mullen (Seattle), and Olga Scheglov (Toronto). These leaders have been preparing for a time when we can get back to the concept of a traditional local chapter meeting.

Scott described past meetings where members could come together, share some food, casually converse, and catch up personally. Then, attendees would be enlightened by a guest presenter who may have brought many samples concerning the topic of discussion to be passed around the audience during the presentation.

He is looking forward to a restart of his arguably largest PCEA chapter. Scott says that a bad day for an Orange County PCEA Chapter was when 50–75 people showed up. They are used to the synergy experience when 100+ people attend and attributed it to the quality stream of sponsors and presenters in the area.

Tim Mullen is preparing for local chapter meetings because he recalls the success the meetings had by bringing an abundance of electronics industry sponsors and presenters into contact with their local membership. He also mentioned that the chapter has access to a 68-seat amphitheater for their meetings and that there's no lack of sponsors and presenters.

Olga Scheglov is an electrical engineer living in Toronto, who has many years of experience associating with local chapter members in Canada. She is very excited about the possibility of her local chapter meeting again. Many of her colleagues—PCB designers, engineers, and technicians—are anticipating future meetings and want to network and hear how the format will evolve.

I asked each of them what their wish list would be for their PCEA chapter to receive before they can again open and meet:

- **Scott:** A four-minute video he can send to members, both new and old.
- **Tim:** More help at the local board level to help with all the details involved in coordinating rich meetings for the members.

Figure 1: From top left to bottom right, Tim Mullen, Kelly Dack, Stephen Chavez, Olga Scheglov, and Scott McCurdy.

- **Olga:** More advertising materials to explain and promote the PCEA in Canada.
- **Steph:** The COVID-19 challenge to subside so that all of the people who work for the organization he chairs can get back to fully using their senses to follow their passion for helping collaborate, inspire, and educate within the electronics industry.

PCEA Chapter Overview

Presidents of active chapters include:

- Phoenix, Arizona: Randy Kumagai
- Orange County, California: Scott McCurdy
- Silicon Valley, California: Bob McCreight
- San Diego, California: Luke Hausherr
- Research Triangle Park (RTP), North Carolina: Randy Faucette
- Seattle, Washington: Tim Mullins
- Nogales, Mexico: Villalba Gonzalez, Roberto Ivan
- Monterey, Mexico: Luis Saracho

Chapters being formed, as well as the presidents, include:

- Albuquerque, New Mexico: Brian Iorio
- Columbus, Ohio: Nicole Pacino and Jody Waltzer
- New England, New Hampshire: Scott Miler and Ryan Primmer
- Northern Illinois and Southern Wisconsin: Anaya Vardya and David Carmody
- Ontario, Canada: Tomas Chester and Olga Scheglov

Message From the Chairman

by Stephen Chavez , MIT, CID+

I cannot believe we are now in the last several months of the year. The holiday season is just around the corner! It's hard to believe most of us are still working from home and probably will be through the end of the year, the way things are going. But we are definitely in full swing and thriving in today's virtual world. Who would have ever thought we'd be here in this isolation situation and for this long?

Stephen Chavez

The industry is still moving forward, and there are lots of activities going on throughout the industry as well. Since face-to-face meetings are not happening throughout the industry, virtual events continue to be the norm. We just saw PCB West come and go. Many large industry events—such as CadenceLIVE, Siemens' Realize LIVE, and others—have adapted and are now taking place virtually. Webinars are coming along in full strength, as most of our mailboxes are flooded with invites.

All of our local, regional, and global PCEA chapters are doing their part and adapting as well. No longer able to meet in person until who knows when, webinars, teleconferences, emails, and IM chats are the way things are continuing to happen. As the old saying goes, "Where there is a will, there is a way," and our chapters are doing just that.

The PCEA Silicon Valley Chapter recently held its first-ever virtual event with great success. Several other PCEA chapters will soon follow in their footsteps in the virtual world as well. I am excited to see how the PCEA leadership, along with each of the chapters, are meeting today's challenges to remain active and evolve in these tough times.

Refer to our column and the PCEA website to stay up to date with upcoming industry events. There are lots of free webinars being offered, so take advantage of them as you can! And if you have not yet joined the PCEA collective, I highly encourage you to do so by visiting pce-a.org and becoming a PCEA member.

I continue to wish that everyone and their families remain healthy and safe.

Next Month

There is a group of dynamic leaders in the PCB industry who happen to be women leading the PCEA. In next month's column, find out who these leaders are, as well as their ideas for advancing your career by becoming involved with the PCEA.

Upcoming Events

- October 6–8, 2020: **AltiumLive 2020 Virtual Summit**
- October 6, 13, 20, and 27, 2020: **EDI CON Online**
- March 6–11, 2021: **IPC APEX EXPO** (San Diego, California)
- April 13–15, 2021: **DesignCon** (Santa Jose, California)
- May 5–6, 2021: **Del Mar Electronics & Manufacturing Show** (Del Mar, California)
- May 11–13, 2021: **IPC High-Reliability Forum 2021** (Baltimore, Maryland)
- November 10, 2021: **PCB Carolina** (Raleigh, North Carolina)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Conclusion

We must not let our senses atrophy as we engage virtually for the time being. For now, to successfully reach those with whom we wish to truly communicate, we must figure out ways to activate all senses. Will you blandly explain to your audience that applying too much heat to a PCB causes failures like delamination, or will you go the extra mile for those in your audience who have not smelled the odor of burnt FR-4 material by sending out samples of damaged boards before your presentation? If we do not get back to on-site visits, tours, and meetings soon, a tactic like this to engage the senses could make a critical difference between virtually reaching your audience or not.

Along with our PCEA chapter leaders, I am hopeful that our local chapters will be able to meet again soon. Local sponsors, great presenters, meals, and even live hugs and fist bumps are terrible things to waste. See you next month or sooner! **DESIGN007**

Kelly Dack, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). To read past columns or contact Dack, click here.

DigiLens Brings Ultra-Compact CrystalClear AR HUD to Any Auto Dashboard

DigiLens Inc. has announced the availability of its CrystalClear Augmented Reality (AR) Heads-up Display (HUD), boasting the largest field-of-view (FOV) HUD up to 15° x 5° and packaged into approximately 5 liters of volume.

Most cars today have a thin dash that doesn't allow a large volume HUD to reside beneath the dashboard. Conventional mirror-based HUDs and DMD-based AR HUDs support safety with real-world view assisted navigation, but are much larger than DigiLens' waveguide-based HUDs. The CrystalClear AR HUD is based on DigiLens' proprietary photopolymer material to enable a thinner multi-layer waveguide with a light engine to direct the light from underneath with maximum efficiency for a full HUD display solution.

"HUD volume, field of view and the image location have been the biggest barriers to adoption of AR assisted driving in automotive," said Chris Pickett, CEO of DigiLens. "We have, by far, the widest FOV HUD available on the market and the HUD image is displayed at infinity thereby giving meaningful and contextual visual data that can be attached to the world in front of a driver, so the driver never has to take their eyes off the road."

(Source: Globe Newswire)

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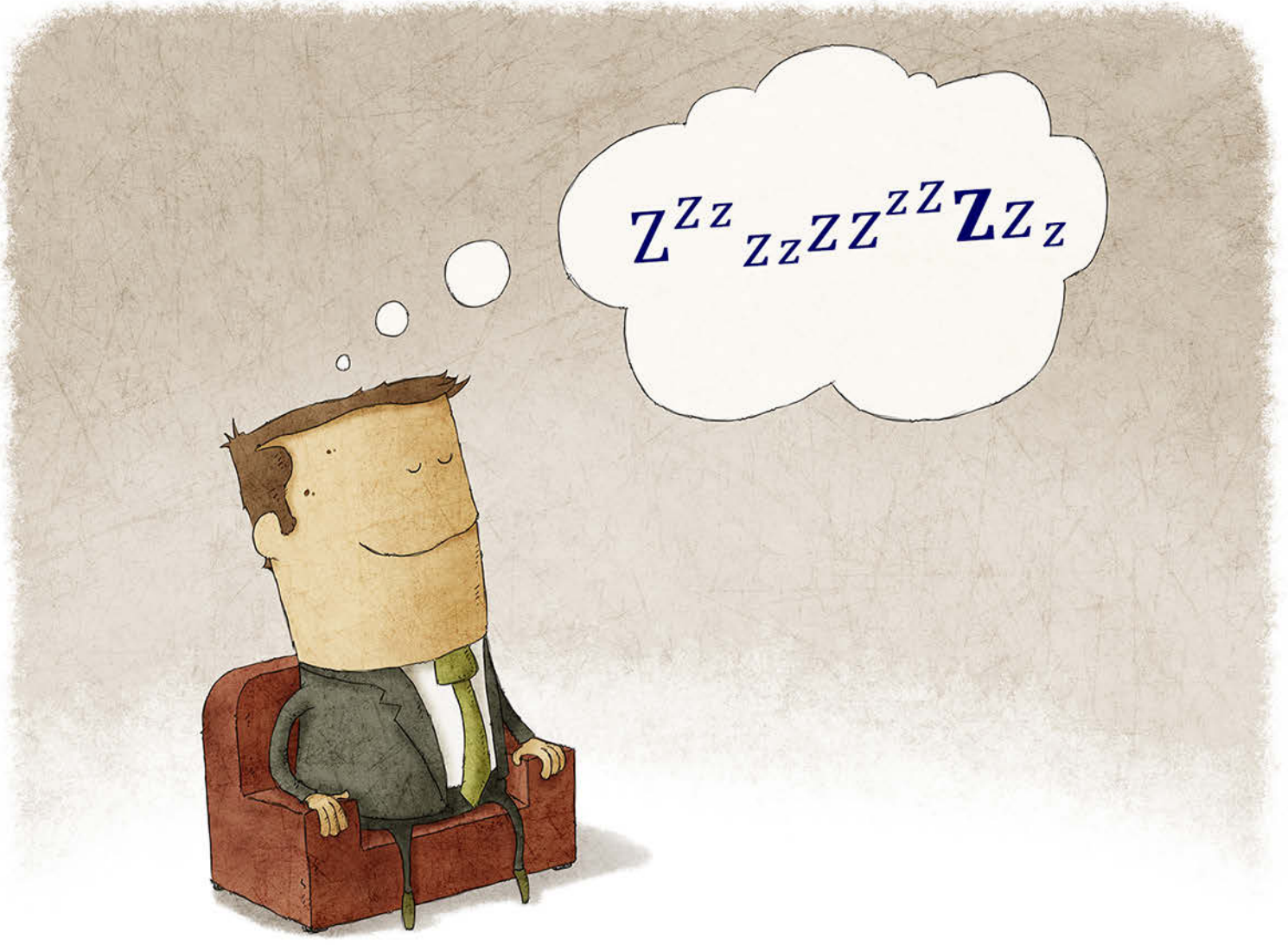

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Empowering Electrically-Aware PCB Designers of the Future

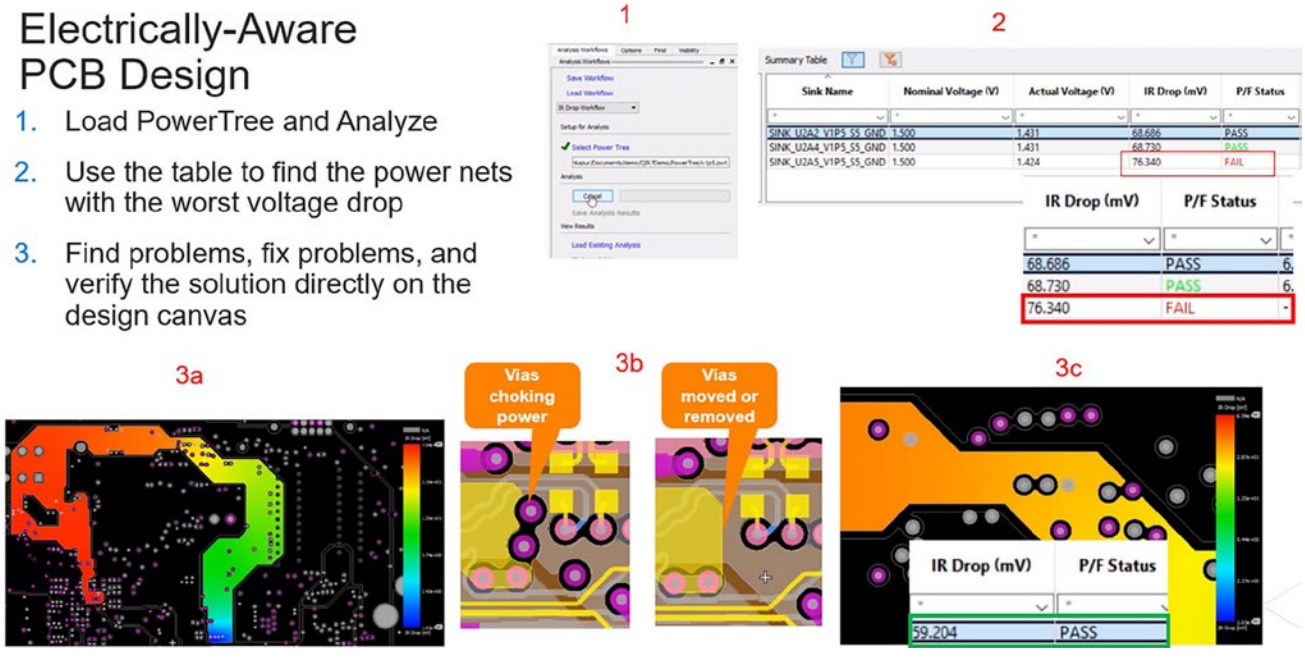
Feature by Michael Nopp
CADENCE DESIGN SYSTEMS

PCB design has always been where the rubber meets the road in terms of applied engineering to make a physical product. Driven by all the disciplines required to build a modern PCB, design teams need better tools to streamline ever-shortening design cycles. Time is of the essence, and more data is needed to improve design tradeoffs.

Current PCB design job postings explicitly request a generalist to tackle all facets of PCB design. The amalgamation of traditional disciplines and use models is giving rise to the engineer who works on the entire flow in a smaller team. As the traditional, dedicated layout designer is now becoming a generalist, the push to integrate and understand so many concepts such as high-speed design and the complexities of modern-day interfaces is pushing PCB design tool requirements.

Younger EEs are driving tool requirements as well by breaking down the traditional dedicated groups of layout: SI and PI experts. Faster data rates and the smaller interconnect densities required to meet current and future specifications are driving designers to extract and simulate interconnects to verify noise margins on more and more nets. In the future, PCB teams will also need to be electrically aware to meet interconnect density requirements and faster data rates. When more requirements and non-experts converge, the tools need to change.

Point tools of the traditional PCB designer organizations are difficult to pick up, and more analysis at the early stages of the design is needed to catch the low-hanging fruit of design problems. Potential failure cases must be screened out before signoff; otherwise, changes and reiterations of the design eat into the product cycle. At most hardware sites, schedules are compressed, and time to market is essential. Reducing design cycle time is key to market success. This can be achieved by enabling the engineer to quickly access analysis to shorten the designers' observe, orient, decide, and act (OODA) loop.



The OODA loop can be applied to the PCB design process when screening and fixing problems. PCB design requires filtering the available information, sorting and putting that information into context, and then acting with better information. Cadence has continued to invest in the area of modern system design and analysis to cover all facets of the PCB design process, such as the newly introduced Sigrity Aurora flow.

Sigrity Aurora is designed with the goal of raising up a generation of electrically-aware PCB designers. It is an enablement tool with dedicated workflows to screen PCB boards in the signal integrity (SI) and power integrity (PI) domains. Shortening the design cycle time means shortening the OODA loop and reducing the friction of design changes in the light of analysis feedback.

A user goes through the OODA loop in the PCB design process by first observing the PCB for various failure constraints by simulation or electrical rule checks with the Sigrity Aurora flow. Once the workflow is selected, and nets run, the tool orients the user with the Allegro canvas overlay and sortable tables of data. This enables designers to screen a large amount of data in massive designs.

In many cases, the entire board cannot be manually screened, and items may be missed, such as a reset line being coupled to a noisy aggressor that could cause a fatal system reset. In screening the design for potential SI and PI problems, users bring issues to the forefront of the design cycle before issues are found at signoff or in the lab.

When new interfaces are used, the focus often shifts away from lower-speed nets and the system itself. Issues can fall through the cracks, and designers may miss overlooked nets. Expensive rework late in the design cycle causes design slippage and board re-spins. By expanding the surface area of analysis coverage, fewer cycles are used fixing problems later in the design cycle.

Cadence is also investing in the area of design feasibility analysis. The OODA loop of the design process can be augmented in the feasibility stage as well. The users can pre-plan topologies and explore the design space by sweeping parameters like trace length. Once the variables are explored, users can simulate drive strength and define constraints for successful routing. Designers can experiment in a sandbox to assess placement and stackup changes on SI and PI problems without a schematic.

Cadence will continue to invest in and enhance the PCB design flow, now and into the future. The crossroads of physics, mechanical design, and electrical engineering culminate in the art of PCB design, and the next generation of PCB designers will have to be more electrically-aware than ever before. **DESIGN007**

Michael Nopp is a lead product engineer at Cadence Design Systems.

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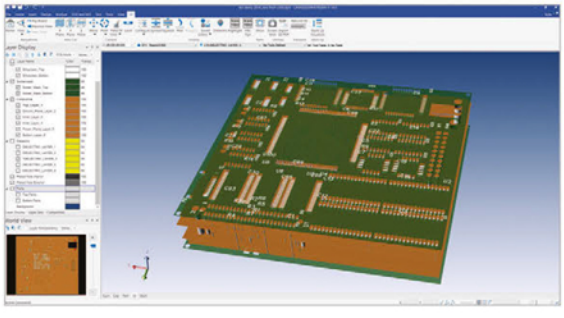

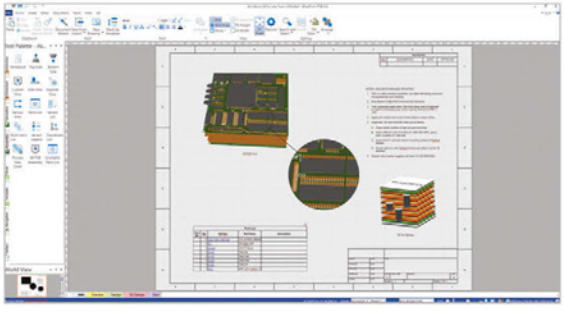

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Why Do High-Frequency Materials Have Different Dk Values?

Lightning Speed Laminates

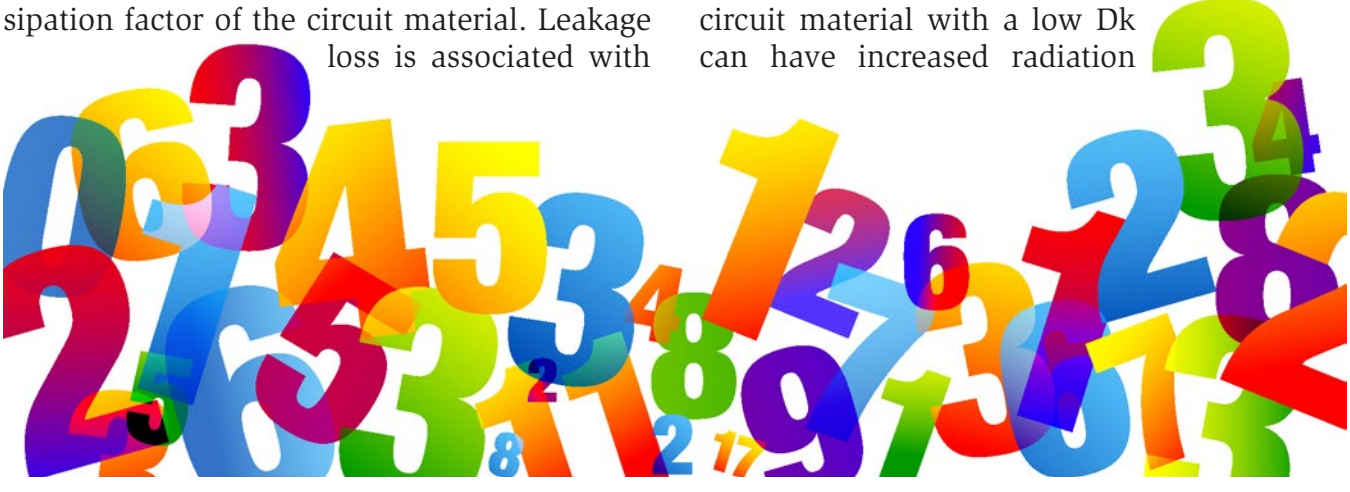
by John Coonrod, ROGERS CORPORATION

When an engineer researches high-frequency circuit materials, they will notice there are many offerings of what appears to be the same material type but with different Dk values. One might ask, "Why are so many different Dk values desired?" The answer is not straightforward, but there are very good reasons for these different materials. This column will give a quick overview of the need for these materials with different Dk values, as related to different high-frequency applications.

Insertion loss is often considered with many high-frequency applications and is made up of four components: conductor loss, dielectric loss, leakage loss, and radiation loss. The conductor loss is related to the circuit conductor; often, the major concern is the surface roughness at the copper-substrate interface.

Dielectric loss is mostly related to the dissipation factor of the circuit material. Leakage loss is associated with the volume resistivity of the dielectric material, which is between the copper planes. Typically, the volume resistivity is very high for high-frequency circuit materials, and due to that good property, leakage loss is not a concern. Although, some high-power applications can have an issue with leakage loss. The last component of insertion loss is radiation loss, and that is how much loss is radiated off the circuit.

Radiation loss is generally not desired because it is an increase of the signal loss, but there is an additional concern with the radiated energy having the potential to corrupt neighboring circuitry. There are many different items that can cause radiation loss to vary, including circuit design, substrate thickness, PCB fabrication anomalies, the Dk of the substrate, and frequency. In general, a high-frequency circuit material with a low Dk can have increased radiation



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loss, and a higher Dk material will have less radiation loss. However, there are cases where higher radiation loss is desired, and that would be for antenna applications where they have circuit patterns intended to transmit (radiate) energy at a certain frequency. In the case of antenna applications, you will typically find that a lower Dk material is used, but there are exceptions.

Radiation loss is generally not desired because it is an increase of the signal loss, but there is an additional concern with the radiated energy having the potential to corrupt neighboring circuitry.

There is another attribute of Dk that relates to circuit size. In general, circuits using materials with a lower Dk value will have a longer wavelength than circuits using material with a higher Dk value. Many RF applications are very sensitive to wavelength, and the designs of the circuit features are very often based on a fraction of wavelength. As an example, a circuit structure intended to resonant will often be designed to have a physical size that relates to half the wavelength for the intended frequency of resonance.

Expanding on this example, if an RF circuit design is intended to have a resonant peak at 3.6 GHz, it uses 20-mil material; the Dk value of the material is 3.66, so the resonator element should be about 0.97" (24.6mm) in length. However, with that same comparison and the only difference is material with a Dk value of 6.4, the length of the resonator element will reduce to be 0.77" (19.6 mm).

That is a size reduction of about 20%, and if a material is used with a Dk value of 11.2, that will give a size reduction of 37%. These different resonator sizes, using materials with different Dk values, will still yield a resonant peak at 3.6 GHz. However, with the decreased resonator size, the other circuit features will also decrease; in some cases, that is not desired. There can be many trade-offs to consider when choosing materials with different Dk values.

Another thought for Dk differences involves considering coupled features. In RF engineering, there are often circuit features coupled together by their electric fringing fields. These coupled circuit features are used to design and implement many different types of RF filters, directional couplers, and impedance matching networks. The strength of the coupled fields between these circuit features is often critical, and the intensity of the coupled fields will vary with a Dk dependency.

A high-frequency circuit using coupled technology and a material with a lower Dk value will have less field intensity than using a circuit material with a higher Dk value. Basically, a circuit material with a higher Dk will cause the fields to concentrate, and they will not spread over a larger area, but they will have higher intensity in a small area. This also goes back to the concept of radiation, where I commented that circuits using materials with high Dk do not radiate as much as circuits using a lower Dk because the fields are more concentrated within the circuit for the high Dk material.

This was a quick overview of different things to consider when using high-frequency circuit materials with different Dk values; however, there can be many other issues to consider for different PCB applications. The designer should consult their high-frequency circuit material supplier when dealing with the details of their particular application and understand what the optimum material choice would be for their circuit design. **DESIGN007**

John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, click here.

PCB007 Highlights

Trouble in Your Tank: A Process Engineer's Guide to Electroless Copper ▸

Mike Carano highlights electroless copper plating solutions, focusing on a copper formulation based on copper chloride, EDTA, formaldehyde, and sodium hydroxide.

The Right Approach: Leadership Lessons I Learned From Sonny Barger ▸

Countless books have been written about the great leaders throughout history who have served as role models for generations of business executives. But what about the lessons that can be learned from the names you won't typically find in the business section of your local bookstore? Steve Williams discusses leadership lessons he learned from Sonny Barger.

Punching Out! Are We Selling a Business or Watching 'Die Hard'? ▸

There is a lot of drama involved in selling a business. According to Wikipedia, the movie series "Die Hard" is about "a police detective who continually finds himself in the middle of violent crises and intrigues where he is the only hope against disaster." Tom Kastner explains how if you use the "strong or powerful" definition of "violent," that pretty much describes many M&A deals.

The Plating Forum: Immersion Plating Reaction in Electronics Manufacturing ▸

Plating or metal deposition is a key component in the manufacturing of electronic packages (circuit boards and integrated circuits). Plating occurs when a metal ion in solution (electrolyte) is reduced to the metal. The reduction takes place when electrons are supplied to the ion. George Milad dedicates this column to the immersion reaction.

Just Ask John Mitchell: Are IPC's Positions Dictated by Politics? ▸

First, we asked you to send in your questions for Happy Holden, Joe Fjelstad, and Eric Camden in our "Just Ask" series. Now, it's IPC President and CEO John Mitchell's turn! A regular PCB007 columnist, John focuses on many of the challenges affecting the global electronics industry supply chain. Over the years, he has served as an engineer, manager, and executive at a variety of companies and organizations. We hope you enjoy "Just Ask John."

Better to Light a Candle: Chapter 8—Expanding the Model in This New Reality ▸

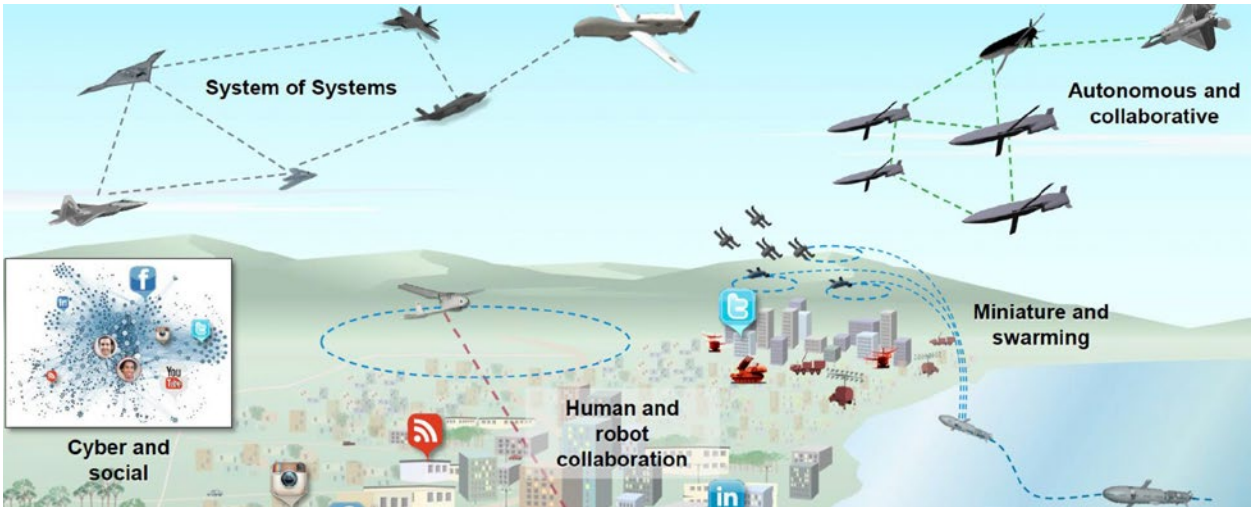
Marc Carter posts an update on the collaborative grassroots effort to prepare the next generation of PCB "experts" by outlining the progress of efforts to replicate the MTU "prototype" at other industry-academia "nodes" around the country.

North American PCB Industry Sales up 10.1% in July ▸

IPC announced the July 2020 findings from its North American Printed Circuit Board (PCB) Statistical Program. The book-to-bill ratio stands at 1.0.

Rogers Introduces RO4450T Glass Reinforced Thermoset Multi-Thickness Bondply ▸

Wireless circuit designers can now enjoy a true breakthrough with Rogers Corporation's RO4450T™ bondply. This product offers designers a spread glass reinforced bonding material in seven thickness options ranging between 0.0025" (0.064 mm) and 0.006" (0.152 mm), greatly improving flexibility for high multilayer board count designs.



The Aerospace and Defense Chapter of the HIR

Feature Interview by the I-Connect007 Editorial Team

Nolan Johnson and Andy Shaughnessy recently spoke with Jeff Demmin of Keysight Technologies, who breaks down the work his team has done on the Aerospace and Defense Chapter of the Heterogeneous Integration Roadmap (HIR).

Nolan Johnson: Jeff, IEEE pointed us in your direction to discuss your chapter of the HIR. What's your background and involvement with the HIR?

Jeff Demmin: My background is broadly in semiconductor packaging. From 2015 to 2019, I worked for a company called Booz Allen Hamilton, which is a major government contractor. In that role, I supported leading-edge technical research related to packaging and heterogeneous integration, primarily at DARPA. I also have some background in the publishing world.

With my long career in packaging and my more recent experience specifically in the military and aerospace arena, I got tapped to work on the Aerospace and Defense Chapter of the HIR. I know most of the people involved in it, and I like to participate in industry activities, so it was an obvious match. Also, I want to be clear that my involvement is as the co-chair of this committee on the HIR and is not associated with my work for Keysight Technologies, nor does it represent the company's thoughts. I do this mostly in my spare time, which is probably true of many of the people participating.

I jumped in relatively early a few years ago, shortly after the HIR effort was begun. It was created to continue the work of the broadly used International Technology Roadmap for Semiconductors (ITRS), which had been around for a couple of decades, driving the node-based metrics for how the semiconductor industry should move ahead. But with Moore's Law running out of steam, mostly meaning that it's too expensive to keep it going, the HIR was one thrust that arose from the demise of the ITRS.

Johnson: The rationale makes sense. There may be a portion of your overall design that requires cutting-edge fabrication technologies but forcing your entire design to adhere to that

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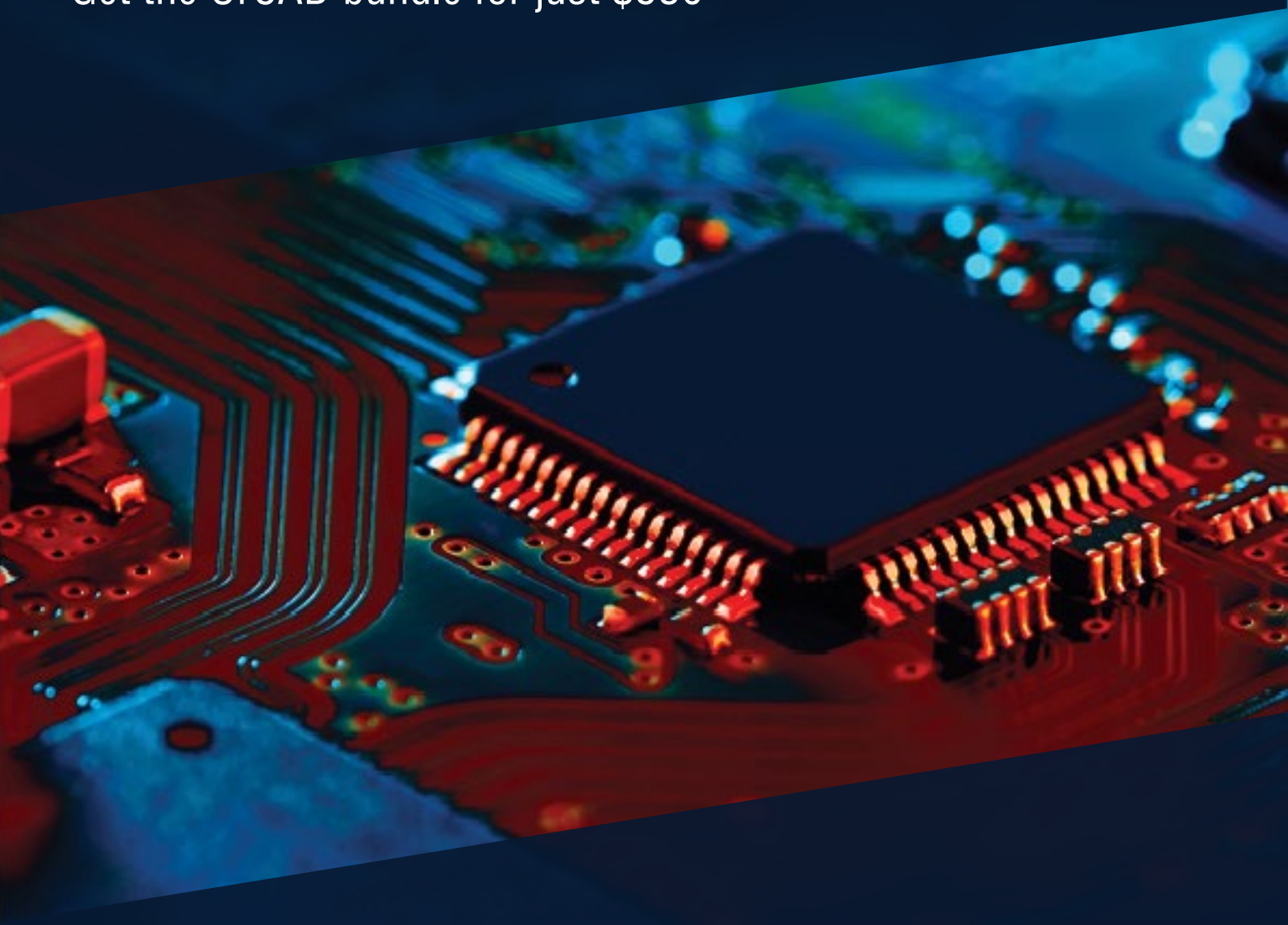

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Jeff Demmin

just because you need it in one key section has always been onerous. This does give you the opportunity to flex with what's inside the package.

Demmin: The most obvious example of that, which has been recognized for a long time, is memory and processors. They use different fabrication processes. It's still silicon, digital, etc., but they're different processes just because of the nature of how they function. Splitting memory off from processors has been common for quite a while.

But all the other functions that end up in a big system-on-chip piece of silicon makes it quite inefficient to do it that way. Designers do everything they can to minimize the area's silicon usage. And if you can carve out something that doesn't need that leading node, that's a smart thing to do, but you need to put it all back together after you carve it up. That's the heterogeneous integration angle need that arises from this partitioning.

Johnson: Your target audience and the industry you're writing about have a reputation for being fairly conservative. What would be the motivation for the mil-aero industry to jump into this technology?

Demmin: It's different depending on what industry you're in. One of the challenges is that the HIR effort covers everything from consumer to military. Companies that are on the digital high-volume side that are very supportive of this—such as Intel, AMD, and NVIDIA—can save a lot of money and create new capabilities if they can divide up their functions and then integrate them after the optimized manufacturing of each.

Xilinx was the first to divide up one of their big FPGAs, and they split it into four slices and put them on a silicon interposer that connected them together. Nowadays, that's pretty common to do something like that; companies like Intel are integrating different kinds of devices—not just the same device divided into more manageable chips. There's a lot of interest in heterogeneous integration of processors, data converters, memory, ASICs, and even optical components now.

On the military side, in spite of what people might envision as unlimited funding for military stuff, that's not really the case—especially when the volumes are low, and you don't have the total volume driver as you do in cellphones to amortize design, mask, and fab costs. Having those same kinds of savings, while still mixing and matching the best types of devices for different functions, offers that benefit for the aerospace and defense world.

It has even more challenging because there would commonly be a wider variety of devices potentially in a radar system or defense communication or electronic warfare where you need to be able to put together silicon, gallium arsenide, indium phosphide, and gallium nitride, among other device types to get the best possible performance. Challenges are conceptually similar in military and aerospace, but there are typically more types of devices for these specialized applications.

Johnson: What was your team's process for putting together the chapter?

Demmin: Tim Lee of Boeing is the other co-chair, and he started on this before I did. The roadmapping process is especially tricky for heterogeneous integration, where there are so many variables. It doesn't always work to have the node-drive tables and metrics as had been in the ITRS. There are different types of devices, applications, design processes, and materials. There are so many more variables that couldn't replicate what had been done before on roadmaps.

The aerospace and defense chapter starts with a landscape of what people are doing. That meant compiling information on government efforts in this area, as well as some industry capabilities. Step zero of a roadmap is to have a starting point. The initial release of the chapter last year was more like a landscape, such as, "Where do things stand now? What are some of the activities underway?" It wasn't as much of a prescriptive roadmap of what we're projecting to be in place, but we will be working toward that in future editions. The process moving forward will follow the same practice as the ITRS, with alternating years of totally new versions and more modest updates in years in between. We're due for an update with some changes.

For the 2020 update after the inaugural 2019 edition, we put together a high-level table that looks more like a roadmap but still needs input to populate the various topics into the future. We broke it up into some different areas of performance, metrics, design processes, integration technologies, and segments of reliability. For these heterogeneous systems, reliability has not been thoroughly thought out and captured. There are all kinds of standards for single chips and packaging. There are different approaches that are still in the works.

One example that highlights how A&D is different from commercial and consumer products is the supply chain. That's one of the big differences between aerospace and defense compared to the product areas covered in the HIR. It's just a matter of security requirements throughout your supply chain, but it also requires obsolescence management in A&D because product lifetimes are often longer than the typical lifetime of devices within it. That's much less of an issue for commercial products where there are multiple suppliers, and you are churning new designs routinely that incorporate whatever the latest available devices are.

One new development that we expect to help the HIR is high-level interest and funding in semiconductor manufacturing from the U.S. Government. You've probably seen a couple of different bills in Congress and the Senate. They represent an enormous level of funding—at least $25B—for the semiconductor industry in the U.S. Clearly, it's focused on manufacturing, which is a notable change and a good addition to the DARPA-style research targeting breakthrough technologies. Also, it's very broadly based, with funding via the NSF, Department of Energy, and Department of Commerce—not just the DoD. There are efforts to create interposer-based heterogeneous integration facilities in the U.S., for example, rather than relying on off-shore capabilities.

One example that highlights how A&D is different from commercial and consumer products is the supply chain.

Johnson: You do have a bit of interposer design and manufacturing required for heterogeneous integration.

Demmin: It's just interconnect on the interposer, so theoretically, it's easier than fabricating leading-edge devices. People have even tried things like having just a layer or two for customization in your interposer design above standard pre-fabricated power and ground planes. It's not quite as efficient for performance or design, but you can do it faster. As volumes increase, I can see some novel approaches like this facilitating adoption by reducing cost and turnaround time.

In DARPA's CHIPS program, part of the output was some very advanced designs and integration schemes, but getting those interposers manufactured and devices assembled was difficult because those capabilities aren't really available on a merchant basis in the U.S. Another output from the CHIPS program was a "wish list" for a national capability for interposer-based assembly.

This was input into the SHIP program. SHIP is a Naval Surface Warfare Center program for "State-of-the-Art Heterogeneous Integrated Packaging." This program is underway, and all of the detailed specifications and metrics for the SHIP program will be very helpful for the HIR.

Johnson: There is a lot of implied impact on PCB fabrication and assembly down the line as heterogenous integration becomes more prevalent.

Demmin: Definitely. All the advanced R&D like at DARPA is necessary, but a lot of it comes back to the PCBs for the advanced package substrates. That's where the rubber hits the road. The large volume of everything depends on the circuit board.

DARPA frequently uses a slide that shows that the PCB is the original heterogeneous integration platform, and it arose out of the need during World War II for a proximity fuse. They needed to get a lot of functionality within the small device, and the first high-volume PCB was the answer. The most advanced packaging substrate is conceptually no different from that PCB from 75 years ago.

Johnson: Do you have some specific feedback you'd like to hear from industry participants?

Demmin: We have a few others besides Tim and me, but we'd appreciate anyone who can help with informed input. To provide some focus, I've sent them this table, asking them to provide inputs on whether there should be other rows and get their input on what they think is state of the art, what they think it should be, and where it's headed. We're theoretically doing a 5-, 10-, and 15-year outlook, and it might be useful to have more granularity. Feedback on this table is the main thing I've asked for from other volunteers and the audiences of these presentations.

Johnson: Thank you very much, Jeff.

Demmin: Thanks. SMT007

Editor's note: To learn more, read Demmin's article "The Heterogeneous Integration Roadmap for Aerospace and Defense" in October's SMT007 Magazine.

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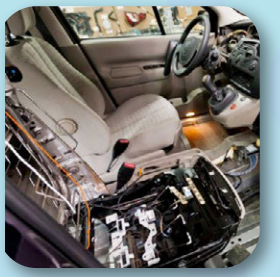

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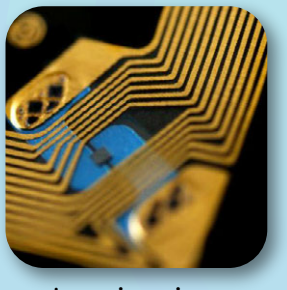

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Pushing the Boundaries of Thermal Management

Sensible Design

by Jade Bridges, ELECTROLUBE

Thermal management plays a central role in circuit and electronic assembly design, ensuring improved reliability and increased performance of devices. But what if you could push the boundaries even further and extend the long-term stability? To explore how this can be achieved, I'm going to touch on some of the latest advances in thermal management technology.

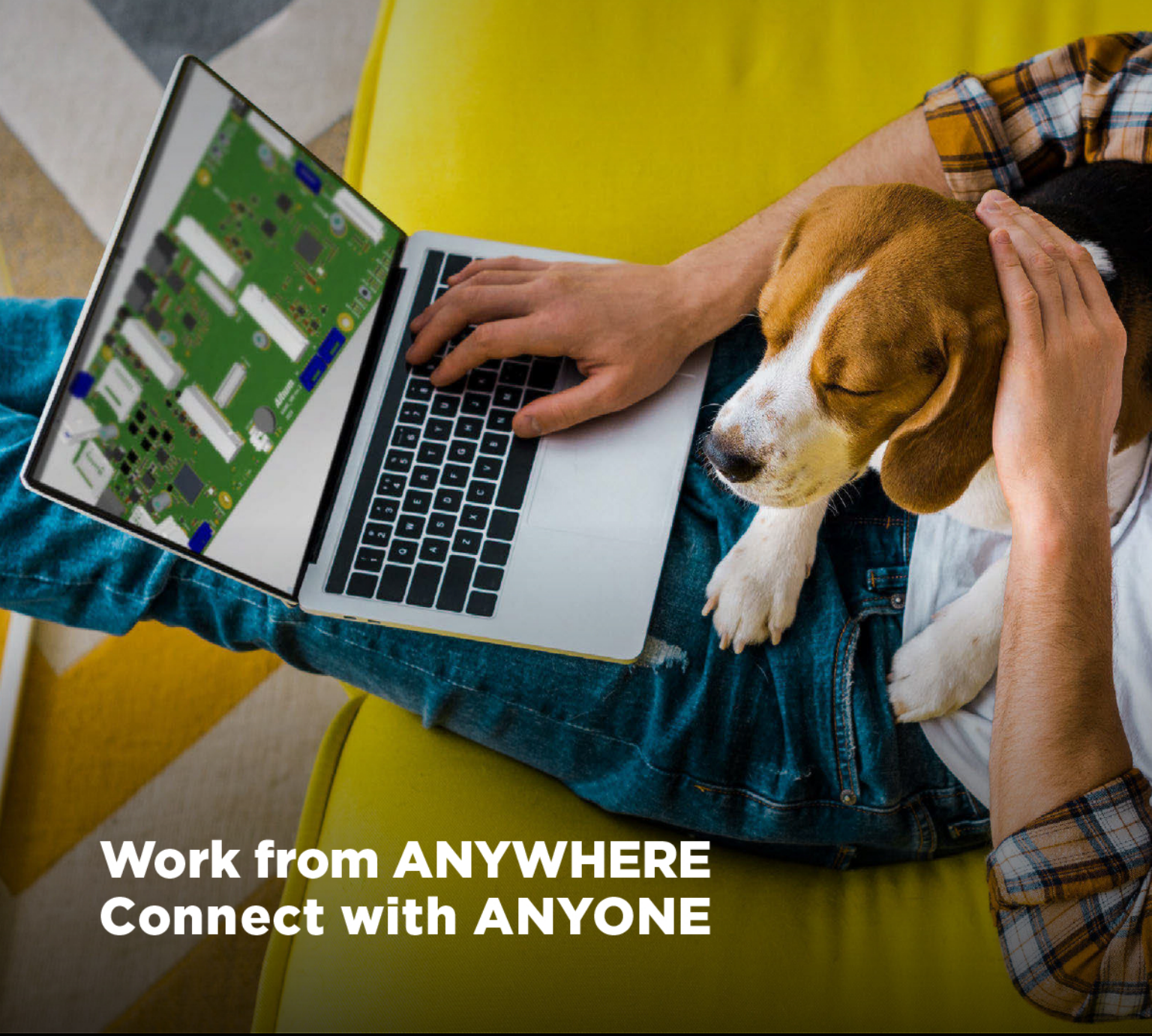
Also, in keeping with our five-tip format, I will take a closer look at options for the automated application of thermal interface materials (TIMs) and discuss the feasibility of using a high thermal conductivity encapsulation resin instead of a TIM. There are a number of environmentally friendly thermal management materials available these days, so I will also examine ways to improve your green credentials, as well as demystify the importance of bulk thermal conductivity.

Without further ado, let's get started with the new advances in thermal management.

1. What are the latest advances in thermal management technology, and how do these products differ from some of the more traditional pastes and greases?

Thermal pastes and greases have been leading the way in thermal management for many years and are expected to do so for many more years to come. Pastes are easy to apply and rework whilst providing a cost-effective alternative to thermally conductive encapsulants. However, make way for the new kids on the block: phase change materials (PCMs).

Once heated above their phase change temperature, PCMs become highly thixotropic liquids that perform as well as—and sometimes even better than—a traditional thermal grease. Moreover, their low phase change temperature ensures low thermal resistance over a wide temperature range and safeguards minimal bond line thickness with improved stability. With phase change technology, a key benefit is



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the greatly reduced effects of pump out, making PCMs an excellent choice for applications that undergo widely varying temperatures.

The application methods of PCMs for high volume production mean that most can be utilised in existing production processes with minimal—if any—changes, whilst also allowing for easy rework, offering many of the same benefits of traditional thermal pastes. PCMs offer greater long-term stability compared with thermal greases as they are better suited to thermally challenging applications where product life expectancy and reliability may be critical, such as automotive/aerospace electronics or remotely-located wind power inverters. Traditional thermal pastes/greases will continue to be a popular choice, although for some applications, especially those requiring greater long-term stability, a PCM is likely to win over the crowd.

2. What are the options for the automated application of thermal management products?

Automated applications involve the use of specialist equipment that typically consists of an applicator head where the material is fed to the applicator via dispensing equipment. Due to the high viscosities of the thermal management materials, the dispensing equipment is usually a follower-plate system that connects to the thermal paste container as supplied. In addition, automated stencil and screen applicators are widely used. For example, we work with a number of local and international equipment manufacturers.

3. When would I feasibly require an encapsulation resin with high thermal conductivity?

Electronic components and devices will produce varying levels of heat during their operation. Where significant amounts of heat are generated, intervention in the form of thermal management may be required to prolong working life and increase reliability. For certain types of applications, it may be beneficial to encapsulate the whole device in a heatsink enclosure using a thermally conductive encapsulation resin. This method offers both heat dissipation and protection from the surrounding environment, such as high humidity or corrosive conditions.

Once again, it is important to ensure that no air inclusions occur during the potting operation, as these will interfere with heat transfer to the metal case. Mineral fillers used in some resins systems have a higher thermal conductivity than the resin base, so filled resins are better than unfilled resins, as far as thermal control is concerned. The higher the filler level, the higher the thermal conductivity. However, higher filler levels will lead to higher viscosity and a greater possibility of air inclusions in the potting.

4. What options are available for more environmentally friendly thermal management products?

In recent years, we have seen demand increase for more environmentally friendly products across all our product groups. However, within the thermal management range, we have developed a high-performance thermal management paste that is entirely free from zinc oxide (ZnO). The non-silicone heat transfer compound is recommended for applications where the use of zinc oxide is restricted; for instance, in the marine industry, ZnO is a pollutant, and silicones are prohibited in places like offshore utilities. HTCX_ZF is a highly stable, non-curing paste that enables simple and efficient rework of components (if needed) and is recommended where efficient and reliable thermal coupling of electrical and electronic components is required, as well as between any surface where thermal conductivity and heat dissipation is important.

5. What is the importance of a bulk thermal conductivity value?

The initial selection of suitable TIMs for testing is often conducted based on high bulk thermal conductivity, indicating the efficiency

of heat transfer through the TIM itself. However, bulk thermal conductivity alone could give a false impression of the expected performance. When tests are conducted under application conditions, low thermal resistance of the device indicates the true heat transfer efficiency of the TIM.

Conclusion

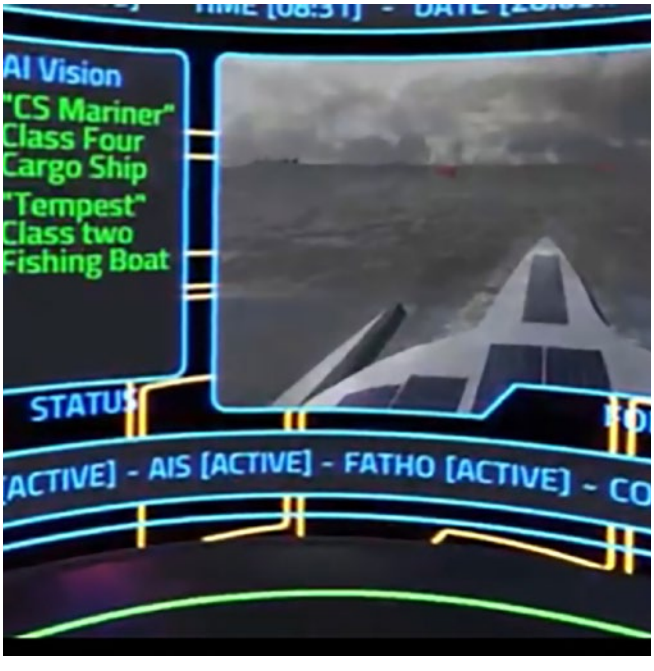
It can be a complex process deciding on the right choice of material and/or application technique regarding thermal management products. I strongly recommend getting expert advice before settling on any particular material or method. I hope this month's column has shed some light on current thermal management issues. **DESIGN007**

Jade Bridges is global technical support manager at Electrolube. To read past columns from Electrolube, click here. Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments*, and watch the micro webinar series "Coatings Uncoated!"

Mayflower Autonomous Ship Launches

Ocean research non-profit ProMare and IBM have announced the completion and launch of the Mayflower Autonomous Ship (MAS), an AI- and solar-powered marine research vessel which will traverse oceans gathering vital environmental data.

Designed to provide a safe, flexible and cost-effective way of gathering data about the ocean, the new-generation Mayflower promises to transform oceanography by working in tandem with scientists and other autonomous vessels to help understand critical issues such as global warming, micro-plastic pollution and marine mammal conservation. ProMare is coordinating the scientific studies working with IBM Research and a number of leading scientific organizations.



MAS features an AI Captain built by ProMare and IBM developers, which gives MAS the ability to sense, think and make decisions at sea with no human captain or onboard crew. The new class of marine AI is underpinned by IBM's latest advanced edge computing systems, automation software, computer vision technology and Red Hat Open Source software.

To enable followers around the world to stay updated with MAS as it undertakes its various missions, IBM and ProMare have today launched a new interactive web portal. Built by IBM iX, the business design arm of IBM Services, the MAS400 portal is designed to provide real-time updates about the ship's location, environmental conditions and data from its various research projects. Live weather data will be streamed from The Weather Company, as MAS is receiving forecast data and insight from the new IBM Weather Operations Center.

The portal even features a seven-armed, stowaway octopus chatbot called Artie, who claims to be hitching a ride on the ship. Powered by IBM Watson Assistant technology and created in partnership with European start-up Chatbotbay, Artie has been trained to provide information about MAS and its adventures in a lively, and accessible format.

MAS will spend the next six months in sea trials before attempting to cross the Atlantic in Spring 2021.

(Source: PR Newswire)

How the HIR Impacts Design Through Assembly

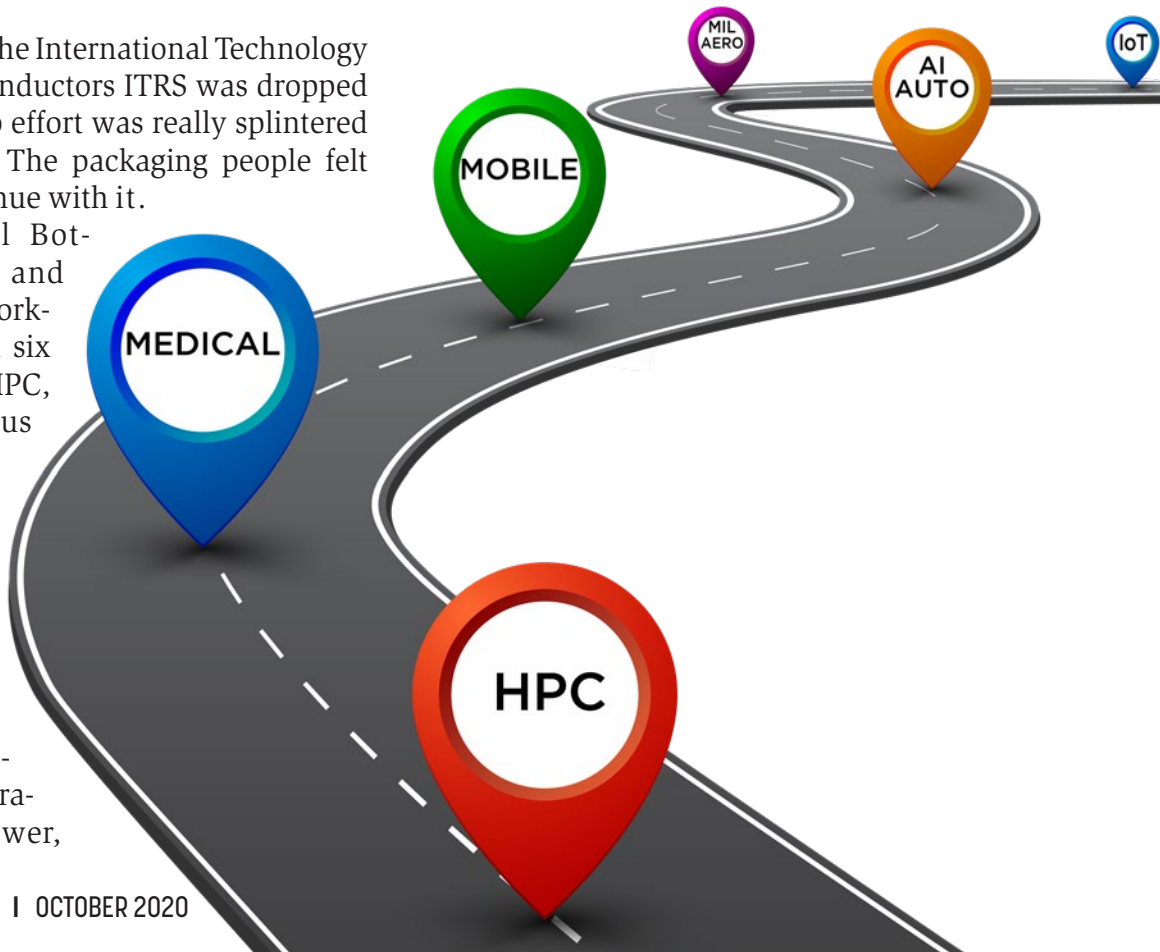
Feature Interview by the I-Connect007 Editorial Team

In this experts meeting on the Heterogeneous Integration Roadmap (HIR), the I-Connect007 editorial team met with Paul Wesling of the IEEE Electronics Packaging Society (EPS) to discuss what's in the HIR, where the organization is going with it, what the path is for the industry to have a roadmap like this, and how to use it in a practical sense.

Nolan Johnson: There is quite a lot of future technology in the HIR that will affect PCB design, fabrication, and assembly. Could you fill us in on how the HIR project began and provide us with an overview?

Paul Wesling: When the International Technology Roadmap for Semiconductors ITRS was dropped in 2016, the roadmap effort was really splintered into different areas. The packaging people felt that we should continue with it. Bill Chen and Bill Bottoms led that task and set up a bunch of working groups. We took six application areas: HPC, medical, autonomous automotive, mobile, aerospace and defense, and IoT. We have a chapter on each of these markets. Then, we have chapters on the various building blocks: single- and multi-chip integration, photonics, power, MEMS and sensors, and all of the 5G, analog, and mixed-signal stuff.

For the underlying technologies, we have a chapter on each of these, such as research materials and devices. A large section on future devices, such as carbon nanotubes, is from the Electron Devices Society (EDS). There are also small sections on supply chain and security. These are big issues across much of our IP, especially when there are various breakthroughs in the supply chain companies around the world, doing different things with PCB design, testing, integration, etc. We also cover thermal management, co-design, and simulation. How do we find CAD/EDA systems that will integrate from the transistor model all the way up to the PCB and the system level and pass information



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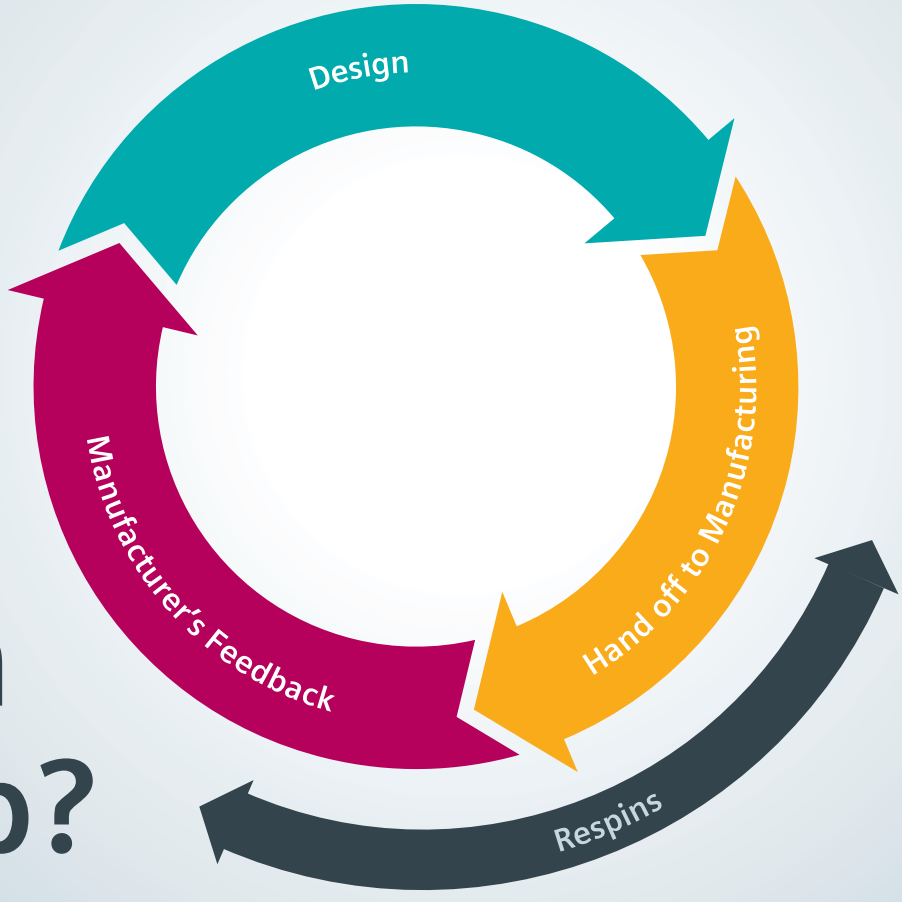

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back and forth, as opposed to doing it in silos today? We still have the same problem there.

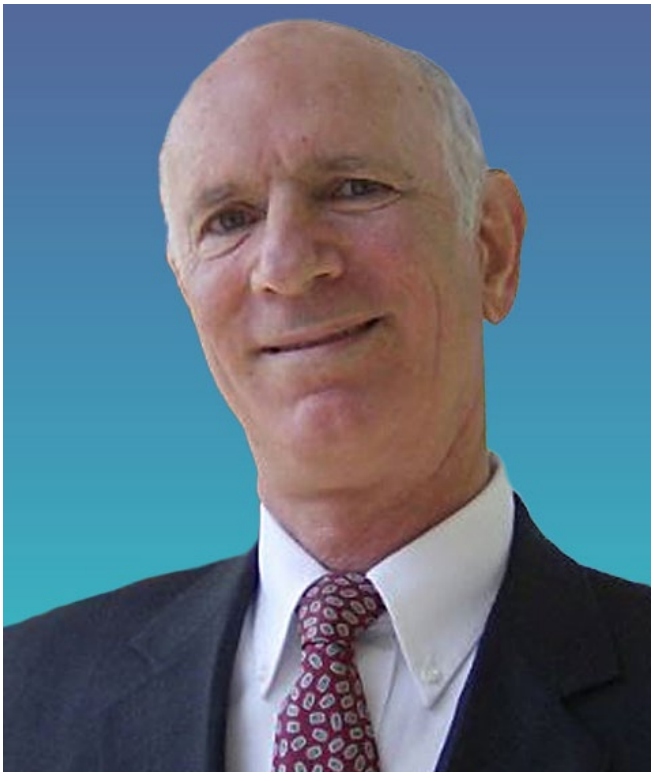
Finally, there are three technological areas. Perhaps the biggest focus areas are system-in-package (SiP) options, and where that's going over the next 10–15 years: 3D and 3D interconnect, and wafer-level packaging at the wafer-level, fan-in, and fan-out. It also covers module system integration and different substrates. That's my quick overview.

Johnson: How can people access it?

Wesling: On our website at pwesling.com/hir, you can pick out any chapter. In addition, there is a PDF of the full roadmap (>600 pages), or you can unzip it on your machine and have it locally with a full text search, which is kind of handy. It's the way I structure conference proceedings. You can also find a video overview that was prepared for ECTC and broadcast in June; it's a six-hour webinar with an index. For example, if you want to see what's going on with single- and multi-chip packaging, you can skip to the 176th minute, which will show a 10-minute summary by the head of that working group. We also have nine one-hour video overviews of many of the chapters that are more in-depth, and we're still working on similar videos for the other chapters.

Johnson: Some portions of the HIR directly apply to PCB fabrication; not all of them do, but some come pretty close. How is this roadmap intended to be used by the industry?

Wesling: There are four different groups that we see using this. First, research labs that need to look into the 10-year or 15-year period could use it. As we find out what they're doing, then we can reflect it every year or two in the roadmap and see what's integrating with other stuff. Second, the academic community could review it as well, such as Ph.D. students, depending on the projects on which they're working. Third, corporations that are either suppliers to this or users of it will want to keep an eye on it. They don't want to end up down a blind alley somewhere, working on a technology that does not seem to be getting support. Fourth, technologists can use it to ask, "Where should my career go in the next 10 years? If I'm working on high-level PCBs or things like that for power electronics, where do I see that integration for automotive electronics and 400-volt power distribution? Where is that going?"



Paul Wesling

We monitor these four communities because that's who could use this roadmap. Our next roadmap is supposed to come out soon. This is a large group of volunteers. But the idea is that we'll take the pre-competitive information that we can glean from our 400 or so volunteers and put it into updated roadmaps with, for example, new projections and issues with line width, or whatever it is we're tracking, and where it's going. We see it working for those four communities and being an interactive resource that's freely available, so we hope it gets passed around.

Johnson: A lot of information on the roadmap tends to be related to integrated circuits (ICs), which makes sense since much of the technology is now inside the packaging.

Wesling: It involves the chiplets and higher levels that are up and down the stack (Figure 1).

Johnson: Since our readers are primarily attuned to PCB manufacturing, how is the technology in the HIR going to change what happens on the PCB?

Wesling: First, I want to address co-design and simulation. We expect that instead of finding local maximums or optimization for IC layout and then having to have a lower level of optimization at the board level and system level, we hope to trade off across the whole stack of technology. We expect PCB people to be working backward with the IC and chiplet design. It will be a challenge for CAD/EDA companies to provide the tools.

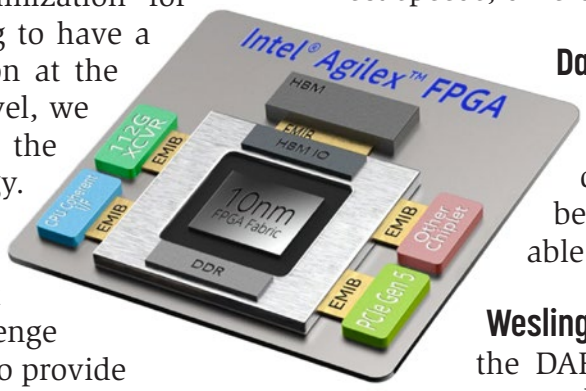


Figure 1: Intel Agilex FPGA Chiplet application. (Source: Intel)

Andy Shaughnessy: That's a fundamental change in how you do your job, who you communicate with, and what you communicate to them.

Happy Holden: We can't depend on Moore's Law any more. With five to seven nanometers for gate geometry, we're not getting all of our future gains by going to one nanometer, 0.1 nanometers, and 0.001 nanometers. The alternative would be putting multiple chips together in a different material, in some fashion, to make these future gains in performance and lower cost. It's not going to just be the single chip with all the horsepower of that single chip.

Wesling: We expect single chips to keep picking up more parts of the system, but the thermal and design and interconnect limitations aren't going to make that possible—except for special cases, high volume, or something like IoT. We expect to see better optimization. The board-level people must have models that can be extracted and pushed down to the chiplet level and the interconnects and the wafer-level processing stuff. There may be better models needed at the PCB level.

Testing is likely to change a lot. We hope to have a lot of known good die since it will be difficult getting access to things without having to scan in or scan out for all the parts at the board or the system level. There's going to be a testing issue, which is covered a lot in the test chapter. It may prove difficult for the board-level people to move to new materials, different interconnect speeds, different intra-process testing, etc.

Dan Feinberg: You mentioned chiplets quite a bit, which is relatively new. When do you recall chiplets first becoming commercially available in relevant places?

Wesling: Two years ago, I remember the DARPA thrust on chiplets. We would call them individual chips or subsets. Our roadmap covers both. We've adopted the idea that you have a bunch of chips and a bunch of passives, such as inductors and capacitors, and then make your system with interconnects.

Feinberg: Advanced Micro Devices (AMD) was the one that made great use out of it. They went from a lap behind Intel to a totally different racetrack because of chiplets. There are a lot of other uses for it, but what would you think is the driver? For me, the driver of chiplets has been the move toward 50- and 100-thread CPUs.

Wesling: Lisa Su, AMD's CEO and president, highlights that. It was their earlier generation, which we cover in the roadmap, that split that big chip into four chiplets to spread the power to make interconnect better and hook it up to memory better. That was an excellent application and probably the first major one we saw.

Aerospace and defense think chiplets will be their salvation for building systems because they can't build SOCs; they may only build 200 of their design. They need to use commercial chiplets and make their systems using your inter-

connects. Chiplets may become a moderately-used term, but we may also call it other things.

Holden: For me, this is an old topic because by 1972, we were putting multiple gallium arsenide LED dies on a PCB and wire bonding them over for second-generation calculators and things like that. Everybody thinks this is a 21st-century technology, but most of them aren't aware that back in the early '70s, we were doing a lot of chip-on-board and multiple chip-on-board.

Wesling: If you read chapter eight, you'll see that we still see wire bonding as a high-use application for bonding chips, three- and four-layer tiers, etc. Wafer-level packaging and flip chip may be coming in, but there's still going to be a lot of wire bonding.

Johnson: Happy's comments harken back to a time when all manufacturing took place at the same company. And because it was all under one roof, you could develop your own protocols and communications. It's different now. The various functional roles are fulfilled by third-party specialists. The need to communicate with multiple OEMs at the manufacturing level about this very detailed information is critical. For the PCB manufacturers, this technology could be the point where, no matter how well our systems work, they're going to break.

Wesling: That's why we've put in a supply chain chapter, which is not too developed, but we'll soon have one that's more extensive. One pain point is when only one company follows a standard. If we look back in five years to what we've published now, part of what we publish will not have been adopted. These are not standards; these are options for companies, consortiums, and university teams to get together and see if it works. Consequently, you'll see lots of potential solutions. Probably only a few will get implemented.

The other thing is in the supply chain. Our supply chain is spread out. Somebody does design, somebody does fabrication, and somebody else does assembly. This becomes a challenge in both supply chain and security. Looking into the crystal ball and knowing what will happen is the tough part. That's why this roadmap extends to about 600 pages because it covers lots of possibilities—not all of which are going to happen—that can keep people in jobs for the next 10 years, for example.

You want to look at how it affects what your focus is, which is substrates and PCBs, and—more specifically—do they go away and get replaced by some other multi-chip substrate? Does polymer end up going somewhere? Does low-temperature processing start coming in here? What kind of things do you see that you can pull out of here that might be interesting? Once you get some draft ideas, you might kick them back to the people in the working group—because they're all listed at the end of the chapter—and say, "I'm thinking this. Is that still what you're thinking?"

This morning, I thought, "This is going to be about setting the ground rules and projections, and then every few months, coming up with something else—either digging more deeply into something that wasn't covered before to say what could happen or correcting what you thought earlier." Over the next months, we hope to have many of the updated chapters out for the 2020 version. Several of the chapters are being fully rewritten, but most of them are just being updated.

Johnson: The change to heterogeneous integration and the use of chiplets really is based on using an interposer, which ties together unpackaged chips into a system. Is that basically a PCB inside the system-in-package (SiP)?

Wesling: Yes. It's between silicon and the next level—the interposer (Figure 2).

Johnson: The interposer employs an interconnect design methodology—more than you would normally use in an active piece of silicon. Does that mean that PCB designer experience is going to be valuable on the wafer design side? Do the design tools need to change?

Wesling: Things like that are analogous to what PCBs have done in the past but at much higher

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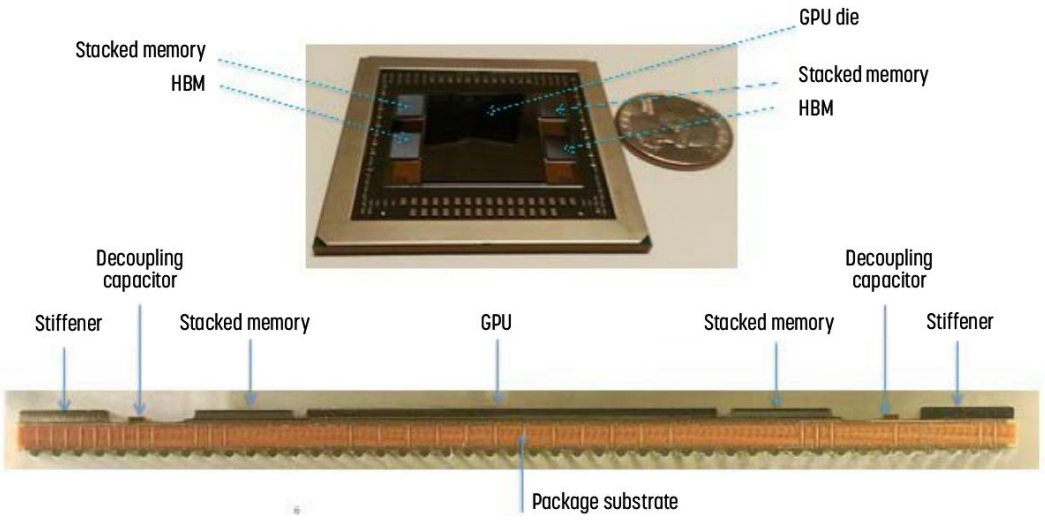

Figure 2: AMD Fiji GPU-HBM Si Interposer 2.5D Package. (Source: ASE)

densities. My guess is that the design function is going to be subsumed by the system-level packaging and substrate people rather than the PCB industry.

Holden: We don't have a roadmap, but it is also important to emphasize the other end of the spectrum. I believe in disposable electronics and printed electronics, such as a wristband that you can throw away when you're done using it. It would be made out of paper but designed with a five-cent chip to communicate with my smartphone and collect the information my doctor wants. Then it would upload data to AI that makes conclusions and tells my doctor to give me a call to come in if it doesn't like what it's seeing.

Wesling: It's printed roll to roll and extremely cheap, almost like a newspaper.

Holden: That's where some of our people in PCB manufacturing or flex will decide to invest in that part of the developing market.

Johnson: Thank you for your time, Paul. I hope you had a great time.

Wesling: This has been fun. **SMT007**

Bear Robotics, SoftBank Robotics Group Create Food Service Robot

Bear Robotics and SoftBank Robotics Group have collaborated to bring a new robot named Servi to the food service and hospitality field. This strategic partnership has brought together Bear Robotics' unrivaled robotics technology and SoftBank Robotics Group's vast experience in developing and commercializing service robots. Working together has allowed both companies to meet skyrocketing demand for these autonomous indoor robots in restaurants and other dining venues.

Servi has been developed to be a new member of the food service workforce to assist staff and elevate the overall customer experience. Servi's agility and object detection put its safety in a class of its own. This has resulted in significant interest in from the hospitality market in Japan, Korea, and the United States. Servi comes with additional features like bussing, drink delivery, and patrol mode. This will allow restaurant and dining hall owners to maximize their operating efficiency, while also elevating service quality to customers.

(Source: Business Wire)

MilAero007 Highlights

Standard of Excellence: Five Ways to Ensure You Have the Right Military PCB Supplier ▸

With the current shortage of qualified and certified military PCB suppliers, finding one has become more challenging than ever, and the trend toward consolidation over the past few years has only added to the shortage. Anaya Vardya shares five guidelines to consider when developing a bilateral relationship with your military PCB supplier.

ACDi Awarded Department of Defense Indefinite Delivery/Indefinite Quantity Contract ▸

American Computer Development Incorporated (ACDi) announced the award of an Indefinite Delivery/Indefinite Quantity (IDIQ) contract by the Department of the Defense, Department of the Navy, Naval Surface Warfare Center (NSWC) Crane Division.

AVX Supplies the First ESCC QPL Approved Polymer Electrolytic Multianode Capacitors ▸

AVX Corporation—a manufacturer and supplier of advanced electronic components and interconnect, sensor, control, and antenna solutions—is the first manufacturer qualified to supply polymer electrolytic multianode capacitors for use in European Space Agency (ESA) programs.

NASA to Highlight Artemis Booster Test With Live Broadcast ▸

NASA broadcasted a Space Launch System (SLS) rocket full-scale booster test at 2:40 p.m. EDT Wednesday, September 2, on NASA Television and the agency's website, followed by a media teleconference.

TT Electronics Awarded Team Tempest Contract From BAE Systems ▸

TT Electronics, a provider of engineered electronics for performance-critical applications, announced it has been awarded a contract from BAE Systems for the design, development, and qualification of a DC-DC Converter to support project Tempest. Harnessing TT's extensive engineering capabilities, this unit will be used within the Flight Control System (FCS) to deliver power conversion functionality to a number of elements within the FCS.

American Standard Circuits Offers New Thermal Management Micro eBook ▸

American Standard Circuits has recently released their newest micro eBook, *The Printed Circuit Designer's Guide to Thermal Management: A Fabricator's Perspective*. Part of the I-007 eBooks library, this is American Standard's fourth free downloadable eBook to date.

300 Below Selected as Top Team for U.S. Air Force Manufacturing Olympics ▸

300 Below Inc., recipient of 2019's Innovation of the Year in Manufacturing Technology, was announced as one of the top 92 participating teams selected from across the globe competing in AFWERX's Base of the Future Challenge, as a catalyst for fostering innovation within the U.S. Air Force (USAF) by using its technology to triple the life of at-risk metals for ~20% cost of the item.

Understanding MIL-PRF-31032, Part 3 ▸

Continuing with Part 3 of the discussion on understanding the military PCB performance standard MIL-PRF-31032, Anaya Vardya explains how the next step in the process is to create a technical review board (TRB) to oversee the quality plan.

FLEX007
A SPECIAL DESIGN007 MAGAZINE SECTION

Flexible Circuit Technologies Offers a Flex Roadmap for the Future

Interview by I-Connect007 Editorial Team

Andy Shaughnessy and Happy Holden recently spoke with two flex experts from Flexible Circuit Technologies: Carey Burkett, vice president of business development, and Mark Finstad, senior application engineer. They discussed their views on the future of the company and flex and rigid-flex technology, as well as the need for more flex training and educational opportunities.

Andy Shaughnessy: Carey, start by giving us a big picture view looking down the road for FCT, and then Mark can talk in more detail about the technology.

Carey Burkett: Flexible Circuit Technologies (FCT) has grown over the past five years, and we believe that trend will continue given the growing needs across all markets for the products and services that we offer. We provide design support services and produce flexible circuits, rigid-flex, flexible heaters, membrane switches, and plastic components. We offer expertise in EMS assembly services on flex and rigid-flex in producing assemblies, and take things further for our customers with product module builds all the way to complete product box builds.

Our optimism for continued growth has to do with the market drivers that we see across almost every industry. These trends include

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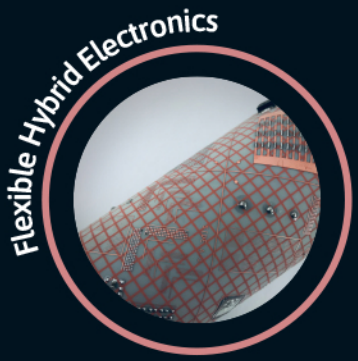

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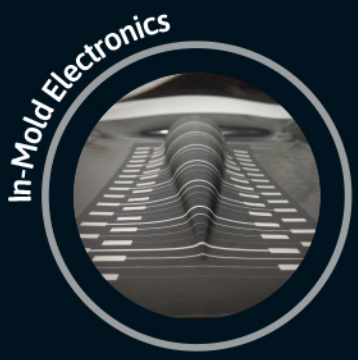

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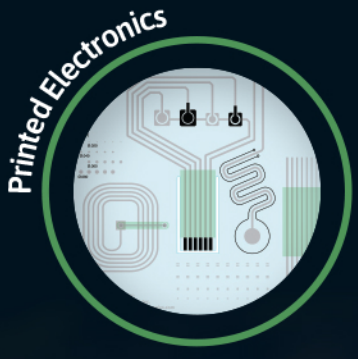

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Carey Burkett

miniaturization, IoT and connectivity, mobility, wearables, and requirements for high-speed data and increased signal integrity. These trends are also driving product designers toward the products and services that we offer.

For example, due to miniaturization, product development engineers are often required to pack more electronic capability into the same space or smaller spaces; this can lead to requirements for flex and/or rigid-flex circuits. Further IoT, connectivity, and high-speed data requirements across many industries are driving added needs. Beyond that, you have growing needs for devices based on mobility needs and, further, many wearable applications for a broad range of products. These trends continue to lead engineers to the types of solutions that we provide.

Another trend that we have responded to relates to customers moving from a transactional supply chain to a more value-added supply chain. Many OEMs are working to narrow their supply chain to a more manageable size. Given this trend, we have grown far beyond providing bare flexible circuits, rigid-flex, and flexible heaters. Today, as an EMS assembly organization, we offer expertise in assembly on flex, allowing us to meet increased needs for assemblies. Beyond providing assemblies, customers often seek more. We offer plastic components for our customers; again, we perform product module builds to complete product box builds.

We were already supporting the design and build of the circuit and assembly that usually becomes the heart of the product or device. It was a natural step to move beyond that to where we provide additional value-added services. We recently added a plastic molding company to our portfolio, as we are often required to attach the assembly to a plastic carrier, or we may be required to input the circuit into plastic housing.

We continue to respond to customer demands. Today, that is evidenced by doing complete product box builds for FDA-registered products. This demonstrates our ability to meet the robust quality and traceability requirements that these programs demand.

Our headquarters is located in the Minneapolis, Minnesota, area, and all of our production facilities are located in Asia. In Minneapolis, we recently partnered with a local company, HSIO. HSIO offers expertise in advanced high-performing circuits. They are continuously performing R&D as they push the envelope relating to advanced circuits, and they also perform prototyping to smaller-scale production for their customers. We are leveraging them as an R&D group and attaining learnings from HSIO that can be applied to our production facilities in efforts to take a significant leap forward in our capabilities as they relate to supporting customers with advanced, high-performing circuit requirements.

This relationship is very important, as we are in the process of building a new state of the art production facility in Zhuhai, China. Our new facility will include the very latest in industry equipment, and we will also leverage our learnings from HSIO as we seek to meet the increased demand for advanced circuits that require tighter trace and space, more complex via structures, improved signal integrity, and more. We are extremely excited about our technical direction and look forward to the opening of our new facility in the spring of 2021.

Shaughnessy: Where do you see your technology moving in the future?

Mark Finstad: We see a lot of high-speed requirements. That has become a significant driver when people are selecting vendors. To support these high-speed applications, our new facility will be set up to process high-speed, low-loss materials, such as LCP and PTFE. A lot of the equipment we purchased will cater to processing those different kinds of high-speed materials.

I haven't seen devices getting a lot smaller because everything has already been shrunk to where it's almost too hard to handle. But now they're just trying to put 10 times more functionality into the same sized package. What that means to us is that even though the circuit may not be getting smaller, all of the features in that circuit are getting smaller. The challenge is to be able to do that in high volume and in a good yield.

Shaughnessy: Do you see more people who are being squeezed into having to use flex for the first time? I see some companies switching to flex because rigid boards won't fit in the application anymore.

Finstad: In reality, most flex circuits aren't replacing the rigid boards; they're replacing wires, wiring harnesses, and cable assemblies. Many customers find that they are running out of room for discrete wires because they take up a lot of space. They also find that wiring harnesses can have wiring errors and can be hard to assemble. Flex ends up being a lot more reliable, and it takes up a fraction of the volume with much lower mass. It's just a much neater, more reliable package when you're all done.

Burkett: Absolutely. We see many companies being driven to these solutions, given the trends mentioned earlier. Often, engineers and designers do not have extensive experience in using these solutions, and there is a lack of true expertise in the supply base. Typically, customers and prospects come to FCT to obtain design consultation and guidance. We also are doing many educational webinars for customers and prospects in support of their efforts.

Mark Finstad

Shaughnessy: Do you get a lot of the new designers who have been designing rigid for 30 years and find they have to design their first flex circuit? Do they ask you what to do?

Burkett: We do. Typically, engineers seek guidance in the design phase. We encourage customers and prospects to seek design support as early on in the process as possible. Attaining experienced design consultation is where customers can gain significant savings, including cutting down the number of revisions to get to the final solution and attaining true cost-effective designs that will perform properly within the given application.

Given the rapid growth in the need for flexible circuits and rigid-flex, it has created a limited pool of true experts that can support customers with design expertise. Mark is our director of application engineering and co-chairs the IPC-2223 Flexible Circuit Design Committee; he is one of the top experts on the globe. Mark, along with our team of application engineers and our CAD team, offers 25–30 years of flex/rigid-flex expertise. Our group of

experts understands the materials, material properties, and what can and cannot be done, and their expertise is incredibly supportive to our customers in guiding them to a cost-effective solution that is manufacturable at higher yields and will perform within the given application. There's no doubt that design support is one of the most critical aspects of what we offer.

Finstad: We do a lot of training. I present at PCB West and IPC APEX EXPO every year, and we also do flex design training at a lot of smaller venues. I usually start by telling the class that I have them captive from anywhere from two to four hours, and I hope that they can retain some of what I talk about. But in the end, there's only going to be one person leaving that room as a flex design expert, and that's me. But I will also leave you with a great tool for when you have questions—my business card with my phone number. If you have a question, give me a call.

I still have customers from my military days who call me and have me review their drawings.

I still have customers from my military days who call me and have me review their drawings, even though we can't build the circuits because they're ITAR. I review the drawings and make sure that everything looks good because I don't want bad flex circuit designs out there.

Happy Holden: I was going to ask about LCP, but you mentioned that your new facility would focus on LCP and other new materials. Does that also include materials that would be suitable for wearables?

Finstad: It will include anything required for high speeds and low loss. That really seems to be the key factor there. I wouldn't steer anybody toward those materials if they are not required because they are more expensive. Recently, all of the big flex material manufacturers have come out with their own mix of low-loss materials, which laminate at more standard pressures and temperatures, allowing us to use existing equipment. If you look at the performance of these materials compared to thermoplastics, they're actually as good as, if not better than, thermoplastics.

As far as wearables, we have supported projects where we've used stretchable materials. These materials have not gained widespread acceptance in the industry yet, so processing knowledge is limited. We typically work with the customer in a developmental capacity to determine if those types of materials can be used successfully with an application that they might bring forth.

Holden: There are also highly flexible solar cells in the wearables so that they won't be burdened down with batteries, or the batteries will be flat printed electronic batteries.

Burkett: For wearables, we have addressed applications from head to toe. Certainly, there are added considerations that must be accounted for when designing for specific wearable solutions. We have utilized certain newer materials (i.e., stretchable materials and stretchable inks), and we are also keeping an eye on advancements that are being made within this space so that we can take appropriate steps in support of our customers.

Holden: Is the growing area of 3D and printed electronics beginning to be applied as a hybrid between what you're doing traditionally and what they would like to do but can't do yet?

Finstad: We do printed electronics, and we've been doing it for decades. Some of our biggest customers are in disposable medical applications for printed electronics. I have one very high-volume disposable medical application right now that uses a regular flex, all polyimide and copper. It's used one time in surgery and then tossed in the garbage.

Holden: One company in Michigan makes vitamins and nutrients, as well as cosmetics. A research area is in electrophoretic flexible masks to remove wrinkles; it's just a printed battery in a circuit. Their chemicals are electrophoretically driven into the skin, and once it's depleted, you can throw the whole thing away.

Finstad: We serve that market, too. There are a couple of products designed to create "micro-injuries" below the skin surface. This creates scar tissue, and it tightens everything; it's almost like a facelift without having any cutting done. You go in for these treatments, and a month later, you look 10 years younger. In some of these applications, the flex circuit is visible to the patient, so they want it to be visually appealing.

Shaughnessy: Mark, you and Nick Koop from TTM presented your flex class at the virtual PCB West. Tell us about that.

Finstad: It was good. We like doing livestreams. I've watched a few of them where I've just had to listen to a voice and look at the slides go through, and I lose interest pretty quickly. We wanted to do something that was livestreamed to bolster what we normally do because Nick and I both like interaction with the class.

There's going to be a learning curve in working with these virtual things, but overall, it went really well. We had good interaction. In the three hours we talked, we addressed 30–40 questions and had another 15–20 comments.

Burkett: We probably had 65–75 attendees.

Finstad: It was good. We started with total attendees in the upper 60s, and we retained them through the whole class. We never dropped under 60 for the entire three hours.

Shaughnessy: Do you think the virtual format is here to stay? It's not the same as a live event, but lots of people like it because they can watch while they're at work and they don't have to fly halfway across the country.

Burkett: We are doing a lot more events like that, and we're learning as we go. As you mentioned earlier, some of our attendees are being forced into flex. We put on a webinar on this topic, and we usually get really good attendance. The interaction is a bit different when compared to being on-site and in a classroom. That stated, our attendees have responded with very positive comments related to the training that we provide.

Shaughnessy: I appreciate both of you taking the time to do this.

Burkett: I enjoyed hearing some of your background and stories, Happy.

Holden: Thank you. Like you, I've been in this industry for a long time. We have a lot of stories to tell. **FLEX007**

Technology Roadmaps in the Electronics Industry

Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

Whenever the topic of roadmaps surfaces, I frequently quote the Cheshire Cat's exchange with Alice in Lewis Carroll's classic *Alice's Adventures in Wonderland*. If you've never read the book or don't recall the exchange, I refer to the point where Alice encounters the cat at an intersection which leads in many directions. The exchange goes as follows:

Alice: Would you tell me, please, which way I ought to go from here?

The Cheshire Cat: That depends a good deal on where you want to get to.

Alice: I don't much care where.

The Cheshire Cat: Then it doesn't much matter which way you go.

Alice: ...So long as I get somewhere.

The Cheshire Cat: Oh, you're sure to do that, if only you walk long enough.

While building technology roadmaps is not quite so lacking in purpose and direction, there are often similar discussions that take place when committee members try to chart a clear and certain path into the future in a constantly changing technical environment. It is not an easy task, and it is not always accurate, but having something to refer to (as opposed to nothing) provides a measure of comfort and a sense of future direction regarding where technology might be heading.

Over the last quarter-century, I have been personally involved with several electronics industry roadmaps focused on electronic interconnections with an emphasis on printed circuits, rigid and flexible, as well as assembly technology and connectors. To a fair extent, I have, on my own and with colleagues, tried to shape the road ahead of the roadmaps by developing new technologies that caused the roadmap to make an adjustment to its course. The development

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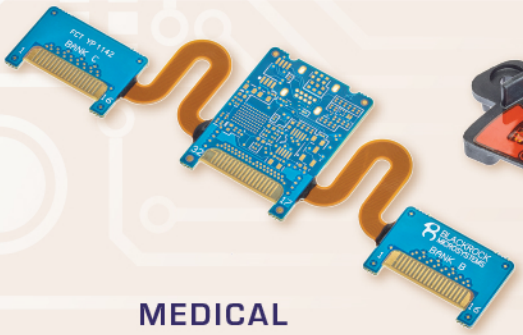

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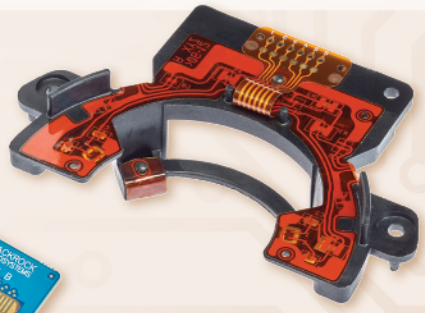

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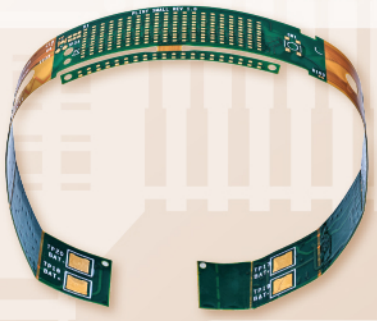

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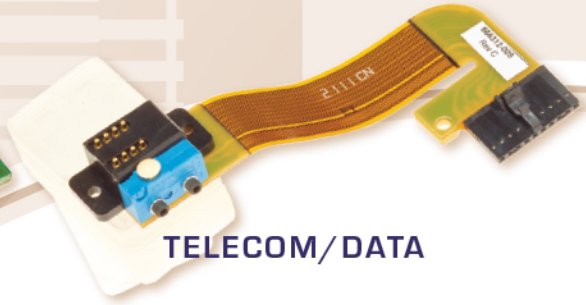

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of chip-scale packaging in the mid-'90s and the Occam Process idea are both easily identifiable "cases in point" in my career.

Most roadmap activity is a rather mundane exercise of extrapolating current technology trends. However, technology trends are not always linear. Often, they are punctuated with newer developments that, while not always foreseen, have future impacts and directions that were not fully appreciated at the time. More on this subject a bit later.

For printed circuit technology (like all electronics, in general), the mantra has always been "smaller, lighter, cheaper, better, faster." If you think critically about that hierarchy of desires and have some appreciation of science and engineering, and if you achieve the first "smaller" objective, all the other objectives fall in line. Smaller is lighter, cheaper, and faster, so it's automatically better.

Let's look at the most common metrics in PCB technology: minimum line-and-space size, minimum hole (or via) size, and circuit layer count. These circuit features have always trended down while operating frequencies have steadily risen. On the other hand, layer counts, the other major mechanical metric for PCBs, have typically risen, but they have also been going down. This stems from changes in component technology that have taken place over the years. In the 1970s, components were almost exclusively through-hole mounted and wave soldered into position. The problem was that if electronic products were to become smaller, components would need to be smaller, too, and/or more function would have to be carried out by larger components, which would be fewer in number.

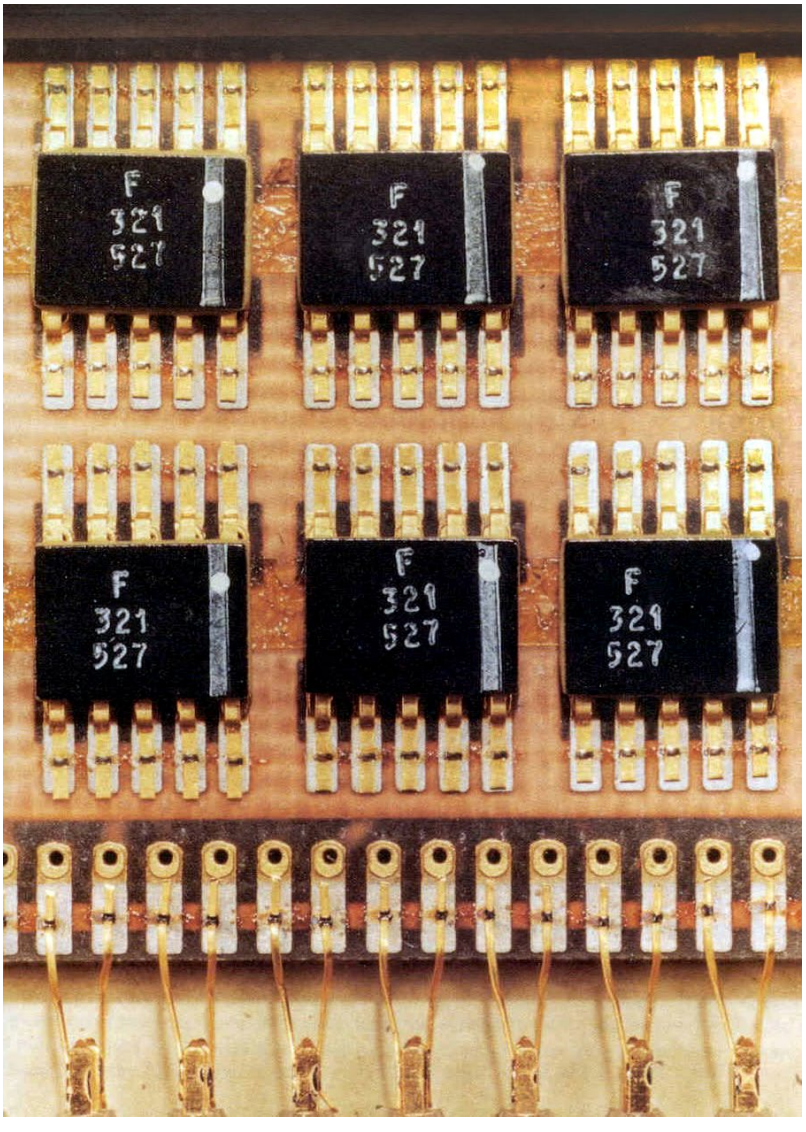
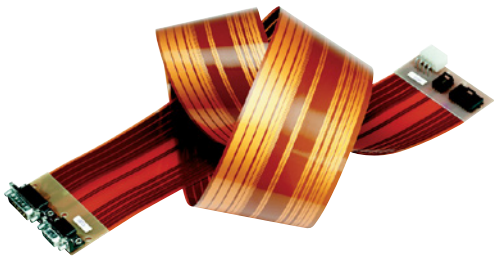


Figure 1: Apollo computer boards used surface-mounted IC packages. The dual in-line package (DIP) ultimately replaced it before it was upstaged by surface mount a decade later. (Source: NASA)

Enter surface-mount technology (SMT) in the 1980s (Fairchild Instruments' early IC packages in the 1960s were actually surface-mount devices and the Apollo, as shown in Figure 1).

Original SMT devices were those electronic devices where the component leads are provided on two or four sides of a smaller footprint device designed to be soldered directly to the surface rather than mounted through the holes drilled in a PCB. SMT ameliorated a good deal of electrical parasitic effects and returned a great deal of board space to the product developer because plated through-hole technology took up a surprising amount of area—something that has not always been fully appreciated.

Here is where we circle back to my earlier allusion to show how roadmaps can lead technologists down less than optimal technology roads



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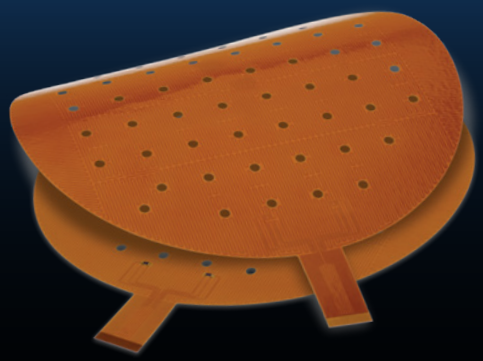

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to the future. Surface mount was and still is a good thing, but those seeking to provide a roadmap for future component termination pitches decided—by fiat—that every future lead pitch would be 80% of the previous one. Thus, 1.25 mm went to 1.0 mm, 0.8 mm, 0.65 mm, and 0.5 mm.

While this is completely arbitrary and seemingly harmless, it has had a knock-on effect, which had negative implications that are encountered daily by PCB designers. The myriad component pitches and formats cause uncounted headaches as designers try to interconnect devices with mixed pitches, land design rules, and redistribution of circuits to get through the maze of wires and terminations required to operate.

While it was a sad fact of life for peripherally leaded SMT components, carrying it over to area array component lead pitches was an even sadder oversight.

While it was a sad fact of life for peripherally leaded SMT components, carrying it over to area array component lead pitches was an even sadder oversight. With area array components, only a single common base lead pitch was required, and it could be depopulated as needed. However, since area array components followed the same defined roadmap path and progression, we have as many lead pitches for area array as for peripherally leaded devices. At the end of the day, it is completely unnecessary and even illogical.

Today, there are a few hundred-thousand package types and variations. Could it have been course-corrected in the process? Probably not. Business-oriented technologists were too wedded to the 80% rule convention, as deficient as it is from a design perspective. Could it still be changed? Perhaps. It remains to be seen whether the allure of the benefits of a standard grid is ever again fully understood and appreciated.

There is nothing stopping any package supplier from providing IC packages with terminations only on a fundamental grid pitch (including peripherally leaded components, but that takes a bit more care). At the end of the day, it is only a matter of desire and will on the part of the purveyors and the demand from enlightened customers. (If interested in digging into this topic, I recommend downloading a copy of *Solderless Assembly for Electronics: The SAFE Approach.*)

The Black Swan: The Impact of the Highly Improbable by Nassim Nicholas Taleb is a good book that should be read by anyone who desires to create a roadmap for an uncertain technological future (many great individuals in history have stated the difficulty associated with prediction, especially about the future). According to Taleb, a black swan is "a highly improbable event with three principal characteristics: It is unpredictable, carries a massive impact, and, after the fact, we concoct an explanation that makes it appear less random, and more predictable, than it was." The experience of chip-scale packaging seems to me to fit the description, perhaps the Occam Process idea will as well one day.

In the world of roadmapping, black swans are something we should always keep an eye out for; however, they have a way of sneaking in the door from time to time. I can only hope that we will welcome them rather than bar them at the door and hope they will go away. Roadmaps are, after all, about trying to forecast change, not to force or prevent change. **FLEX007**

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition,* and watch Joe's in-depth workshop series, 'Flexible Circuit Technology.'

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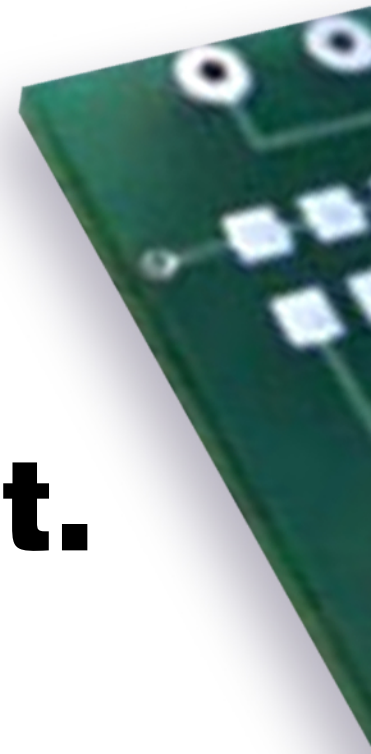

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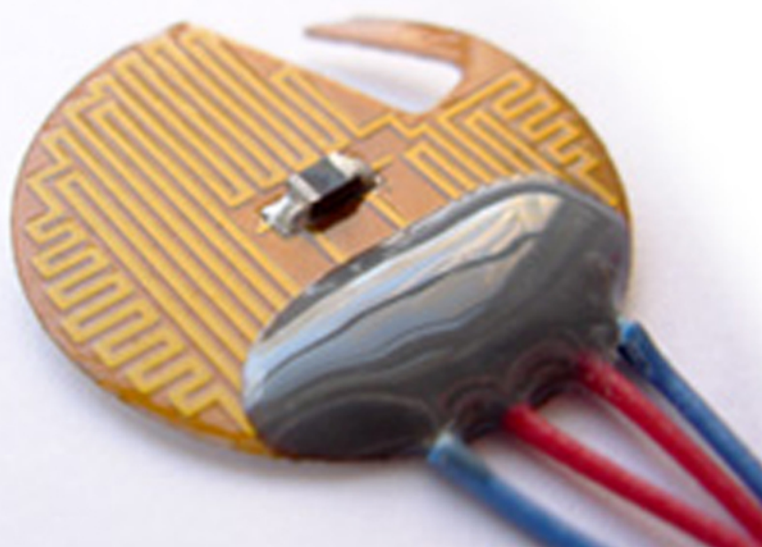

Flex007 Highlights

Documenting Your Flex Circuit Design ▶

As a flex circuit applications engineer, when Flexible Circuit Technologies' Tony Plemel receives an RFQ, the first thing he does is look at the customer's data and review their manufacturing notes. Quite often, he finds notes that supersede IPC specifications in manufacturing documents, as customers often believe these added notes and associated specifications will make the circuit more robust.

Consider This: Let's Talk About the Basics of Flex ▶

Flexible PCBs, by their very nature, are designed to be flexible. This presents problems in securely and reliably attaching the ends of the flex circuits to a solid, stiff, main PCB or other electronic devices. A combination of hard, as well as semi-flexible, stiffeners, is used for this purpose.

EPTE Newsletter: Circuit Board Shipments in Taiwan up Slightly ▶

The COVID-19 pandemic continues to disrupt the global economy. In this column, Dominique examines the impact on Taiwan. Taiwanese companies posted positive results compared to last year as manufacturing and exports increase.

Flexible Thinking: Thermal Management—Electronic Technology's Rodney Dangerfield ▶

Thermal engineering has, unfortunately, often been treated with less respect than it deserved. Dealing with the heat generated by electronics was often not given full consideration until after the design was completed and prototyped, and the problem manifests as a failure. Joe Fjelstad emphasizes why keeping devices cool is a vital objective.

Innovators Create Flexible, Printed Coil for Stringed Instruments ▶

The Purdue team's circuit board works in the same general way as a conventional electric guitar pickup: string vibrations cause the electromagnetic field to oscillate and induce a voltage in the stationary coil. The electric signal generated is then carried to a power amplifier and speaker.

Flex Talk: The Black Magic in the Business ▶

When you work with flex or rigid-flex, the communication between designer and fabricator needs to be impeccable, and the primary method of transferring information is through the fabrication notes. Tara Dunn gives a recommendation that, although not strictly required by the fabricator to build the product, will certainly benefit the end-user.

I-Connect007's Latest Innovation: Joe Fjelstad's E-Workshop on Flexible Circuits ▶

I welcomed the opportunity to enjoy a privileged preview of I-Connect007's latest innovation in technical webinars: a series of e-workshops covering structures, applications, materials, and manufacturing processes in flexible circuit technology with the industry's leading authority—Joe Fjelstad.

GTX Corp 4G LTE SmartSoles Gaining Interest ▶

GTX Corp, a pioneer in the field of health and safety wearable GPS human and asset tracking systems and personal protective medical equipment, announced it has begun taking pre-orders as field testing its new 4G LTE MB IoT GPS SmartSoles commences.

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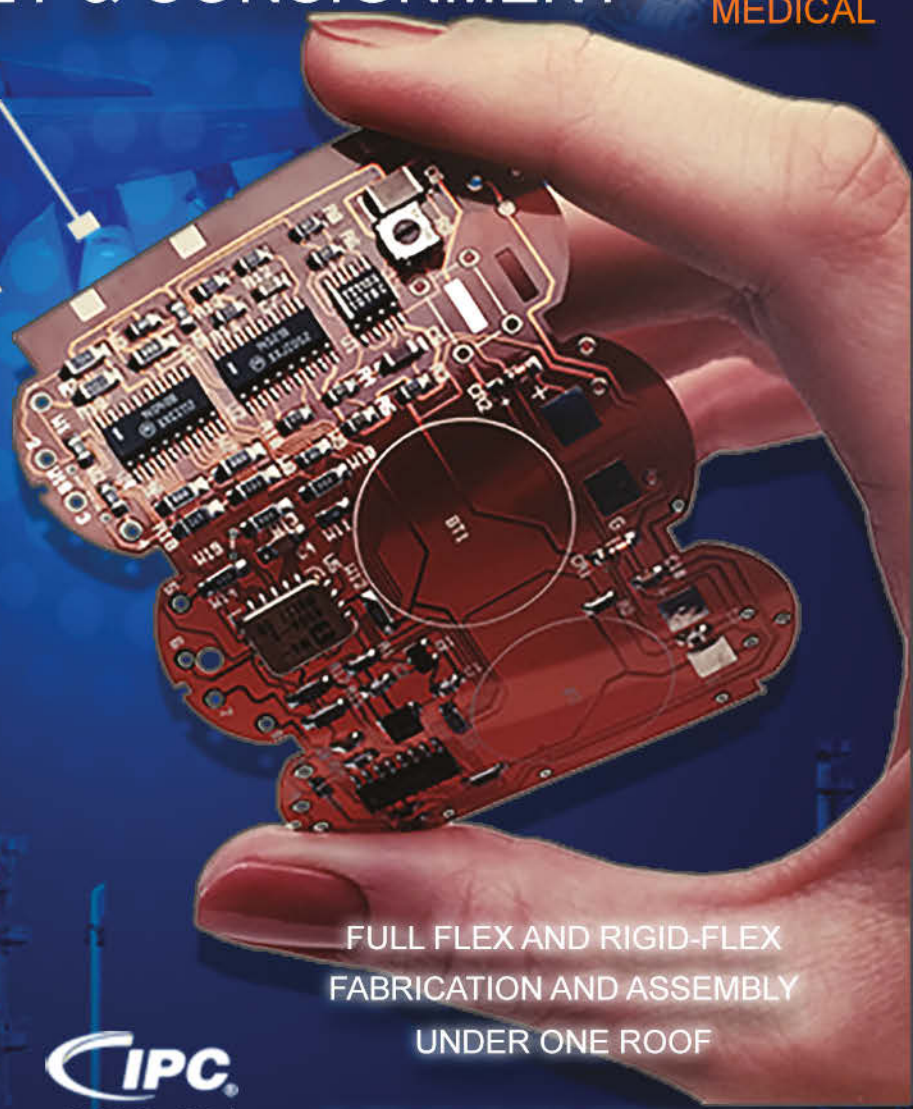

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Heavy-Copper Flex Circuits See Large Growth

Consider This

by John Talbot, TRAMONTO CIRCUITS

Flex circuits can be designed and manufactured to handle heavy currents. Thicker copper—3 oz. to 20 oz.—prevents true high cycle flexing. However, the circuit can be used in "bend to fit" and limited bend applications in high-current situations. Heavy copper—as thick as 20 oz.—has been manufactured in single-sided and double-sided applications. Multi-level flex copper circuits are used when the board must have a heavy, bendable copper section for power applications and a thin flex section for attachment purposes. This is similar to rigid-flex but all bendable, and some parts are as normally flexible (1 oz. RA copper).

The flex base material has a very high voltage breakdown rating of 2000 volts per mil of thickness, which allows higher voltage use in a thinner, bendable package. The heavy copper can present difficulty during the etching operation, as the etch solution will etch down through the thick copper, creating a tapered effect. Typically, the amount of sidewall width lost is 1.5–2 times the copper thickness. This etching undercut means your line width to space is much larger than a typical 1-oz. copper circuit.

A 6-oz. copper line and space minimum starting width is around 30 mils. When you start with a 30-mil-wide trace in 6-oz. copper, the final trace width will be in the area of a 20-mil-wide trace. This loss of sidewall width must be accounted for in your Gerber data. Additionally, the spaces will widen by the same formula, creating wider spaces between tracks. Each manufacturer has its own set of design rules for etching heavy copper. Before you start to design your heavy-copper flex circuit, talk to your flex PCB shop to make sure you understand their different production guidelines and heavy copper limits as to thickness, trace, and space etching losses.

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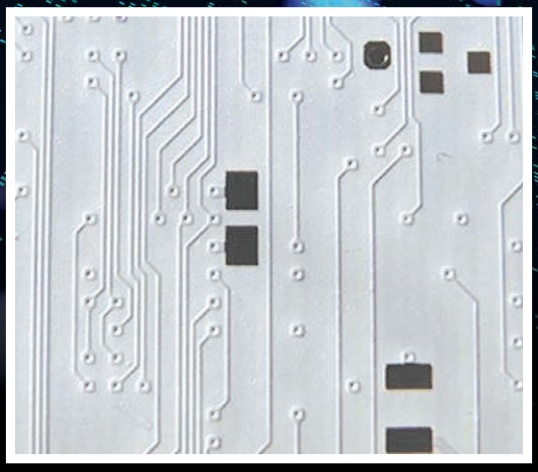

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The heavy-copper flex can have plated vias, as well as multiple traces and circuitry. Some heavy-copper flex circuits can have components designed onto the surface, although they must be placed clear of any bend area. Heavy-copper flex-based circuits are used in applications where a flat, stiff, circuit board will not fit. Typically, heavy-copper flex circuits are single- or double-sided circuits with simple, open designs. Crowded, highly populated circuits do not bend well because the components do not bend.

When designing a bendable, heavy-copper flex circuit, consideration must be given to the placement of the components. All components must be kept clear of the bend lines. If only a small bend radius is required, some components, such as capacitors, will allow a very small radius.

Multilayers are possible but with limits on layer counts and significantly decreased ability to bend. As a multilayer is a composite construction consisting of many layers, it imparts a larger stiffness in the inability of adjoining layers to move in relation to each other, creating a rather stiff but bendable package.

A typical flex solder mask or cover coat can be used. The solder mask must be sprayed or applied in such a way as to cover the sides of the tall, heavy-copper traces. When a cover coat is used, extra layers of glue sheets are used to fill the gaps in between the higher heavy-copper traces.

An additional use of bendable, heavy circuit boards is the creation of vertical surface buss bars made by combining the attributes of a bendable flex board with heavy copper and designing the fingers to be soldered into the main PCB. These heavy-copper fingers that protrude off the board are made by removing the flex material portion with a sculpting laser, leaving the copper behind (Figure 1).

A bendable buss bar can snake around the surface vertically, supplying power and carrying heavy currents. The base printed circuit could be less expensive—typically a 1- or 2-oz. FR-4 PCB with the vertical, bendable power board carrying the current. Thermal dissipation would be increased because the buss bar would be vertical, increasing the thermal shear and airflow. Single-layer, double-layer, and

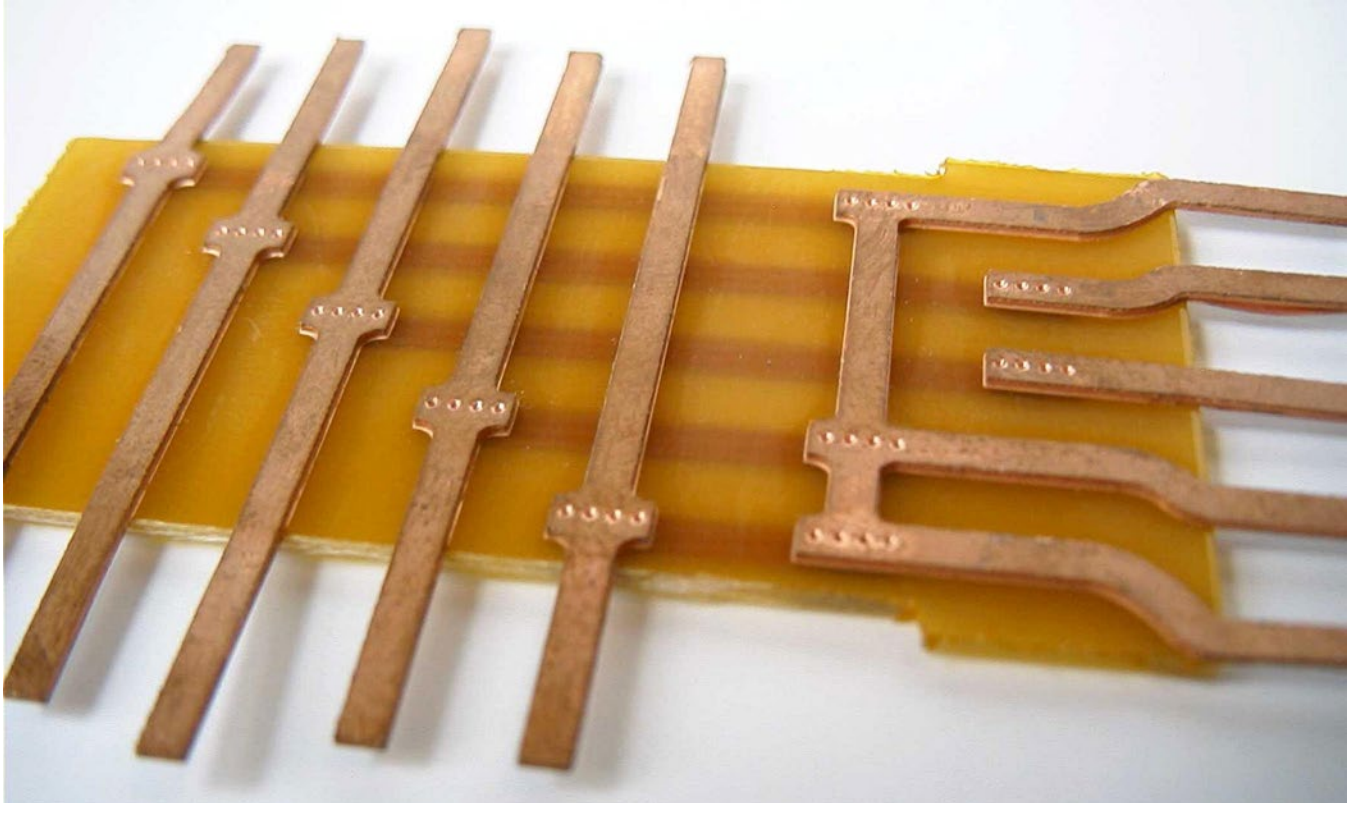
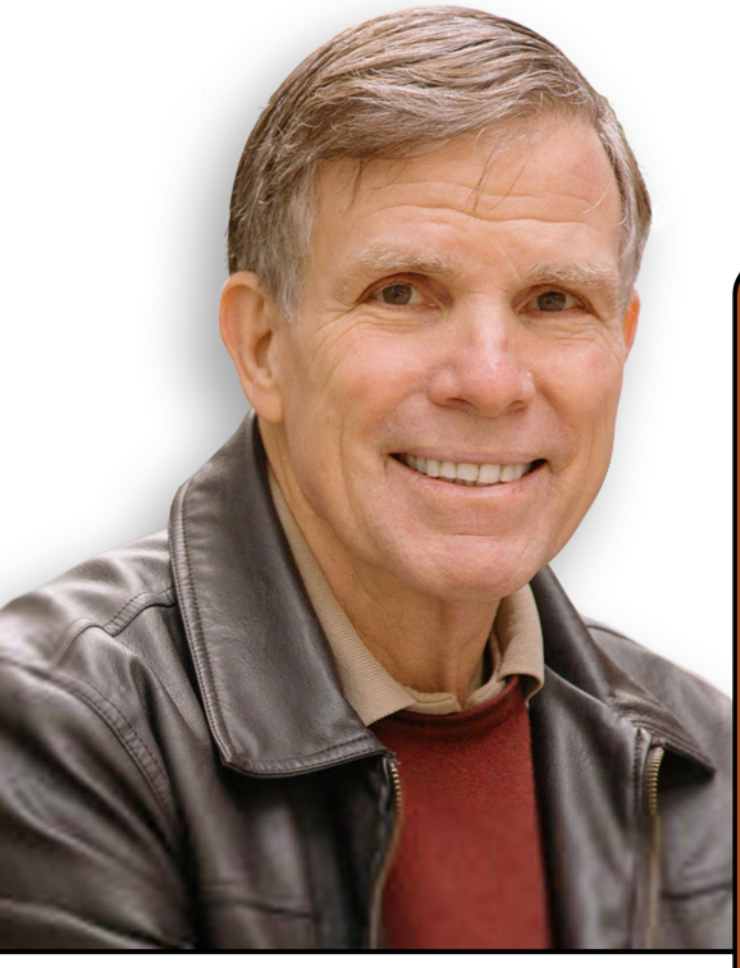


Figure 1: Heavy-copper leads off the flex PCB.

I-007e WORKSHOP



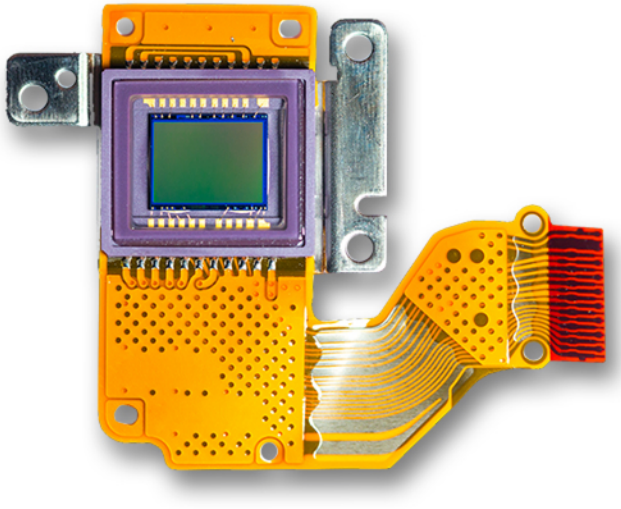
Online Training Workshop Series:

Flexible Circuit Technology

with Joe Fjelstad

This free on-demand workshop series is a comprehensive look into the structures, applications, materials, and manufacturing processes of flexible printed circuits.

START WATCHING



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multilayer designs could reduce the clutter and cost of a medium heavy-copper FR-4 PCB.

When designing bendable, heavy-copper flex buss bars, the copper must be thick enough to support the attachment fingers. The fingers could fit into a slot on the base FR-4 PCB or be surface mounted by bending the fingers at 90 degrees. A bendable, heavy-copper flex circuit can snake around the surface of a PCB, vertically supplying power and carrying heavy currents, creating a standard PCB with the bendable power board designed to carry the current throughout the entire rigid FR-4 PCB. Single, double, and multilayer heavy-copper flex designs could reduce the clutter and cost of a medium heavy-copper FR-4 printed circuit.

When a bendable, heavy-copper flex circuit is used for the previously noted PCB buss bar and plated with 10 oz. of copper, it will possess considerable strength. You can bend it into any shape, including 3D shapes, and it will retain that shape due to the thickness of the copper.

A bendable, heavy-copper circuit can withstand a small number of flex cycles. However, it is not designed to flex repeatedly. A properly designed and manufactured bendable, heavy-copper flex circuit of 6 oz. copper can bend as far as 360 degrees, in as little as one-inch diameter, for a few times—enough to shape and solder the heavy-copper flex circuit to the PCB base board. Some mechanical attachment device is suggested to keep the circuit in the desired shape if it utilizes 4 oz. of copper or less.

The heavy-copper, flex-based, buss bar can have plated vias, as well as multiple traces and circuitry (Figure 2). Some buss bars have components designed onto the surface, but they must be placed clear of any bend area.

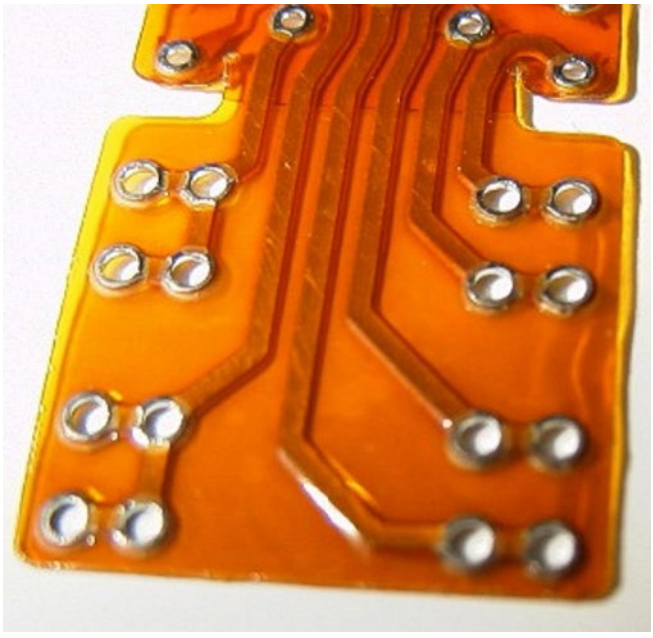

Figure 2: Heavy flex circuit with 6 oz. of copper on both sides.

When a heavy-copper flex PCB is used for a power supply, buss bar, and plated with 10 oz. of copper, it will possess considerable strength and weight with higher-than-normal reliability. **FLEX007**

John Talbot is president of Tramonto Circuits. To read past columns or contact Talbot, click here.

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Quality Engineer,
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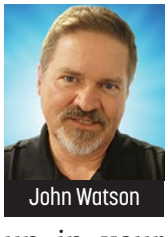
IPC

1 Lightning Speed Laminates: Utilizing mmWave Technology to Optimize High-Speed Designs ▶


John Coonrod

For the past several years, John Coonrod has been working with many different millimeter-wave applications. In this column, he shares areas where understanding the tricks of mmWave technology could help improve design and performance for very high-speed digital technology.

2 Elementary, Mr. Watson: Overcoming PCB Designs Pitfalls ▶


John Watson

When starting every PCB design, the hope is that we can navigate through any pitfalls that arrive. Unfortunately, many times, issues happen that you do not handle correctly; they fall through the cracks and end up in your PCB design. John Watson explains how that is when the real problems begin.

3 Beat the Heat With New Book on Thermal Management Design Processes ▶

Learn how to beat the heat in your designs with The Printed Circuit Designer's Guide to…Thermal Management: A Fabricator's Perspective—the latest title in our educational library.

4 Real Time With...I-Connect007: The App Notes and Fab Notes Roundtable ▶

Most of our readers are familiar with our Real Time With... video program. Now, Real Time With…I-Connect007 is turning the cameras around to focus on recent issues of our magazines. In this first installment, four of our recent contributors—Dana Korf, Jen Kolar, Mark Thompson, and Kelly Dack—review the June and August issues of *Design007 Magazine,* which covered app notes and fab notes, respectively.

5 Tim's Takeaways: Thermal Management for PCB Designers—Staying Out of the Fire ▶


Tim Haag

If there's one thing in life that really feels the pressure of being in the hot seat, it's the PCBs that we design. But PCB designers often feel a lot of pressure while doing their work, which puts them squarely in the hot seat. Tim Haag shares four techniques in thermal management for PCB designers.

6 Dana on Data: A Team Method to Reduce Fabricator Engineering Questions ▶


Dana Korf

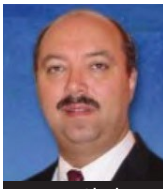
Hundreds of PCB designs are released to be quoted or fabricated every day around the world, and most will have engineering questions or technical queries generated once the data package has been received and analyzed. Dana Korf outlines seven fundamental steps based on Lean/Six Sigma concepts to reduce data transfer issues.

7 The Bare (Board) Truth: 5 Questions About Improving Thermal Management ▶


Mark Thompson

Mark Thompson from Monsoon Solutions answers five questions about thermal management at the design and PCB levels, including how much heat a via dissipates, how to identify potential thermal issues, and more.

8 Mentor and Z-zero Collaborate on New Stackup Tool ▶


Max Clark

I recently spoke with Max Clark, business unit manager with Mentor, a Siemens Business, and Z-zero founder Bill Hargin about the newly formed partnership that resulted in a new stackup tool that Mentor is now selling worldwide. Fun fact: Hargin used to work for Mentor as part of the HyperLynx team, which now has an interface with Z-planner Enterprise.

9 This Month in *Design007 Magazine*: Thermal Fundamentals With Mike Jouppi ▶


Mike Jouppi

The I-Connect007 team recently interviewed Mike Jouppi, one of the champions of thermal management in PCBs. Mike spent decades working on updating the old IPC current-carrying data, which dated back to the 1950s, and he is the primary architect behind IPC-2152—the standard for determining current-carrying capacity in printed board design.

10 Quiet Power: Be Aware of Default Values in Circuit Simulators ▶


Istvan Novak

Simulators are very convenient for getting quick answers without lengthy, expensive, and time-consuming measurements. Istvan Novak explains how, sometimes, you can be surprised if you forget about the numerical limits and the limitations imposed by internal default values.

Career Opportunities

Fetching New Team Members

Find industry-experienced candidates at I-Connect007.

For just $750, your 200-word, full-column ad will appear in the "career opportunities" section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs, and suppliers.

In addition, your ad will be featured in at least one of our newsletters, and your posting will appear on our jobConnect007.com board, which is also promoted in every newsletter.

Potential candidates can click on your ad and submit a resume directly to the email address you provide or be directed to the URL of your choice. If you wish to continue beyond the first month, the price is the same per month.

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CIRCUIT FOIL

US Sales Manager

THE ROLE:

- To promote, sell and secure orders from existing and prospective customers in North America (USA, mainly, and Canada)
- To provide administrative help to our CFT Inc office in Glenside, PA
- To demonstrate our products to existing and potential customers and to assist them in selecting the copper treatments best suited for their needs
- To provide technical assistance to customers in case of claims, technical assistance, new product development
- To promote our products to OEMs
- To attend fairs (IPC, DesignCon,...), technical conferences (IPC 4562A,...) and customer presentations

THE PROFILE:

- Master's degree in engineering, with experience in technical sales
- At least 5 years of relevant experience in similar position
- PCB sales experience an advantage
- Very good knowledge of all product/services and international market regulations
- Knowledge of financial indicators
- Ability to work under pressure in order to meet deadlines
- Good organizational, planning, analytic, negotiation, presentation and people-management skills

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FTG

Chemical Process Engineer

Fredericksburg, VA

Scope:

Responsible for implementation and maintenance of chemical processes used to manufacture printed circuit boards.

Responsibilities:

- Research availability of chemical processes
- Write plan for process implementation
- Implement process and perform failure mode analysis to establish correct operating conditions
- Write all necessary procedures and instructions for process operation, maintenance and safety
- Monitor process operation on a daily basis to ensure consistency
- Perform failure and root cause analysis when product/process problems occur
- Perform chemical analyses on processes when required

Knowledge and Skills:

- Ability to read, write and communicate in English necessary to perform the job
- Knowledge and application of statistical techniques for process control
- Knowledge and application of failure mode effect analysis techniques as applied to process improvement and process development
- Ability to lift 25 pounds
- Will be exposed to hazardous waste while performing daily job duties
- Will undergo chemical handling training prior to start and will actively participate in ongoing hazardous waste and chemical handling training

Education and Experience:

- Bachelor of Science degree in chemical engineering or equivalent
- Must have general knowledge of methods used to train people in the operation and theory of the processes they operate

Salary negotiable and dependent on experience.
Full benefits package.

lisabradley@ftgcorp.com

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Career Opportunities

MacDermid Alpha ELECTRONICS SOLUTIONS

We're Hiring!
Connecticut Locations

Senior Research Chemist:
Waterbury, CT, USA

Research, develop, and formulate new surface treatment products for the printed circuit board, molded interconnect, IC substrate, and LED manufacturing industries. Identify, develop, and execute strategic research project activities as delegated to them by the senior research projects manager. Observe, analyze, and interpret the results from these activities and make recommendations for the direction and preferred route forward for research projects.

Quality Engineer:
West Haven, CT, USA

Support the West Haven facility in ensuring that the quality management system is properly utilized and maintained while working to fulfill customer-specific requirements and fostering continuous improvement.

For a complete listing of career opportunities or to apply for one of the positions listed above, please visit us here.

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MacDermid Alpha ELECTRONICS SOLUTIONS

We're Hiring!
Illinois / New Jersey

Technical Service Rep:
Chicago, IL, USA

The technical service rep will be responsible for day-to-day engineering support for fabricators using our chemical products. The successful candidate will help our customer base take full advantage of the benefits that are available through the proper application of our chemistries.

Applications Engineer:
South Plainfield, NJ, USA

As a key member of the Flexible, Formable, and Printed Electronics (FFPE) Team, the applications engineer will be responsible for developing applications know-how for product evaluation, material testing and characterization, and prototyping. In addition, this applications engineer will provide applications and technical support to global customers for the FFPE Segment.

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Career Opportunities

Manncorp™

SMT Operator
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:

- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:

- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical trouble-shooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision
- Ability to lift up to 50 lbs. repetitively

We Offer:

- Competitive pay
- Medical and dental insurance
- Retirement fund matching
- Continued training as the industry develops

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ventec
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Customer Service Rep.
Near Chicago, USA

We have a great opportunity at Ventec's Elk Grove Village facility to join our customer services team as a customer service representative (CSR) to act as a customer liaison, manage incoming orders, order entry into ERP system, provide product/services information, and resolve any emerging problems that our customer accounts might face with accuracy and efficiency. As a CSR, you will provide a two-way channel of technical communication between Ventec's global manufacturing facilities and North American customers to ensure excellent service standards, efficient customer inquiry response, and consistent highest customer satisfaction.

Skills and abilities required for the role:

- Proven B2B customer support experience or experience as a client service representative
- Strong skill set in Excel, Word, and Outlook for effective communication
- Strong phone contact handling skills and active listening
- Customer orientation and ability to adapt/respond to different types of characters
- Excellent communication and presentation skills
- Ability to multi-task, prioritize, and manage time effectively
- High-school degree

What's on Offer:

- Excellent salary & benefits commensurate with experience

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits.

Please forward your resume to jpattie@ventec-usa.com and mention **"Customer Service Representative—Chicago"** in the subject line.

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Career Opportunities

MivaTek Global

MivaTek Global: We Are Growing!

MivaTek Global is adding sales, technical support and application engineers.

Join a team that brings new imaging technologies to circuit fabrication and microelectronics. Applicants should have direct experience in direct imaging applications, complex machine repair and/or customer support for the printed circuit board or microelectronic markets.

Positions typically require regional and/or air travel. Full time and/or contractor positions are available.

Contact **HR@MivaTek.Global** for additional information.

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Service Engineer
Schmoll Laser Drilling and Direct Imaging

Burkle North America seeks a full-time service engineer in the Northeastern U.S. This position will provide expert-level service on multiple laser drilling and direct imaging product lines. Install, commission, and maintain Schmoll products at multiple customer sites across the Northeast. The candidate will perform modifications and retrofits as needed. Maintain complete and detailed knowledge of Schmoll products and applications and handle a wide variety of problems, issues, and inquiries to provide the highest level of customer satisfaction. Assist customers with the potential optimization of their machine functions and work with clients on application improvements.

Qualifications

Required: Bachelor's degree from a technical college/university in an associated field. Three years directly related experience, or equivalent combination of education and experience. Must possess a valid driver's license and have a clean driving record.

Preferred: Experience in control systems and electronic troubleshooting, as well as in general electrical and mechanical service tasks. Experience and knowledge in the PCB manufacturing process, with a focus on laser drilling and/or direct imaging.

Send resume to hr@burkleamerica.com.

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Career Opportunities

LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Sales Account Manager

Sales Account Management at Lenthor Engineering is a direct sales position responsible for creating and growing a base of customers that purchase flexible and rigid flexible printed circuits. The account manager is in charge of finding customers, qualifying the customer to Lenthor Engineering and promoting Lenthor Engineering's capabilities to the customer. Leads are sometimes referred to the account manager from marketing resources including trade shows, advertising, industry referrals and website hits. Experience with military printed circuit boards (PCBs) is a definite plus.

Responsibilities

- Marketing research to identify target customers
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Providing ongoing service to the customer
  - Develop long-term customer strategies to increase business

Qualifications

- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is a leader in flex and rigid-flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Senior Process Engineer

Job Description

Responsible for developing and optimizing Lenthor's manufacturing processes from start up to implementation, reducing cost, improving sustainability and continuous improvement.

Position Duties

- Senior process engineer's role is to monitor process performance through tracking and enhance through continuous improvement initiatives. Process engineer implements continuous improvement programs to drive up yields.
- Participate in the evaluation of processes, new equipment, facility improvements and procedures.
- Improve process capability, yields, costs and production volume while maintaining safety and improving quality standards.
- Work with customers in developing cost-effective production processes.
- Engage suppliers in quality improvements and process control issues as required.
- Generate process control plan for manufacturing processes, and identify opportunities for capability or process improvement.
- Participate in FMEA activities as required.
- Create detailed plans for IQ, OQ, PQ and maintain validated status as required.
- Participate in existing change control mechanisms such as ECOs and PCRs.
- Perform defect reduction analysis and activities.

Qualifications

- BS degree in engineering
- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is the leader in Flex and Rigid-Flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

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- IPC certification a plus, but will certify the right candidate

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APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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Career Opportunities

Manncorp™

SMT Field Technician
Huntingdon Valley, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:
- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:
- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:
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- Retirement fund matching
- Continuing training as the industry develops

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For more information, click below.

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Understands all aspects of interconnect technical sales from PCB design and fabrication to assembly and all technologies from HDI microvias to flex and rigid-flex. Has also sold high-tech laminates and equipment. Proven record of sales success. He is looking for a full-time position.

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Specializes in running multimillion-dollar companies offering engineering, design, and manufacturing services. Proven leader. Supply chain manager. Expert at developing and implementing company strategy. Looking to lead a company into the future. He is looking for a full-time position.

PCB General Manager

Forty years of experience serving in all capacities, from GM to engineering manager to quality manager. Worked with both domestic and global companies. Available for turn-around or special engineering projects. He is looking for long-term project work.

Process Engineering Specialist

Strong history of new product introduction (NPI) manufacturing engineering experience: PCB/PCBA. Held numerous senior engineering management positions. Leads the industry in DFM/DFA and DFX (test) disciplines. He is looking for either a full-time position or project work.

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Worked with a very large, global company for a number of years. Built and managed international sales teams. Created sales strategies and communicated them to the team. One of the best sales leaders in our industry. He is looking for a full-time position.

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This professional has years of experience running PCBA companies. Led his companies with creative and innovative leaderships skills. Is a collaborative, hands-on leader. He is looking for a full-time position.

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Global Engineering Manager/Quality Manager

Has experience working with large, global PCB companies managing both engineering and quality staff. Very experienced in chemical controls. She is interested in working on a project-by-project basis.

CAM Operators and Front-end Engineers

These candidates want to work remotely from their home offices and are willing to do full-time or part-time projects.

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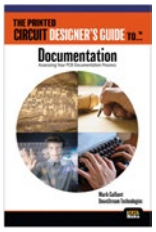
***Implementing "Digital Twin" Best Practices From Design Through Manufacturing with Expert Jay Gorajia,* a 12-part micro webinar series.**

I-007eBooks The Printed Circuit Designer's Guide to...

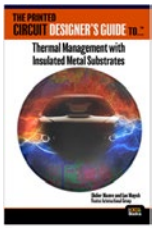
Thermal Management: A Fabricator's Perspective, by Anaya Vardya, American Standard Circuits
Beat the heat in your designs through thermal management design processes. This book serves as a desk reference on the most current techniques and methods from a PCB fabricator's perspective.



Documentation, by Mark Gallant, Downstream Technologies
When the PCB layout is finished, the designer is still not quite done. The designer's intent must still be communicated to the fabricator through accurate PCB documentation.

Executing Complex PCBs, by Scott Miller, Freedom CAD Services
Designing a complex circuit board today can be a daunting task. Never before have PCB designers on the cutting edge faced more formidable challenges, both electrical and mechanical.

Producing the Perfect Data Package, by Mark Thompson, Prototron Circuits
For PCB designers, producing a comprehensive data package is crucial. If even one important file is missing or output incorrectly, it can cause major delays and potentially ruin the experience for every stakeholder.



Thermal Management with Insulated Metal Substrates, by Didier Mauve and Ian Mayoh, Ventec International Group
Considering thermal issues in the earliest stages of the design process is critical. This book highlights the need to dissipate heat from electronic devices.

Our library is open 24/7/365. Visit us at: I-007eBooks.com

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