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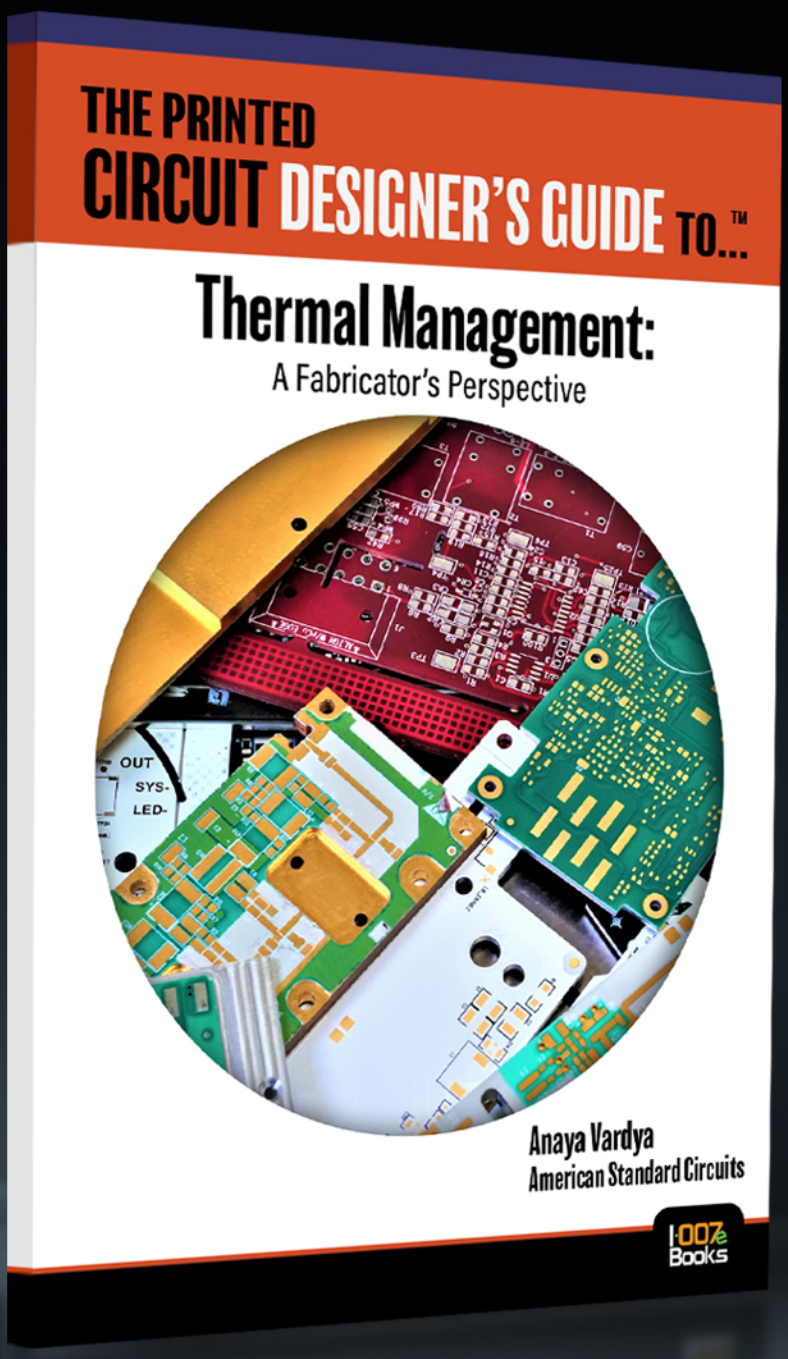

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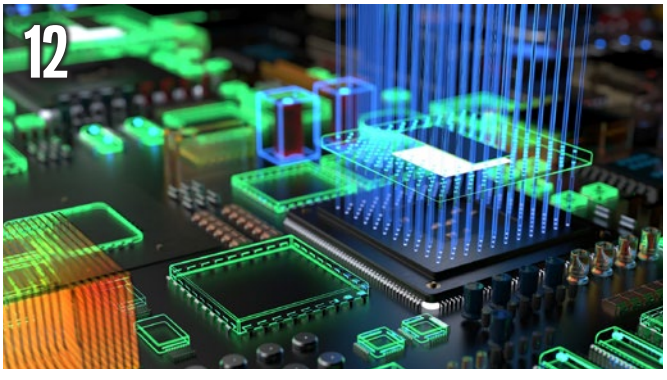
The Simulation Issue

When we started speaking with SI experts for this issue, we were surprised to find that there were several schools of thought regarding simulation. Should you try to get by without simulating your design and only call a third-party consultant when it's almost too late? Should your company invest in a simulation tool, which also means hiring someone with years of experience to operate it? Or should you eliminate the need for simulation from the start by managing your electromagnetic fields properly? This month we asked some of the industry's premier experts on simulation to weigh in on this critical topic.



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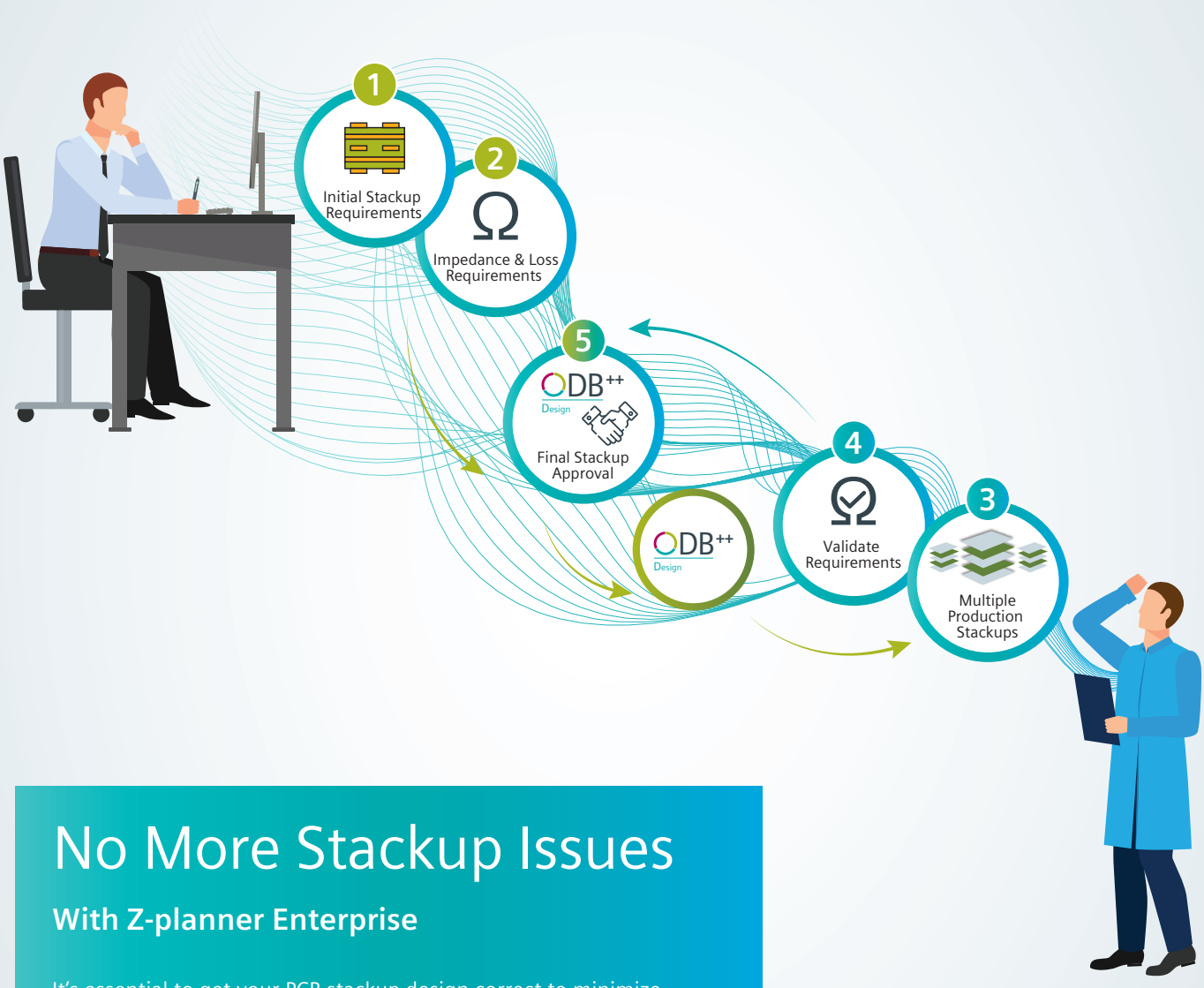

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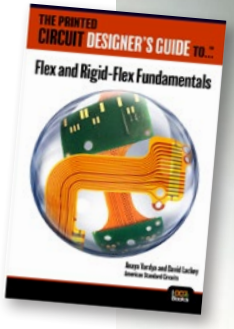
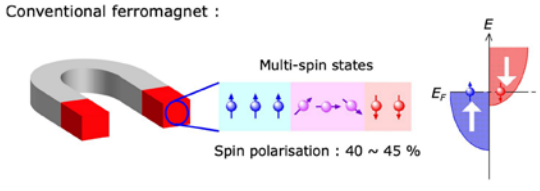
FLEX007

This Month in Flex

There are a variety of ways to terminate and connect a flexible circuit to a rigid board. But the stress on the flex circuit must be considered to avoid broken connections, and many flex connectors come with long lead times. This month, we look at some of the best techniques for terminating flexible circuits. One tip: Work out your connection strategy well in advance of beginning the design process.





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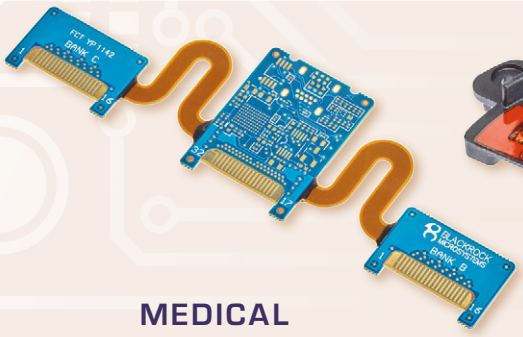

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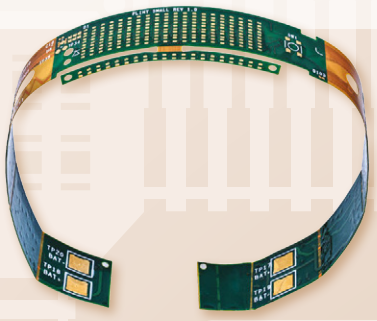

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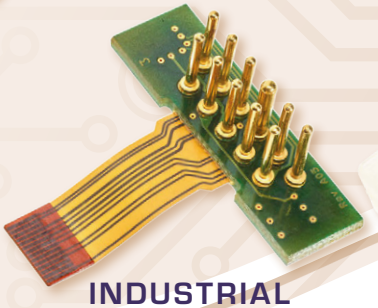

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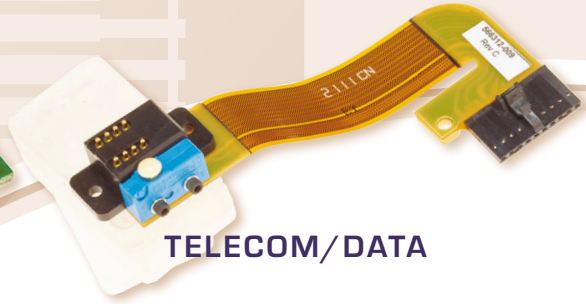

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A Simulating Conversation

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

Simulation tools come in handy, and not just when you're designing a high-speed PCB. They're also a great conversation starter at a trade show. I'm talking about the live kind of trade show with a group of PCB designers and design engineers standing around a coffee break table eating stale conference bagels. (My kingdom for a stale conference bagel!)

Yes, simulation tools rank right up there with design data standards and China in terms of starting a conversation—or an argument—at a conference.

Here's how it usually works. I'll ask, "How many of you primarily work on high-speed designs?" Typically, it's a solid majority. How many of you are designing boards that are not high-speed?

Then I'll ask, "How many of you use simulation?" Out of 15 designers, maybe three hands will go up, and the whole group will chuckle knowingly.

So, I'll follow up with, "Why don't you use simulation?" Answers often range from "It's really expensive" to "We just hope for the best" and "Don't get me started. It's complicated."

Apparently, it is complicated.

Then there are the simulation tools themselves, which are expensive and infamous for their steep learning curves. You can't park a recent EE grad in front of an enterprise-level simulation tool and expect greatness. As Barry Olney points out in his feature interview this month, even today's entry-level simulation tools are not simple to use and require the user to have a solid signal integrity background to get good results.

All of this sounds like the makings of a perfect storm. If the tools are expensive and hard to use, maybe you can get by without them, right?

When we surveyed designers and design engineers about their biggest challenges, sim-

ulation was a popular answer. Some respondents said that their design teams didn't fully understand how to operate simulation tools, while others faulted their company for not using simulation at all or waiting until the design was far behind schedule before sending the job to a third-party SI consultant. Comments included, "Management always budgets for re-spins" and "Time-to-market stresses won't allow simulation." Of course, if you fail EMI, your time to market is a moot point.

When we started speaking with SI experts for this issue, we were surprised to find that there were several schools of thought regarding simulation. Should you try to get by without simulating your design and only call a third-party consultant when it's almost too late? Or should your company invest in a simulation tool, which also means hiring someone with years of experience to operate it?

Plus, there is another viewpoint put forward by Dan Beeker: If you design your board correctly from the start and manage your electromagnetic fields properly, you may be able to eliminate the need for simulation altogether. Is your company already practicing this approach?

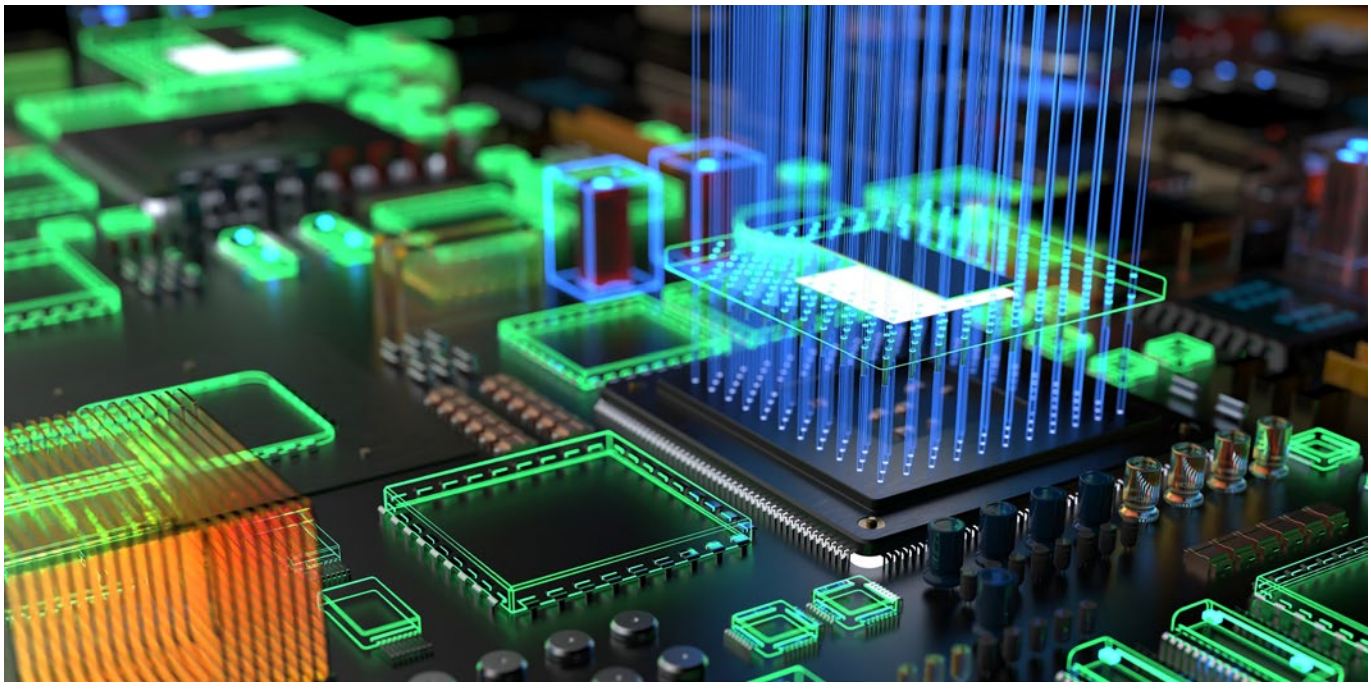
So, this month we asked some of the industry's premier experts on simulation to weigh in on the topic. First, we have an interview with Barry Olney of iCD, who lays out when and why engineers need to use simulation, what they need to measure, and why it takes years to master most simulation tools. Then, we have a conversation with Todd Westerhoff of Siemens EDA that covers simulation from the EDA tool company viewpoint, including some of the reasons why some companies ignore simulation, often until the 11th hour of a complex design.

Next, Martyn Gaudion of Polar Instruments discusses the simulation of stackups, and why results are only as good as the source data. Bill Hargin of Z-zero takes a philosophical approach, beginning with a question he asks conference attendees: "Why do we simulate designs?" Dan Beeker of NXP Semiconductors explains how engineers can avoid using simulation entirely by managing EM fields correctly and focusing on the spaces—not the traces. And John Coonrod of Rogers Corporation discusses how he uses different simulation tools for different tasks, and he compares and contrasts 2D and 3D field solvers.

Do you have a great story about simulation—successful or otherwise—that you'd like to share? Shoot us an email at editorial@iconnect007.com. We're always looking for good content.

See you next month! **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 20 years. He can be reached by clicking here.



Barry Olney's High-Speed Simulation Primer

Feature Interview by the I-Connect007 Editorial Team

The I-Connect007 editorial team recently spoke with Barry Olney of iCD about simulation. Barry, a columnist for *Design007 Magazine,* explains why simulation tools can have such a steep learning curve, and why many design engineers are still not using simulation on complex high-speed designs.

Barry also highlights common mistakes that design engineers make using simulation tools, and he offers a variety of tips and techniques for anyone dealing with simulation challenges. Among them: Don't trust reference designs and datasheets.

Andy Shaughnessy: What are some of the biggest problems in simulation? In our surveys, engineers say that they have trouble doing simulation and analysis. What is so tough about it?

Barry Olney: I think the biggest problem, Andy, is time, and that's the same with PCB design in general. The PCB design is the last process in the design flow, and when I get a job for a board layout, it's already behind schedule. I've never ever had a job where it was on schedule and everything was running smoothly. So, you're pushed for time during the whole process, and to add simulation on top of that, that pushes it back another week or so. Management is reluctant to do it because they think, "Well, it may work and then we can get it through just a little bit behind schedule, but if we leave it another week then it delays things even further." It seems they don't have time to do it right the first time, but they've got the time for a re-spin.

A lot of engineering managers actually schedule in a re-spin because they believe they need at least two iterations before they get a working product. So, time is the biggest factor. That's why they generally tend to skip simulation. There's also the learning curve associated with the high-end tools that requires experience—not just with the tools, but with high-speed design rules. Sourcing IBIS models is another big issue. Maybe you can't find the model, so you have to compromise. IC vendors are now supplying most IBIS models, but for FPGAs,

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in particular, if you get the default IBIS model from the vendor's website, it has a default pin assignment, but once the EE places and routes the actual FPGA chip, you need to redefine the pin assignments for each signal.

Now, the pin assignment of the FPGA that someone designs isn't the same as the one on the IBIS model, and that's where it all goes haywire. You think, "That simulation is simple. You just have to import the IBIS models into the transmission line model and click Go." That should happen, but, it doesn't. Where you don't have pin assignments matching, you have to manually select the required FPGA sub-models from the thousands of pins with 50 or so sub-models. And these have all got cryptic names that are different for each IC vendor. So, you actually have to find the model or driver model that matches the transmission line that you're trying to simulate. Or maybe you cannot find the model at all. Good luck sourcing a connector model. So, again, this all takes time. It took me years to figure out how to do it properly, quickly, and efficiently.

The other thing is the cost of ownership, of course. The high-end simulation tools are expensive, as you know, and are beyond the budget of the average punter. So, it's better to outsource simulation. From a cost point of view, it's not all that expensive. Alternatively, EDA vendors have professional packages that include basic simulation tools. OrCAD has Signal Explorer, that I am now using; PADS has BoardSim EXT, a cut-down version of HyperLynx; and Zuken has tools like Lightning in their CR-5000. These are all entry level simulation tools, but they still require a lot of background knowledge to get them up and running. They are not that simple to use.

Shaughnessy: Do you basically have to be an SI or PI engineer to use simulation tools? Are there any simpler tools that fall under the simulation umbrella that, say, a PCB designer could use?

Barry Olney

Olney: Simulation tools encompass many subtools. For instance, stackup planning and PDN planning is all part of simulation and that can certainly be done by the average PCB designer. The stackup needs to be assigned before you even start placing a chip on the board. You need to define the differential pairs and accommodate different technologies on the same layers of the PCB. You may have a 50-ohm digital signal with 100-ohm differential pair. You may have a DDR3, which has 40-ohm single ended and 80-ohm differential impedance. You may have a USB that's 90 ohms. All these have to work on one substrate, so you need to account for all these different technologies and work out the impedance for all those before you even start your design. PCB designers can certainly do that. It's not difficult. It's pretty straightforward.

PDN planning can also be done by the PCB designer. The optimization of the PDN is a trial-and-error process that needs to be done in conjunction with the stackup materials, planar capacitance, and decoupling, to fully

exploit all avenues. The idea is to lower the AC impedance of the planes.

Shaughnessy: Barry, what's the cutoff? How should a company know when it's time to either invest in a simulation tool or just start farming out simulation? Do they look at it by the speed or the rise and fall rates, edge rates, or if it's serial links? Who would you recommend?

Olney: When it's too close for comfort, basically it's time to do signal integrity analysis. There's two ways of looking at it. There's the old, lumped-element method working in the time domain. That's static timing or the relationship between clock, data, address, and command signals. But what you must appreciate is that that static timing rides on an electromagnetic carrier weight. You have your static timing, which is critical, that rides on this wave of electromagnetic energy through the transmission line. We are used to visualizing the static waveforms on the oscilloscope in the time domain, but we also need to think in the frequency domain. It's a different world working in the frequency domain compared to the time domain. The frequency domain is particularly suited to analyzing the PDN.

This electromagnetic field that transports the static signals can also vary depending on whether it's running on a microstrip or a stripline configuration. If it's on the outer microstrip layer, because there's a mixture of solder mask and air in the dielectric, it tends to speed up the signal. It reduces the dielectric constant because the velocity of propagation is the speed of light divided by the square root of the dielectric constant. If you have a lower dielectric constant, then you have a faster speed. So, you must take into account the actual static timing of the devices, their relationship between the clock and the data and address, plus the timing of the propagating signal through the transmission lines.

Shaughnessy: When you have customers come to you, what are some of the typical jobs where they should have done a simulation and they didn't?

Olney: Generally, memory analysis. DDR is new territory to a lot of designers. They want to feel confident in what they've done and make sure they haven't made a mistake. That's one reason why people get simulation done, and the other, of course, is they have a board that doesn't work, they've been trying to fix it and they need help. That's when they're desperate, and it shouldn't come to that; that's plan B. Simulation should be done up front, as I've mentioned before, you need to do it before you even start placing a chip on the board.

Happy Holden: Are there situations where the board might work but you fail FCC? What other external things can you fail even though you connected the point, and it seems that the board works?

Olney: Yes, that happens a lot with reference designs. A reference design is done by smart engineers who design chips, and they know how to do a basic PCB layout, but in general they're not highly experienced PCB designers, so they don't know a lot about design for manufacturability. These new reference designs work great in the lab with a few wires hanging off here and there. Great, we've got it working. They make the reference design available, and everyone copies it thinking it's a golden board. But if you were to temperature cycle the board for the equivalent of 10 years, there are reliability issues. So that's generally what happens—intermittent problems in the field.

Shaughnessy: Do you find datasheets to be helpful?

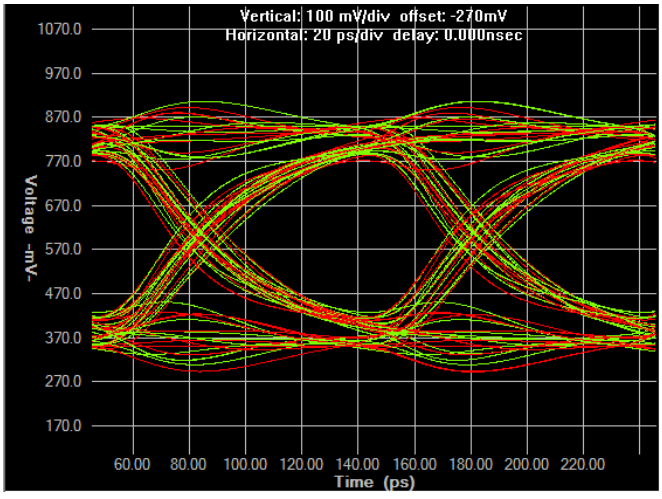
Olney: I always say to assume the datasheets are wrong, especially libraries of physical components because you look at a mechanical draw-

ing and there's always one number on there that just doesn't fit, and you've got to work it all out. You can generally go back to the actual physical component and measure it. There's always something wrong with the datasheet.

Shaughnessy: I remember the big three EDA companies were talking about having simulation tools that would run concurrent with the design, like they would be running during schematic and all through. Is that how it is now or is it something that is right at the very end?

Olney: Ideally you need to do that, yes. You need to simulate the schematic, which you can do. You can create freeform schematic models and then add an estimate of the lengths of the transmission lines. For example, for memory you may say, "I have two and a half inches here. So, I'll put a two-and-a-half-inch, 50Ω, transmission line, attach an IBIS model at either end and see how it goes." That's really good for building up the maximum length you have to play with because before you do the placement you need to know the maximum timing you can have on a chip. If you place the chips too close together it's difficult to route, and if they are too far apart then it may mess up your transmission lines with long delays and too many reflections.

So ideally you need to work out the placement before you put the chip on the board, and that also helps with your routing topology. You may want to do flyby topology—that's how you generally do DDR3 and DDR4—but there's no need to do a flyby if you've only got a couple of memory chips. You can still do a T-topology route, which means branching out with equal delay into each chip. All the professional EDA tools now have a way of extracting the topology, so once you have routed a particular section you can extract the topology of that from the PCB, so you get the physical transmission line. That includes whether it's running on microstrip or asymmetric stripline, for example. It builds the actual physical structure of the PCB, including layer transitions (vias), into



Much of high-speed simulation is centered on achieving a nice eye diagram.

the simulation model. Then you can virtually simulate the board itself, so that's the final process—making sure all the timing is right on the physical simulation.

Holden: Does anybody publish or sell a good dielectric material library?

Olney: I do (laughs). Actually, our stackup planner has 35,330 individual materials at different frequencies. There is a choice of over 700 series of rigid and flexible dielectric materials from over 60 manufacturers. There is every material you would ever need. If you can't find a new material, I'll add it free of charge. It's very comprehensive.

Shaughnessy: What good sources of information on simulation analysis are out there? If someone is new to the industry, what would you recommend to them as far as getting some more information?

Olney: Well, I think reading your magazine, Andy, is a good start, and other industry magazines. The SI Forum is a really good source of information with many experts on there that can answer your questions, as is attending any of the technical seminars that Rick Hartley and people like him run. They are a good start. I

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started off attending conferences and technical sessions. Happy's "Design for Manufacturability" was probably one of my first back in 1990. You can learn about the engineering process, but design for manufacturability is very important, and it's not taught in universities. There are a few courses on signal integrity that are targeted at EEs but not so much PCB designers. I developed the "Advanced Design for SMT" course for the Australian Electronics Development Centre back in 1994 to teach high-speed design techniques.

Holden: I guess we should qualify that a lot of what we're talking about in terms of problems apply to analog and digital designers, but if people are involved in RF design and doing it correctly then they have learned a lot of these things early on. It's just that the percentage who are really good RF designers is so small.

Olney: RF and microwave design is a different world altogether; the circuits are very high frequency with fast rise time and short wavelengths, so you need to be very careful. Every stub is an antenna. That's why coplanar waveguides are typically used for RF, because they tend to stabilize the signal. For a microstrip signal, for instance, you've got coplanar waveguides with ground pours on either side of the signal which tends to dampen the radiation.

Shaughnessy: A lot of designers and engineers agree that simulation is a great idea, but many of them don't use it. Why don't more people use simulation?

Olney: I'm sure it's mainly to conserve time. Managers always strive to reduce their design cycle. But simulation isn't that expensive or time consuming if you outsource it. For instance, I can analyze an average complex board for about US$5,000 and find the problem. If I were a manager and I had a choice of a small investment in analysis or taking the risk of a re-spin, I know which I'd choose. It's a no-brainer as it verifies that the product will perform reliably!

Dan Feinberg: One of the things that you just raised and Happy just mentioned is that people often look at price, but it's really cost, and they're different.

Olney: Absolutely. The cost of a re-spin is a lot more than the price of the tools or outsourcing analysis. It's not just engineering time you are wasting, but time to market and lost opportunity which can be extremely costly.

Shaughnessy: Lee Ritchey says a lot of these conflicts stem from a managerial viewpoint versus the engineering viewpoint. The manager thinks, "Great, the design was done quickly," even though there may be a costly re-spin down the road, because for now, the EE can get on to another project.

Olney: That's right, you'll always have conflict. Engineering and management require different skill sets. The manager is responsible for getting the project completed on schedule and to budget. And, he has to look good to his boss. If he schedules a re-spin, then it is expected. It's in the timeline. Whereas the engineer or PCB designer is more interested in the completion of their work and learning new techniques to improve their skills.

Holden: Is PCB design growing in Australia?

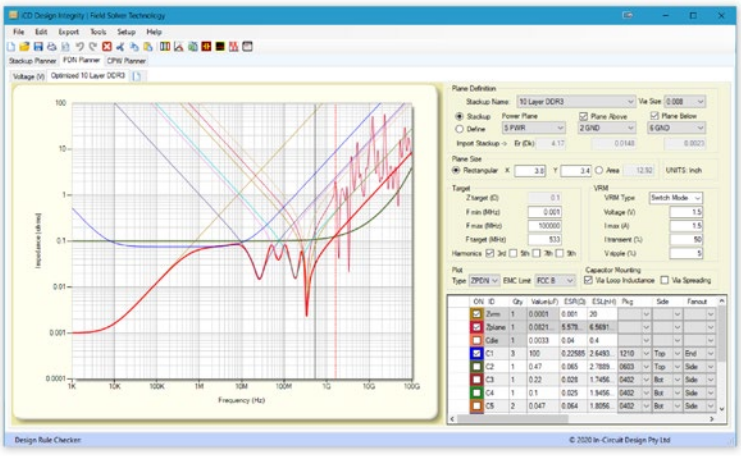
Olney: I guess I am a little out of touch with the Australian electronics industry as I mainly do business overseas now. We have small groups of designers, but there is not a large electronics industry except for defense contractors. It was always difficult to sell VeriBest PCB and Mentor (Siemens) tools in Australia because it's the home of Altium, of course. Everyone uses Altium and going against tradition is very difficult. I guess you could say that the Altium Designer's market is growing. There isn't much

of a market for simulation tools either. In fact, in the past, anyone who did well ended up going to the U.S., so you lose a lot of talent when a company becomes successful; it just disappears offshore.

Holden: Where do your customers come from?

Olney: Lately, the U.S. Probably 70% of my customer base is in the U.S., 25% in Europe, and 5% from other countries.

Shaughnessy: Do you have any recommendations for somebody dealing with simulation challenges right now? Any tips?



An In-Circuit Design field solver simulates a DDR3 stackup.

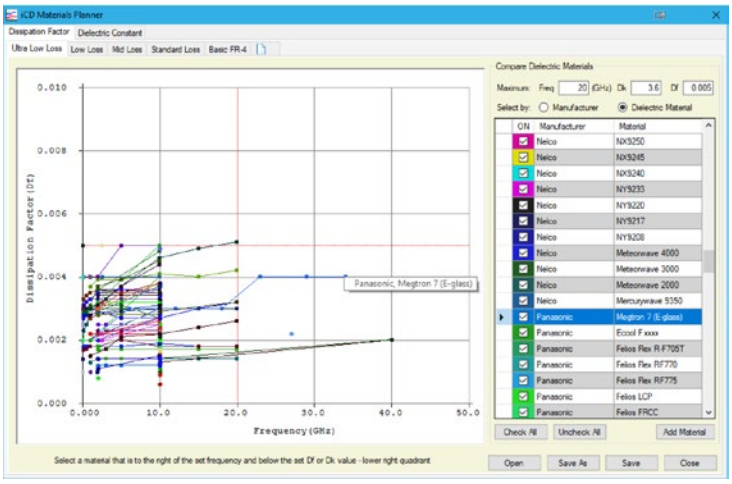
Olney: Sure. The biggest thing is forgetting what you learned at university. Circuit theory is all DC, but when you get into the frequency domain, with high frequency, fast rise time signals, and a distributed system, you need to think in the way of the electromagnetic fields, coupling, and radiation. It's a different world altogether. You really need to educate yourself before you can become a good high-speed designer. The other point I'd like to make is that simulation tools don't complete the analysis toolset. My eyeball is just as good as any signal integrity tool. That's because I have (embedded in my skull) 30 or 40 years of IPC design rules, design for manufacturability, and SI and PI requirements, so I can see a lot of issues before I really need to simulate. Just looking at the topology of the routing, for instance, gives me an idea of whether a design will perform to expectations. On the other hand, simulation gives you another set of eyes and allows you to visualize other issues.

When I do an analysis, I think outside the square. I drill down through the board; I do a teardown of the substrate. First, I look at the impedance and different technologies that must run on each layer, the materials used, and at the minimum cost, of course. It must provide adequate performance, but it doesn't have to be the best material, and it also has to be stocked by your fab shop. So, you must choose the right material for the right job.

These days, one of the largest problems is the amount of power supplies you have on a board. I think the last design I did had 35 power supplies.

Some believe, "Routing is simple. You just route between two planes and keep the critical signals isolated, etc." But until you get in amongst it (as a PCB designer, which I am) you come across the real problems of space. You just don't have the space to put in everything, while working out where these 35 copper pours go, and not interfering with anything else is a major problem in board layout. If you have a trace that crosses from one power plane to another, you are creating return path discontinuities and it can cause untold problems with EMI.

So, you really need to plan how you're going to place these power supplies to get the most effective route. If you can't route a board it may not be because you don't have enough layers. People often say to me, "How do you know when you've got enough layers? Is eight layers enough, or do I need 12 layers?" After a while you get a feel for it. But a good way to test it is just to let your autorouter go loose, and if you don't get 85% completion, then you've got something wrong. If the board is difficult to route, then it may be because of placement. You need to open channels for the router.



A materials planner tool allows the user to compare Df and Dk of various materials.

One of the things I talked about was time. A lot of people start designs when they are not ready for layout. They say, "We started the design, and we'll give you the main processor, the memory, and the power supplies," for instance. You start with these, move things around, and change them from one side of board to the other. Spin them and rotate them and whatever to get the best placement to prevent the rat's nest from crossing over, then route that section. Eventually the EE finishes the schematic, and you add all the other chips. "But the processor would have been better on the other side of the board." Turn it the other way around and all the signals would not be going through the center of the board from one side to the other. So, my recommendation is to never start a board until the schematic has been finished, approved, and it's ready to go.

The other thing I do when I'm analyzing a design is to look at the PDN, which is very important from a stability point of view. The key points for stability in the design are stackup impedance and the AC impedance in the PDN. Adding planar capacitance by using very closely coupled power/ground planes pairs, positioned close, in the stack, to the top and bottom ICs, has a dramatic effect on reducing the AC impedance. This is where the stackup configuration needs to be adjusted in conjunction with the PDN plot.

Minimizing the reflections on high-speed signals is another thing. You may have a driver, and typically the source impedance of the driver is between about 10–30 ohms. But, you need to have a transmission line of say 50–60 ohms. Now, that won't match to a driver of 10–30 ohms. In high-speed design you need to have either a series terminator or a parallel terminator at the end of a long line. Parallel terminations simple match the transmission line impedance of 50Ω. But a series termination must be calculated. The iCD Termination Planner, for instance, extracts the attributes required to determine the source impedance of the driver from an IBIS models IV curves. Then the series termination resistance is calculated, based on a distributed system and load, to match the transmission line for the selected layer in the stackup. In a typical digital design, you've only got the rise time to worry about, but with DDR you've got the data being clocked from both the rising and falling edges of the signal. So, you need to also look at the falling edge of the waveform, and that's quite a lot faster than the rising time of the device. This is due to the design of typical CMOS output drivers. For the same feature size transistor, an n transistor can turn on faster than a p transistor. So, the fall time is always faster than the rise time—which you need to consider.

Simple things like that will get your reflections under control. Now, reflections create a lot of crosstalk because if you have close coupling on the signals, which you normally do with tightly routed boards, you don't have a lot of room. You've got to route things close, and so you get coupling and crosstalk, which creates radiation. EMI is created from all these reflections. It's stabilizing the impedance and the power supply that stops these reflections and radiation allowing the product to pass EMC tests. All critical signals should be simulated. I don't actually simulate every signal within a bus. If you've got a huge bus with 128 bits, you're not going to simulate each one, but one

from each byte lane is enough because they're all routed much the same. Pick the worst-case signals to simulate then the rest will be fine.

When you're routing the data group of signals, it should all be done on the one layer of the substrate. A lot of reference designs that I have seen have address lines and data lines routed on the outer microstrip layer and some on the inner stripline layers. As I mentioned before, that all impacts timing, because of the different velocity of propagation of the outer and inner layers. If you run the entire bus on one layer, then you're matching the timing automatically, so that saves a lot of simulation time and risk.

Crosstalk is very difficult to predict. When I do a teardown of the board, I look at every layer with respect to every other layer. I'll have a look at layer one, which may be a signal layer with respect to the layer two, which may be a ground, and look for any signals outside that ground plane, because once the signal leaves the plane area that increases its impedance, and it will radiate and cause problems.

When you get to stripline, you may have dual asymmetric stripline, and you will have two traces between the planes. You need to look at the planes with reference to each signal layer and see where the return paths will flow. We tend to route signals from one point to another from a driver to a receiver, but what you must understand is the return current will flow with high frequency directly underneath that signal trace, and if there's a split in the plane, or it has to change layers in some way, then you need to facilitate that.

If you have two ground reference planes, for instance, you can place a ground stitching via where the layer transition is. However, if the reference plane changes from ground to power, traditionally we use one decap across the planes to provide a return path for the current. If you have two different power supplies—for instance, a 5V and a 3V—and you have traces going across the split, you should put in a decoupling capacitor going from the 5V to ground and then from the 3V to ground. This stops the noise coupling between the two different power supplies that are going through ground rather than just from supply to supply.

There are a lot of things to look at about overlapping your signals. Broadside coupling is very, very difficult to spot because when we are routing we generally turn off the other layers or just dim them in the background. We are just looking at the one layer we are routing and pushing things around, and we don't understand or see what's on the other signal layer near it. In the stripline situation where you have broadside coupling, you have the width of the trace coupling to the width of the trace below, which is a lot more coupling area than you would have with an edge coupling because you only have the very thin edge of the trace with edge coupling. With broadside coupling, you have a wide trace coupling to another wide trace, and generally you've got a very thin dielectric—like a 3-mil—in between. That makes a beautiful coupling, maybe a good RF coupling, but it's not what you want to do in digital design. Also, be careful of broadside coupling on built-up microstrip layers.

Shaughnessy: It sounds like a lot of this comes down to following solid design and engineering practices, but also having the experience to know what to look for. You can't be a part-timer with simulation tools, I guess.

Olney: It's all about experience. Experience is the greatest teacher of all! That's why I say you can't just put a tool in front of an EE who's just out of college. They don't know what to do—it doesn't make sense to them. They don't understand the principles or concepts, and someone needs to give them direction in how to analyze high-speed designs quickly and efficiently.

Shaughnessy: This has been really great. Thanks for speaking with us.

Olney: Thank you. DESIGN007

Bridging the Simulation Tool Divide

Feature Interview by the I-Connect007 Editorial Team

Todd Westerhoff of Siemens EDA recently spoke with the I-Connect007 Editorial Team about the divide between users of high-powered enterprise simulation tools and those who need a more practical tool for everyday use, and how Siemens is working to bridge the gap. Todd also shared his views on why so many engineers do not use simulation, as well as advice for engineers just getting started with simulation tools.

Andy Shaughnessy: Hi, Todd. This is our simulation issue, and we want to get your thoughts on some of the challenges in this area. What do you see right now? What's the biggest problem in simulation?

Todd Westerhoff: I think the biggest challenge is that there just aren't enough people simulating. There are a lot of people who are designing to rules of thumb, manufacturer guidelines, or getting somebody else to run analysis for them—but there aren't that many simulating themselves. I usually break simulation users into two broad groups: SI experts, who run simulations full time; and everyone else, who run simulations intermittently, if at all. The SI experts have the most advanced requirements and are also the smaller of the two groups.

The general assumption about simulation seems to be that it starts at the top—if we meet the analysis needs of the experts, knowledge and technology will trickle down over time to the broader audience. The problem is that, as an industry, we have too many designs in progress with too few experts to support all that activity. Simulation has two main purposes:

1. Providing a basis for making informed decisions about design trade-offs.
2. Validating a design before manufacture to reduce the risk of prototype spins.

How do we expect the majority of system designers to make decisions and reduce risk if they don't have data to back up those decisions?

Most of the simulation that we need to make design decisions and detect issues during layout doesn't require expert-level attention to

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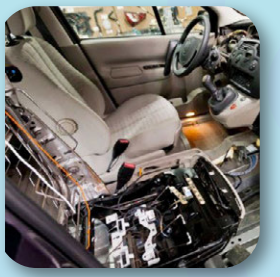

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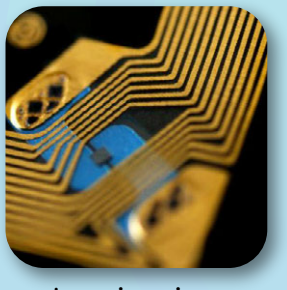

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detail—the need is far more pedestrian. We're not servicing those needs when we focus primarily on the state of the art. SI tools have been around for 30 years now, and we still see the majority of people not simulating, so we need to consider doing something else.

Shaughnessy: Maybe they don't need a tool that you have to be an experienced signal integrity engineer to operate. Can a regular system designer or layout designer use the simulation tools we have today?

Todd Westerhoff

Westerhoff: Depending on the tools you talk about, yes and no. Let's go back to our classes of users. Experts are looking for advanced tools with state-of-the-art performance and capacity. Ease of use is a consideration but not critical, as experts can make pretty much anything work. They have deep SI knowledge and can improvise analytical methods when the situation calls for it. To your question, the tools used by full-time SI/PI engineers are typically not usable by mainstream designers, because the tools by themselves are not enough. You need an analytical methodology, or workflow, to apply the tools to a design and determine whether the design will work, and that process is typically complicated enough (and manual enough) to preclude use by someone who isn't performing analysis full-time.

And that's the rub: if we're not designing a 112-gigabit serial link or a loaded DDR5 interface, most of the issues we face during design and layout don't require the kind of accuracy that an expert is looking for. There are a lot of design issues you want to take off the table before you put a lot of effort into modeling and simulation. You can think of it this way: Experts typically simulate at the level of accuracy needed to "sign-off" a design for fabrication, but system designers are often just trying to assess the impact of a tradeoff on design margin. In those cases, a good answer now is preferable to a great answer later. You can think of that as "trade-off" analysis. It's less accurate, but faster to run and accessible to a wider audience. That's the kind of analysis that needs to be accessible to regular system or layout designers. We have some of those tools in place today, but the world clearly needs more.

Shaughnessy: Everyone agrees that it's rough going at first, trying to understand simulation without decades of experience. Where would a young EE start?

Westerhoff: Signal integrity is one of those fields where there seems to be a lot of tribal knowledge and a relative scarcity of basic training material for new users. DesignCon papers are great for advancing the state of the art, but they are often over the heads of people who don't do SI for a living (this stuff is complicated, after all).

What's the new engineer supposed to do? We seem to have basic material that's easy to understand but doesn't really help you make design decisions, and advanced material that gives you a mathematical formulation for how the physics work, but not enough in-between. There are people who can look at Maxwell's equations and understand how EM waves propagate, but I'm not one of them. It took me a long time to understand why RF structures are characterized the way they are, and how that applies to time-domain circuit analysis. I don't see enough material that explains physical phenomena at a practical, intuitive level and links to the types of design decisions that engineers need to make.

Let's take a step back: What's the most important question when I'm designing something?

Nolan Johnson: Does it work?

Westerhoff: Bingo! The details get complicated but the question is simple: Will our design work, and by how much? How much margin do I have available to make design trade-offs that reduce manufacturing cost, or whatever?

Johnson: Are you talking about something like digital simulation? Is the logic of my schematic going to behave the way I expect it to? Are you looking at the behavior of your schematic at a logical level?

Westerhoff: Great question, but I'm talking about something different. Logic simulation is about making sure my design creates the right logical 1's and 0's, that it has the correct logical function. That's a binary problem: it either works correctly or it doesn't. Signal integrity is about the analog behavior of digital signals—whether they achieve the right voltages at the right times to ensure that signals are received (sampled) correctly. That means we can have margin—the degree by which a signal's voltage exceeds a minimum voltage and timing needed for reliable operation. We want to have enough margin to be reliable but not so much that the design becomes cost-ineffective, since increasing margin tends to increase the cost of producing the design.

Often people will say, "Just take the vendor's reference design and copy it." That works, but with drawbacks, because reference designs tend to be conservative, for good reasons. One, they're the first board built for that particular IC, so nobody knows where they can cut the corners yet. Two, the IC vendor absolutely wants to prove the chip is reliable and they're not trying to manufacture the reference design in volume. So, what's cost-effective for a reference design may not be cost-effective for volume production. Three, what happens when a mistake gets made while copying the reference design? Signal integrity issues can be notoriously difficult to debug in the lab—simply probing a marginal signal can be enough to change its behavior. What happens if you have a low-cost, high-volume consumer design that's failing intermittently in the lab?

Signal integrity issues can be notoriously difficult to debug in the lab—simply probing a marginal signal can be enough to change its behavior.

Shaughnessy: How do you convince people to use simulation in the first place? At DesignCon, a moderator will ask who uses simulation, and three hands might go up. Is it that due to time to market?

Westerhoff: Let's start with why people simulate. I'll give you my list of five reasons why people get started with simulation.

1. There's no other path forward. When I'm designing a new chip with a new package, there are no pre-existing guidelines or rules. It might be a standardized interface, but the IC layout is new, and the package is new, so I know full well that everything won't just come together by itself. I'm going to have to model everything and prove that it works before anything gets built. That's how we designed ASICs in my past; we proved we had a working board-level solution before the chip is taped out.

2. People start simulating because they're having lab failures that affect project schedules and costs. I'm not talking about inconvenience; I'm talking about real impacts. One

company we talked to was making small boards for consumer applications, but spending over $150,000 a year on prototypes due to problems that were readily detectable with simulation. There was a clear argument for saving money, even with a tool purchase and the ramp-up cost of training a new user.

3. Costs and delays associated with outsourced analysis pile up to a breaking point. If I use someone else to do my SI analysis, that takes time and money—even if the SI consultant is internal. If I outsource enough work, it becomes a problem. It doesn't have to be about cost; if lots of people rely on the same SI consultant, they're all dependent on what other jobs the consultant has already committed to. Time is money.

4. Reference designs and rules of thumb run out of gas, and/or overdesigning drives up manufacturing costs to a breaking point. Commodity consumer products will be especially sensitive to something like this.

5. Organizations are proactively seeking to improve their design processes.

Shaughnessy: Wait a minute. You're saying that process improvement ranks last in terms of reasons why people start simulating?

Westerhoff: I am because I'm being practical. Companies don't make big investments to solve problems that aren't costing them a lot of money. They always have other things to worry about.

Simulation is a lot like having good habits: we all agree we should. We all agree that we should floss, eat more vegetables, and exercise more. The question is, how do you lower the barrier to helping someone get started and keeping the process going?

Here's a paradox: If most of what we talk about are the state-of-the-art problems in signal integrity, then we're making the barriers to entry greater, not lesser. We're experiencing an "expert crunch" already and focusing almost exclusively on technology makes it worse.

Johnson: The automotive press is similar: There's lot of coverage on the Corvette and it sells magazines, but when most readers go to the dealership, they buy a Toyota.

Westerhoff: So the question becomes, what does it take to make someone productive with SI and PI tools? I propose that there are three main components. The first is domain expertise. If you don't know what characteristic impedance is, I'm not going to show you what to do with a signal integrity tool, because you won't understand the problem to be solved. The second component is tool training, and that's actually the easy one. The third component goes back to our fundamental question: Will my design work? If I give you a simulation tool and you run a simulation, then what? How are you going to determine if the design passes or fails, and by how much? You need a complete analytical methodology for verifying your design's behavior against a spec to determine operating margin. That methodology will be protocol-specific, and sometimes component-specific.

So the question becomes, what does it take to make someone productive with SI and PI tools?

So you need knowledge, you need tools, and you need an analytical methodology that maps to your interface's specific requirements. People who run SI simulations for a living will put the pieces together themselves, but system designers and layout designers need solutions that work right out of the box. That's what we're trying to do.

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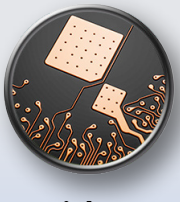

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Shaughnessy: What advice would you offer to someone just getting into simulation who already knows how to design a board?

Westerhoff: Personally, I try to listen to everything that Eric Bogatin and Scott McMorrow say, for different reasons. Eric is a phenomenal educator, and he has a gift for breaking complex topics down and communicating them. Every time I listen to Eric, even on a topic I think I know well, I learn something new. Scott has been state of the art for the 20 years I've known him and shows no signs of slowing down. Every time I talk to Scott, I learn what issues are coming at me in the future, whether it will be six months or two years from now.

It's important that users take the time to understand what they're doing and why. It's not just about tools and features; a simulator is just a tool—it won't make design decisions for you any more than a hammer will build a house for you. You need to understand how to use a simulator to identify and debug design problems, or you're going to get stuck.

You need to understand how to use a simulator to identify and debug design problems, or you're going to get stuck.

If you're just getting started, don't "shoot for the moon" in terms of accuracy. Accuracy isn't just about having the right tools—it's about having the expertise, computer resources, and time to use them. Your goal isn't to find 100% of your design issues, it's to take most of the issues off the table so that you can leverage dedicated SI expertise more effectively.

Shaughnessy: That's good.

Westerhoff: There are two ways you can waste money. The first way is overdesign—you waste money in manufacturing. You keep wasting money for as long as the design is in production. The second way to waste money is analytical overkill—you waste money in engineering. If you're running a more detailed analysis than is needed to establish that the design will work, you're wasting time, and time is money.

Shaughnessy: Do you think we'll see more simulation and analysis tools designed for new users?

Westerhoff: I hope so, but I think what we really need is a better bridge between the experts and intermittent users. Chances are, both groups are going to run analysis on the same designs. If the experts can develop useful "best practice" design guidelines for the organization, then the system designers and layout designers can use automated rule checking to ensure the issues are off the table before detailed modeling and simulation begins. I shouldn't have to build a 3M EM model of a board and run analysis just to find out that I have components without decoupling capacitors nearby.

Similarly, any analysis performed by system designers and layout designers should be able to feed directly into the tools the SI experts use. Simulation is a GIGO (garbage in, garbage out) process, and there's lot of work involved to make sure component types and values are tagged properly. The system designers and layout designers are often closer to a particular design than the experts are, they're in a better position to verify that data is correct, and that helps make better use of limited SI expertise.

There's a natural cycle that occurs with SI technology—the issues that are state of the art today become commonplace over time. That means that over time, you can and should be able to take analytical processes that were originally limited to experts, refine and automate them, and then make them accessible to a wider audience. The question then becomes,

what analytical tasks can you make available to what audience? The SI expert crunch isn't going away, so we're going to have to make system designers and layout designers more self-sufficient and find better ways to couple their efforts to the SI experts in their organization.

Johnson: This takes us back to the very beginning of the conversation: To put together a comprehensive solution in the current environment, you have to be a simulation expert. That's a huge barrier and another area where engineers will think they have to be an expert in an area that's not their discipline or job.

Westerhoff: Absolutely. Most of the time, SI experts are using a collection of tools from different companies to perform a given analysis task. The analysis methodology—what tools get run in what sequence, and how data gets formatted and passed between them—is custom. Parts of the process are usually manual, so you have to pay attention to the details, or the results will be compromised. All of that adds to what you just said: The average system designer will avoid taking on that task.

Since HyperLynx combines DRC/ERC, SI, PI, and 3D EM, we have all the modeling and simulation technology we need to create complete analytical methodologies that don't rely on anyone else's tools. We can define all the analytical steps and data formats, and automate as much of the process as possible, to provide a complete analytical methodology, right out of the box. It's not about having all the tools; it's about having work together with a documented flow. That frees the customer to focus on the thing they care about the most: will their design work, and by how much?

Shaughnessy: Are there any myths about simulation out there that you would like to address?

Westerhoff: I think some people believe that the only thing that matters with simulation is accuracy, and beyond that all simulators are equivalent. Accuracy is important, to be sure, but it's not the only thing. There are times when you want a rough answer quickly, times when you want a decent answer and can be a bit more patient, and times when you want the best answer possible and are willing to wait for it. You need a flexible, graduated ability to trade off speed for accuracy.

Saying that the only thing that matters for simulation is accuracy is sort of like saying that the only thing that matters for cars is performance, and that if you only had a great performance car, you'd never need anything else. I've seen people driving Lamborghinis, but I've never seen anyone take their Lamborghini to the lumberyard.

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Shaughnessy: When should an OEM start to consider using simulation or outsourcing to an expert?

Westerhoff: I'm going to refer you back to my five points, Andy. You consider it when there's no way forward, when you have failures, when your consultants get too expensive, when overdesign costs mount up, and finally, if you're forward-looking. If we're successful at making simulation easier to use, we'll see those reasons change with time.

Shaughnessy: This has been really good, Todd. Maybe we'll catch up in person, if the stars align.

Westerhoff: Always a pleasure, Andy. DESIGN007

Growth and Trends in the Thermal Management Market

Sensible Design

by Jade Bridges, ELECTROLUBE

The ongoing trend for product miniaturisation combined with more modern, higher-powered devices has ensured that reliable thermal management is an essential part of both modern and future electronics design. The LED lighting market is just one example of where thermal management is critical to the durability of the unit. Thermal management products are also offering solutions for greater efficiency in green energy development; photovoltaic inverters, which are known to be particularly sensitive to temperature; connections between the heat-pipe and water storage tank for solar-heating applications; hydrogen fuel cells; and wind power generators.

Is the thermal management market growing now? Yes, it certainly is, due to the ever-increasing number of electronic devices and applications entering the market. Demand has risen for higher performance and greater reliability in products with the added requirement of making electronics more discreet to fit into more challenging locations and environments. Let's explore some of the reasons why the market is growing.

Is product performance or product reliability deemed most important by manufacturers when producing their products for market?

Both! It depends on the product in most cases. For example, everyone will want their product to perform the best, but each product will have a different expected lifetime. For something with a small turnaround time, i.e., a device that is expected to be updated every one to two years, the performance of that prod-

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uct is most likely going to be the most important factor. It may be competing against many other similar devices on the market and therefore must be both reliable and high performing but with an emphasis towards the latter. For a safety-critical device, you absolutely need reliability. It may not be "all singing and dancing" but as long as it does the job it is intended to do without failure, it will be acceptable. There is usually a trade-off with the properties of any design but remember, by considering thermal management from the start, it should be possible to achieve highly in both areas.

It may not be "all singing and dancing" but as long as it does the job it is intended to do without failure, it will be acceptable.

Is there a drive for higher and higher levels of thermal conductivity?

Yes, you could say that there is a drive for increased levels of thermal conductivity. However, if you were to investigate each response in detail, thermal conductivity may not actually be the desirable factor engineers are looking for. In all applications, everyone is striving for improved performance and greater efficiency. Simply increasing the level of thermal conductivity alone may not offer you these improvements.

When specifying the thermal conductivity required, it should be based on the end application conditions and requirements. It should also consider the design of the unit/substrate and the application method of the thermal management compound. If the product is not applied correctly—for instance, if air voids are present—then the product cannot offer the full level of thermal dissipation it is capable of.

In general, when you increase the thermal conductivity you must adjust the amount or type of fillers used in the thermal management material and that could impact the viscosity of the product, which in turn affects the overall performance of the product in the end use application. This change may also impact other properties, such as electrical conductivity/insulation, the material's behaviour in changing temperature conditions, etc. Therefore, while most will say that with electronics becoming more powerful and being used in more challenging environments (and so higher thermal conductivities are needed), each application should be reviewed holistically to make sure that you achieve the best performance from the thermal management material, not just rely on the thermal conductivity value alone.

Heat generation rises in line with miniaturisation and the desire for higher performing components—what are the solutions?

Look at the design of the unit/PCB; are there any ways in which heat could be distributed more effectively? For example, if all heat-generating components are now in one area and close together, could they be relocated? This sounds simple to do but in practice it is not always possible. Other ways to effectively dissipate the heat away from certain areas is to ensure you have the best thermal interface material for your application. That means checking the thermal resistance at the interface, or more simply, checking the temperature of components or areas of the board. When you have this starting information, you can look at ways to improve heat dissipation by adjusting the thermal interface material used, for example. This could be moving to a product with higher thermal conductivity, however, make sure it can still be applied correctly to enable it to perform as expected.

As well as looking at the interface materials used, you could also look into the gaps around the board. Are there any areas where hot air

could gather whilst the unit is in operation? Does the outer case offer any heat dissipation, i.e., is it made of metal? If so, could you utilise a gap-filling product to help remove these localised pockets of air? There are many ways to reduce heat dissipation but again it is important to look at the unit/PCB as a whole, as an action taken in one area of the board may lead to issues elsewhere.

What new trends are expected in global thermal management?

Due to developments in the electronics industry, the introduction of smaller and smarter products is increasing. These advancements in the industry have led to an increased need for innovative thermal management technologies to improve system performance and reliability by eliminating the heat generated by devices. Trends driving growth in this market include the increasing popularity of smartphones and tablets, which have seen considerable growth in the past decade. Due to mounting sensitivity toward weight and price, the need for advanced thermal management solutions is increasing.

Artificial intelligence (AI) is growing rapidly for the next generation of smartphone, smart home device, and smart speaker categories. This is expected to drive the thermal management technologies market further.

Increasing awareness of environmental issues combined with potential performance advantages is propelling the adoption of electric vehicles and a more widely available charging infrastructure, both of which rely heavily on thermal management predominantly for increasing the reliability and performance of battery systems. Also, the increasing adoption of renewable energy resources is a major factor driving the thermal management market.

Due to escalating industrialization across the world, demand has risen for continuous power supplies, which has positively impacted the growth of the thermal management market to ensure maximum reliability. For instance, capacitors are used to temporarily store electricity where required, or in off-grid applications batteries may be required to store power for more widespread use. In such cases, these electronic devices will require protection from the elements but will also be required to operate at higher temperatures and offer some form of thermal dissipation, due to the heat emitted during operation. Depending on the design, thermal management products will be used to help dissipate heat away from devices to maintain efficient, continual power.

Depending on the design, thermal management products will be used to help dissipate heat away from devices to maintain efficient, continual power.

I hope the points covered this month have been helpful and please look for my next column, where I'll be covering more issues on thermal management to get the best heat protection for your circuitry requirements. In the meantime, please contact me if you have any questions. We also have numerous technical resources available for your interest, such as how-to videos on our youtube channel, and articles and blog stories on newly updated, application-focused website at www.electrolube.com. **DESIGN007**

Jade Bridges is global technical support manager at Electrolube. To read past columns from Electrolube, click here. Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments,* and watch the micro webinar series "Coatings Uncoated!"

Alternatives to Simulation

Feature Article by Dan Beeker
NXP SEMICONDUCTORS

We are living in an age where the demands on electronic product designs are constantly evolving. The IC technology and operating speeds continue to pose significant challenges for teams as they work to develop their products. The increased transistor switching speeds and less forgiving compliance standards make signal integrity and electro-magnetic compliance more difficult to achieve. The status quo seems to have become, "We expect to fail EMC testing."

What can be done to increase the likelihood of compliance, and proper function? In some cases, the engineering community looks to simulation as a method of evaluating the PCB design. There are certainly a number of powerful tools available, but they are usually expensive and difficult to use properly. These tools are only of value if the transmission lines are not broken. The simulated results often differ from the measured behaviors, forcing model tweaks and lost time. In most cases, you have an incomplete model and inaccurate measurements, which even when reconciled, do not reflect the real behaviors of the design. It is nearly impossible to get good measurements for this purpose. The probes will affect the signal, as does the location in the transmission line where the measurement is taken. Many teams just do not have the bandwidth or expertise to achieve success using this process.

The fundamental issue is that most simulation tools are not capable of evaluating broken transmission lines. (I say "most" because I am not intimately familiar with all of them.) A broken transmission line is a signal or power conductor that is not one dielectric away from ground. If a signal or power conductor is not directly adjacent to a continuous dielectric bounded by a continuous ground conductor, the EM fields do not stay where the design requires. The field will fill the space between

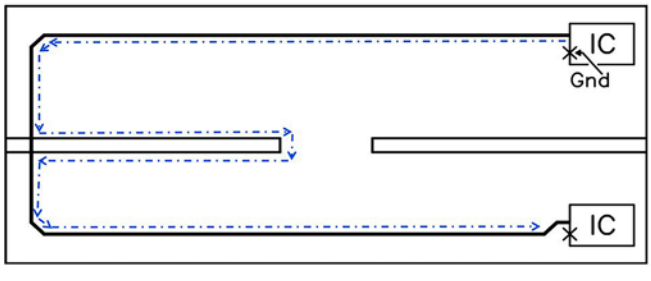

Figure 1: If the return plane is split, the field must fill the space between the signal trace and the ground copper. (Image courtesy of Rick Hartley, consultant)

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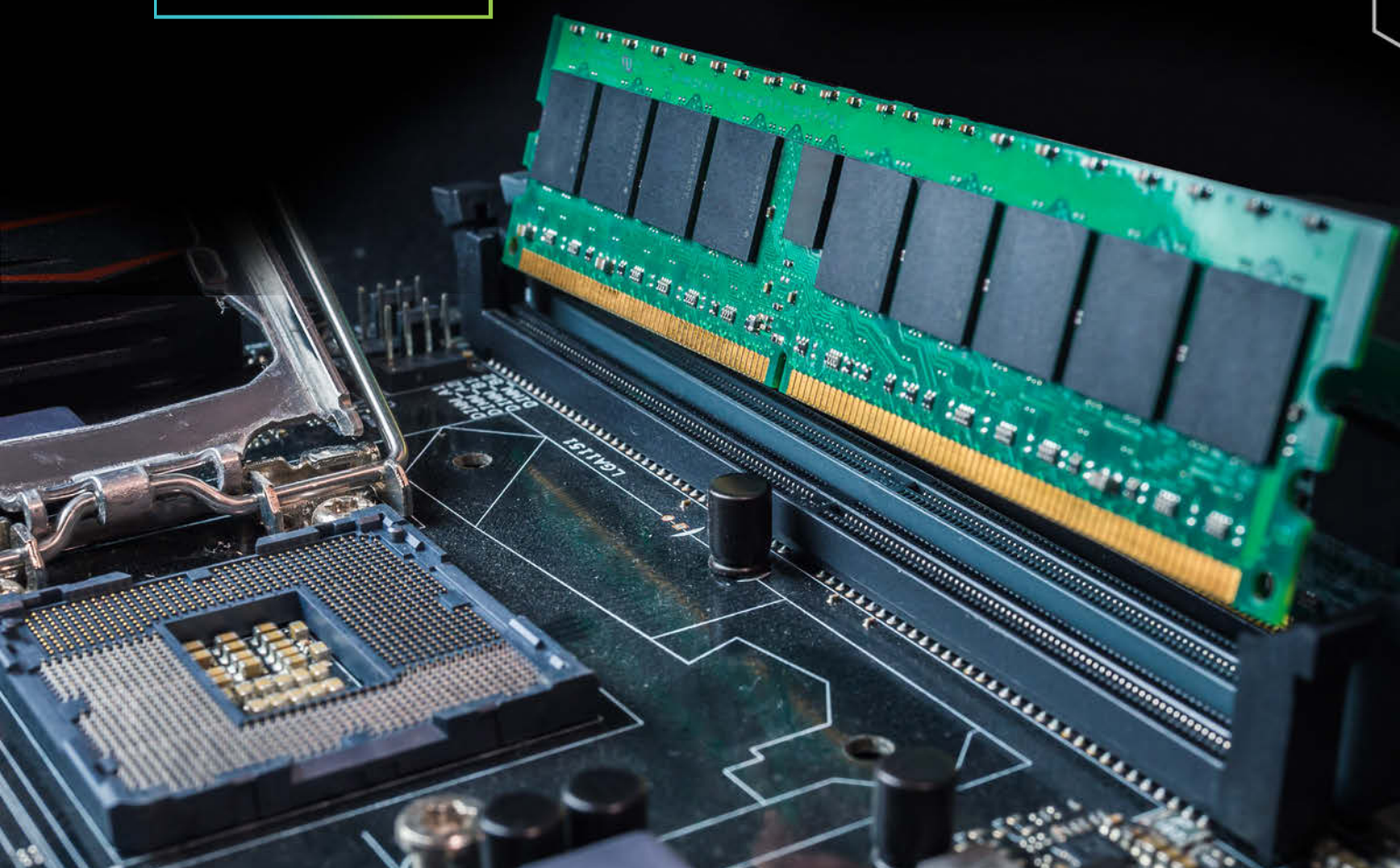

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the signal conductor and the ground conductor that connects to the power source for the PCB.

The more conductors and dielectrics that are between the signal in question and its ground, the more impact on signal integrity and EMC. There are just not enough nodes in the models. It would require characterizing every change in the transmission line geometry, for not only the signal trace in question, but the other nearby traces and the power supplies for the ICs involved. Once a trace crosses a split in the ground plane, the space involved in the signal transmission expands to include the divergent path of the continuous ground conductor. This increases the time it takes to establish the signal voltage, requiring more wave cycles to achieve the signal levels. Each wave cycle increases crosstalk and possible radiated emissions, which occur at every wavefront. Every other signal crossing the split will also have an expanded space to fill. These signals will then share the space and affect the voltage for each signal. If a power supply is not properly designed, signal integrity is compromised for all the signals using that supply. If a signal is compromised, it affects not only that signal, but other signals in the adjacent areas of the PCB.

Having a proper understanding of PC board design and how to totally contain EM fields will minimize or negate the need for simulation. We have to start with a different understanding of how electronic circuits function. Containing EM fields requires three things: two conductors separated by a space. If one of these components is missing, the EM field will behave in well-defined ways. If there is only one conductor, such as a sphere, with no hole in it, any field contained inside the sphere cannot escape. If there is only one conductor and a space, the field will not be contained. If there is no space between two different conductors, such as between power vias next to each other, then there is no field in that space.

Next, it is important to understand that you only get three components to use in managing the fields: conductors, spaces, and switches. ICs are just giant switch arrays. Finally, there are only three things you can do with EM fields: Store them, move them, or convert them into kinetic energy. This is not rocket science. Using this perspective is crucial in achieving signal integrity and EMC goals. It is all about the space.

Empirical analysis of the PCB design can be a good first step in achieving signal integrity and EMC compliance. The first thing you

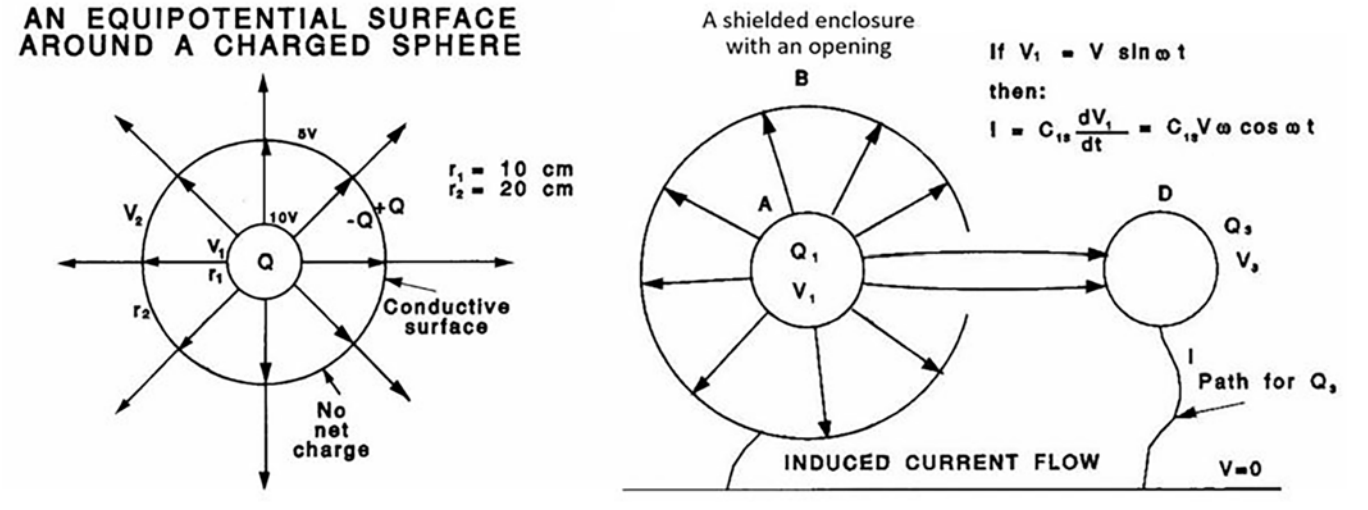

Figure 2: Remember: If you have one conductor, such as a sphere, with no hole in it (2a), any EM field contained inside the sphere cannot escape. If there is only one conductor and a space (2b), the field will not be contained. (Images courtesy of Ralph Morrison, consultant)

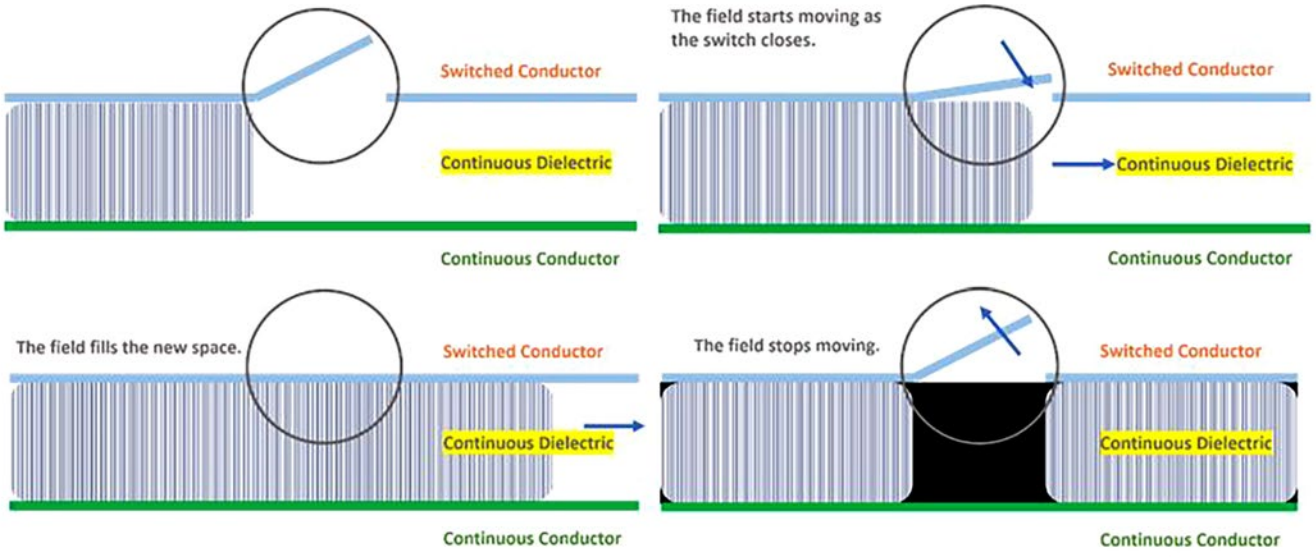

Figure 3: Images depicting the movement of an EM field as a switch closes. There are only three things that you can do with EM fields: Store them, move them, or convert them into kinetic energy.

need to understand is that the EM energy used in the circuit travels in the dielectric, not the conductors. The PCB conductors are used to create the boundaries for the spaces where the EM fields will go. Managing these spaces starts with the board stackup. If at all possible, there needs to be a solid ground plane between each pair of signal/power layers. These form a triplet (signal-ground-signal) or a paired dielectric, which allows routing between the two conductor layers to be done with only the signal via. The opening around the via in the ground plane provides the connection between the top and bottom dielectric layers. For example, in a four-layer PCB, if layer two is ground, then layers one and three form the boundaries for the paired dielectrics between them. In this case, layer four is not adjacent to the ground plane, and must be treated as if it were single layer board. Each signal trace needs to be routed next to a ground trace or ground flood area. When connecting layer

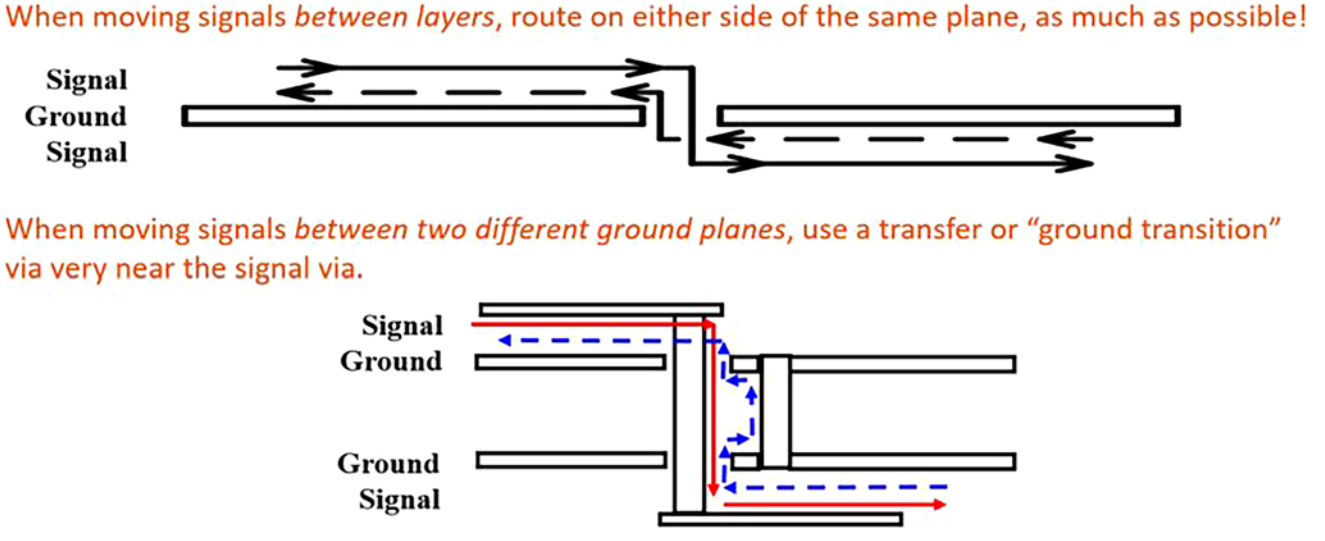

Figure 4: Moving EM signals often involves some clever routing and via placement, but it's not rocket science. (Images courtesy of Rick Hartley, consultant)

four to layer one or layer three, a ground transition via is required, to connect the dielectric between the traces on layer four in the Z-axis to the dielectrics in the triplet formed by layers one, two and three. This pattern must be repeated to create a solid foundation for EM field control.

A six-layer board stack is extremely powerful, providing two sets of paired dielectrics and four routing layers that form good transmission lines. Again, care must be taken when routing between these paired dielectrics, to connect the spaces in the Z-axis. The plumbing must be intact from the source of the energy to the load, in all three dimensions. Some signals can never be compromised. The crystal circuit and power supply are two very good examples of this. The one dielectric rule must always be enforced for these signals, with the traces routed over continuous ground copper on an adjacent layer or co-planar ground copper (a poor second choice).

Analysis of the PDN is the next step on the road to signal integrity and compliance. In the case of the power supply, not only is the one dielectric rule inviolate, but the capacity of the dielectric to carry EM fields must be adequate to supply the needed energy for the devices connected to it. This is not achieved by increased copper weight, but by having an impedance that matches the need. Thinner dielectrics, wider conductors, or multiple parallel transmission lines are required for good power distribution, as are properly sized and placed capacitors in the PDN. The capacity of the power supply transmission lines is critical.

If you need five amps, you need the dielectric that has the capacity to deliver this much energy. Current flow is a measure of the amount of EM field energy passing through the dielectric. Five amps is five coulombs of energy per second, much like the idea of water flow in a pipe, measured in gallons per minute. If you need five gallons of water per second, a one-gallon-per-minute pipe will not do the job. The same is true for the PDN. If you need five amps, you must provide the spaces that can carry that much energy. It is the dielectric that is the key here, not the conductors. Adding more copper weight does not increase the capacity of the dielectric. Again, only reducing the dielectric thickness, increasing the copper conductor surface area (trace width) or adding more parallel transmission lines, will increase the capacity of the PDN.

In conclusion, with proper EM field planning, you can often avoid having to simulate a PCB design. The first line of defense for achieving good signal integrity and compliance is to review the PCB design. Look for areas where the one dielectric rule was violated. Start with the board stack. Are there paired dielectrics? Are they connected to the other layers properly? Are there ground transition vias where needed? This is especially important in circuits such as SMPS designs, where the components are placed on both sides of the board. Properly connecting the top dielectric, adjacent to the top layer, to the bottom dielectric is critical. Each power via needs a ground transition via. Does the PDN provide adequate capacity and properly placed components? In many cases, parallel Z-axis transmission lines are needed to ensure there is enough capacity to allow the energy to move between components.

As Ralph Morrison always said, "Buildings have walls and halls. People travel in the halls, not the walls. Circuits have traces and spaces. Energy and signals travel in the spaces, not the traces." Design the spaces, by using the traces. To help you all remember this, enjoy "All About the Space," a remake of the Meghan Trainor song, featuring my daughter Breezy Beeker on vocals. **DESIGN007**

Dan Beeker is a senior principal engineer at NXP Semiconductor.

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Jan Pedersen: Getting Into Ultra-HDI With IPC Committees

Interview by Andy Shaughnessy
I-CONNECT007

I recently spoke with Elmatica's Jan Pedersen about winning the IPC Dieter Bergman Fellowship Award this year, as well as his work on a variety of IPC committees. Jan, a regular PCB007 columnist, explained how he and a group of committee members are now exploring ways to bring 1-mil traces into the mainstream, and the need to bring more traceability into automotive and medical PCB standards.

Andy Shaughnessy: Jan, congratulations on being awarded the IPC Dieter Bergman Fellowship Award.

Jan Pedersen: Thank you very much, Andy. That was a great surprise for me, and it's a big honor. I'm very honored to receive this. Mainly, this is instant recognition of the hard work that I've been doing for IPC. It is of course on behalf of Elmatica.

Shaughnessy: Well, you've done so much work with IPC regarding standards and design data. And designers and fabricators get a lot out of your *PCB007 Magazine* columns.

Pedersen: Yes, a lot of it is all about IPC standards, how you understand them, and how you use them. What is the standard for you as a user, a manufacturer, and a designer as well? I think that's very important. Basically, it's for everyone, not only for the big players. I think that's the good thing that surprised me: Elmatica is a small company of 40-ish people that is being recognized with this award. That's maybe the biggest thing with this award, actually.

Shaughnessy: And we all loved the video that Elmatica put out, of you getting notification that you had won the award. Having the "FedEx guy" come out of the frozen lake in Norway was great stuff.

Pedersen: Yeah, we had to use the CEO for something! That was great fun, actually, rather than sitting there and saying, "Oh, what's a normal day at the office?" No, it was great fun, doing something different. We are usually

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Elmatica CEO Didrik Bech (left) posed as a FedEx delivery person to hand a special envelope to Jan Pedersen. **Click here to watch their creative video.**

sitting at our home offices globally now, and you just have to do something different.

Shaughnessy: Right. It seems like the work on the committees has just kept on going, despite COVID.

Pedersen: There's been a lot happening. At the same time, Elmatica had its best year ever in 2020. That's amazing. And with all this effort put into IPC, it actually started with automotive and then went through the medical addendum.

The spinoff from the medical addendum now is that we are looking into ultra-HDI levels, what we call Level D. That's something for the future; it's not far into the future but the near future, almost today. We are a group of people in IPC that is working toward 5–10 micron tracks.

Shaughnessy: Wow.

Pedersen: Yes. Now we're out to change that to something else. But we see that just during the last, say, two years or so. If you go two or three years back, most of the PCB suppliers had a big struggle if you asked them to go below five-micron tracks. Today, if you go out there, most of them do 50 microns, two mils. There are enough of them that that can do one mil or 25 microns. That's a big change, just in the last two and a half years.

Shaughnessy: That's something else. Well, it's a really good time for the industry, despite all the craziness in the last year. We've seen a lot of companies saying that they ended up doing really well. I understand you're doing more with traceability in the committees.

Pedersen: I'm working with the automotive and medical traceability, so it's a big thing there. Since IPC-1782, when they went into revision A, Michael Ford asked me to engage in that and do some jobs for traceability at the PCB level. We didn't come to the final stage. But what they're going to do next is at least, for me, I want to have a case study and see: How can we use the 1782A, the traceability standard, at the PCB level? How does it fit in?

Then maybe I have a column in your magazine, or a webinar. Well, not many of us have talked too much about the traceability of the PCB. If you think about it, automotive and medical should require a full traceability down to the PCB level and the materials there. It doesn't. That's something we need to work with. As I said, that's a case study that would bring us closer to where we are and see if we need to update that standard again.

Shaughnessy: Right. So, you'll be working more with Michael Ford? I know he's on the traceability committee. Michael is another Dieter Bergman award winner this year, and a columnist of ours.

Pedersen: Absolutely, I'll be working with Michael. There's so much to do.

Shaughnessy: This is great. Is there anything else you want to add?

Pedersen: For me, the work for IPC is quite interesting since we are developing and going into the ultra-HDI level. But as you know, when you're working with the performance standard for automotive and medical, you have to go into the other groups as well and see what's going on in our tests and cleanliness of the PCB materials.

Another spinoff is the metal base PCBs, a standard that stopped in 2013. Now we're picking that up again, creating a new test method that was missing at that time. That's going to go through the next three or four months now, so there's a lot of things to do and to be engaged in.

Shaughnessy: Well, again, congratulations, Jan.

Pedersen: Thanks so much, Andy. DESIGN007

World's Most Powerful Modular Robot

Umbratek, a cutting-edge new robotic tech startup, has just released its first robotic arm series called the UTRA series on Kickstarter.

With five different robot arm models to choose from, the UTRA series is the world's most powerful and most affordable modular robot on the market today.

Ranging from 4 to 6 axis and built with a modular structure design, each arm can be configured to meet your business needs. Being 90% produced in-house, the UTRA series is approximately 70% more affordable than leading worldwide competitors.

Driving the revolutionary UTRA series is Umbratek's ADRA Actuator series. Each ADRA Actuator is built to last and comes with a high-precision harmonic reducer made of high-strength aviation aluminum and high-carbon chromium steel.

A high-torque density, and compact structure, enable the motor to be integrated into the actuator and lessens the actuator weight. Each actuator is fitted with high-performance servo drivers, which use field-oriented control, to protect against overvoltage, overcurrent, over-temperature, reverse connection, undervoltage ESD, short-circuiting, and rotor lock. The ADRA series also uses dual GMR+TMR hybrid detection technology and comes with a 16-bit off-axis multi-turn absolute encoder.

Umbratek was built with growth in mind. With meticulous design and implementation, Umbratek is always thinking forward. They want to become a world-leading enterprise in the field of dynamic robotics and control systems and continue to explore the limits of the world, working on cutting-edge technologies, and delivering knowledge and technology to those that need it.

(Source: PRNewswire)

Friends and Enemies in Power Distribution

Quiet Power

by Istvan Novak, SAMTEC

In signal integrity, for high-speed signaling, high-frequency loss is usually considered a bad side effect that we want to minimize. The DC loss, on the other hand, matters much less, because in many high-speed signaling schemes we intentionally block the DC content of the signal.

Another description of the column title could be, "Loss may be your friend, but inductance is your enemy." This is clearly just an eye-catching generalization; we could always argue that there are cases in signal integrity, too, when minimizing losses could backfire, or at least would have its negative consequences. In power integrity it is almost the opposite: To deliver DC power, we want to minimize the DC losses, but at the same time we don't want high-frequency noise to travel along the power distribution network. Therefore, AC losses in power distribution are usually helpful.

Inductance is different, though; while it is present in all conductive structures where current flows or can flow, in power integrity, the only situation when we can consider it helpful is when the inductance is in the series path as part of an intentional (or accidental) low-pass filtering where we want to block the noise. In applications where we don't need or don't care for blocking power noise from propagating along the PDN structure, increased inductance comes with the downside that we need more capacitance to balance it. In this brief article we show you a few simulation results to illustrate these points.

As a reminder, the simplified block schematic (Figure 1) illustrates the difference between the Parallel PDN, where we do not have intentional series elements in the power distribution network and the PDN filter where the series element is placed (or taken into account) intentionally to create the filtering. This block schematic is highly simplified: three capacitors are shown in the parallel PDN path, but it can be a mix of any number of same-valued and/or different-valued capacitors. Similarly, the PDN filter can be more complex, having an entire parallel PDN on its output, composed of multiple capacitors. The series path can be more complex, too, for instance having series and parallel resistors around the induc-

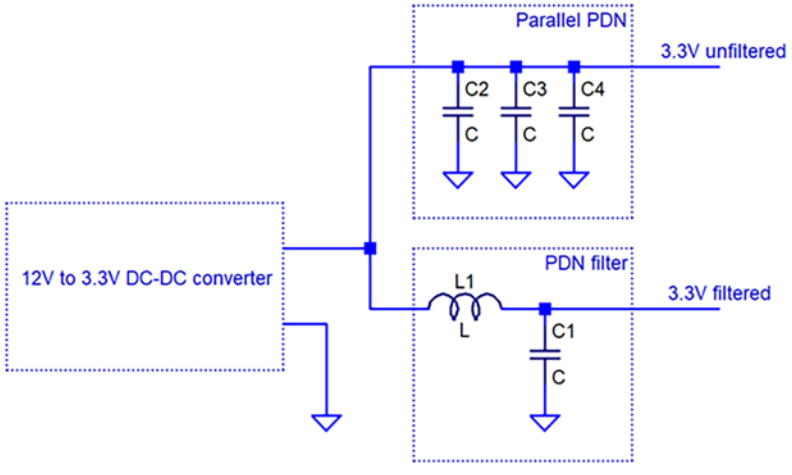

Figure 1: Block schematics of a system PDN illustrating the definitions of parallel PDN and PDN filter.

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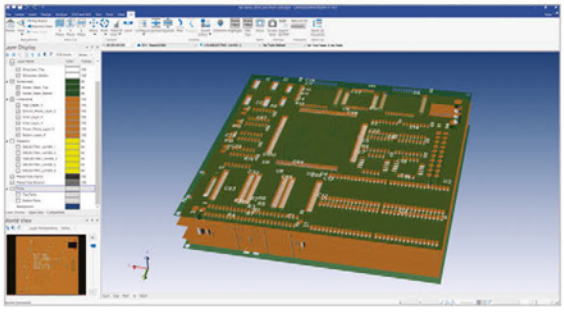

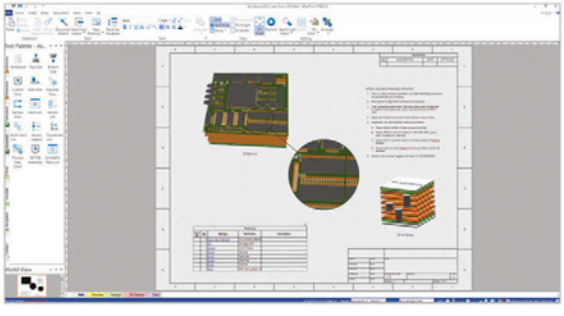

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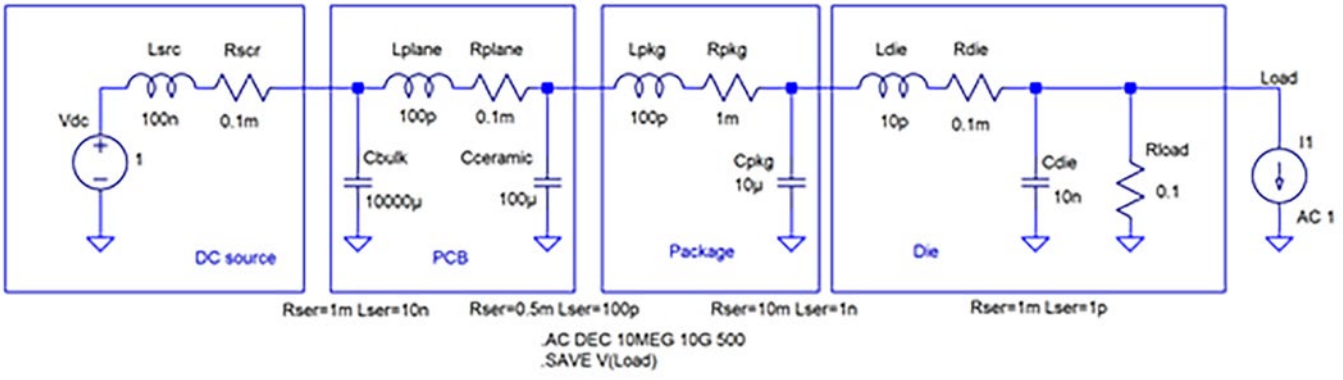

Figure 2: LTSPICE schematics of a simple point-of-load PDN.

tive component. Another illustration (Figure 2) shows a simplified schematic of a point-of-load, end-to-end power distribution network, where we explicitly identify series resistances and inductances.

We can assume that in Figure 2 all inductances are side effects: parasitics of the planes, wires, traces, connectors, as well as the parasitics of the capacitors. Note that in LTSPICE, inductors and capacitors can have parasitics assigned to the part and by doing so, instead of calling out separate circuit elements for those parasitics, will speed up the simulation. With several inductances both in the series and parallel paths, together with the capacitances, we end up with a multitude of potential resonances that we all need to worry about. This circuit was simulated and analyzed in a previous column[1].

To show the consequences of unexpected or accidental series inductance in the power distribution path, we can simplify the PDN circuit to a one-stage interface between the power source and power consumer with an L-C circuit. Figure 3 shows the circuit with its assumed component values. The current sources on the left represent the power consumer (load) and the entire power distribution network is simplified to a one-lump L-C circuit. From the allowed voltage fluctuation and assumed transient current we get a 20-mOhm target impedance. Accordingly, the source

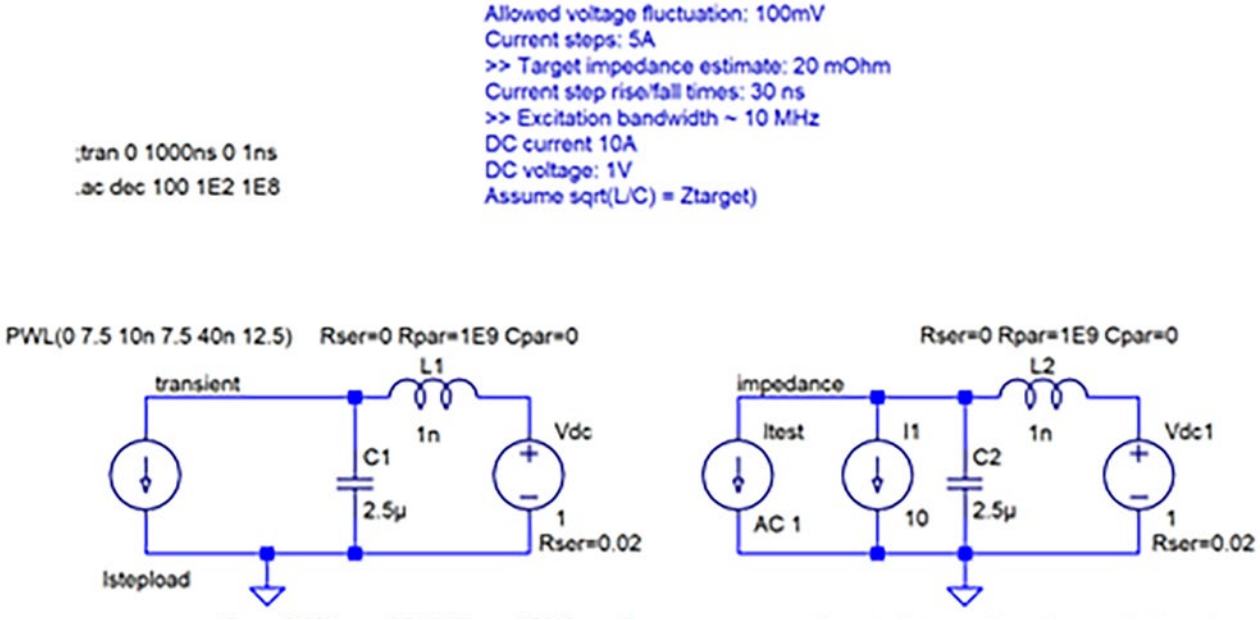

Figure 3: LTSPICE schematics for a one-stage L-C PDN circuit with matched source and load.

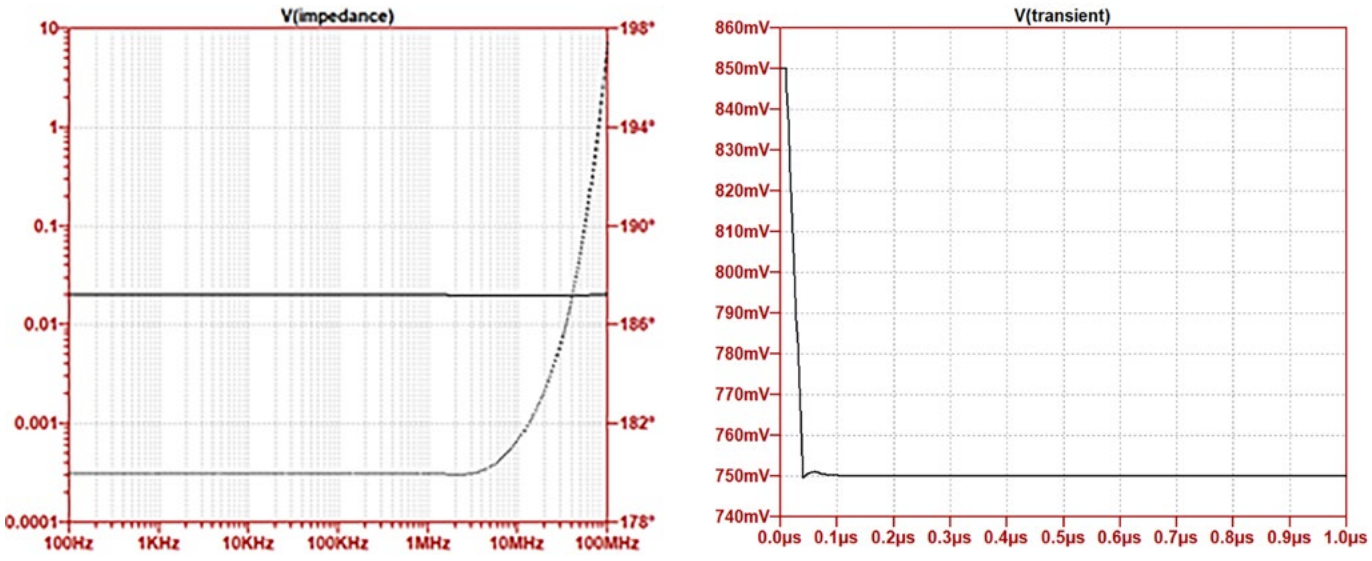

Figure 4: Impedance profile (on the left) and transient response (on the right) of the circuit in Figure 3.

resistance is set to 20 mOhms and the L and C in the PDN is selected such that sqrt(L/C) equals the source resistance, just as we would do with a single-lump transmission-line model in signal integrity. It is this matching of these three numbers that guarantees the flat impedance profile and clean transient response.

Why did we choose 1 nH for this illustration? Simply because we may get 1 nH inductance from a single via, though when we assume 10A DC current, it is not a good idea to let it go through a single via. In a real system the 1 nH series inductance may represent the inductance of the entire PCB structure. Figure 4 shows the simulated impedance looking back from the load and the transient response to a load current step. We see from the clean response that it is 2.5 mF capacitance, all what it takes to balance a 1 nH inductance at 20 mOhm impedance.

We can take the case in Figures 3 and 4 as the baseline and see what happens if for any reason

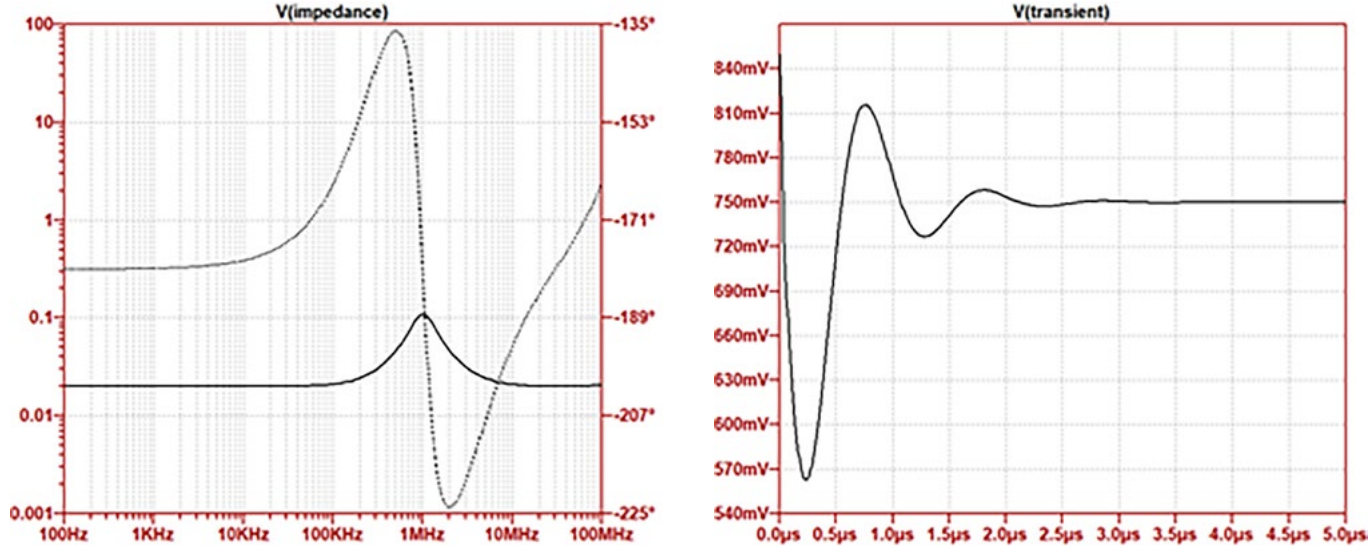

Figure 5: Impedance profile (on the left) and transient response (on the right) of the circuit in Figure 2 when we change the series inductance from 1 nH to 10 nH.

Allowed voltage fluctuation: 100mV
Current steps: 5A
>> Target impedance estimate: 20 mOhm
Current step rise/fall times: 30 ns
>> Excitation bandwidth ~ 10 MHz
DC current 10A
DC voltage: 1V
Assume sqrt(L/C) = Ztarget)

;tran 0 5000ns 0 1ns
.ac dec 100 1E2 1E8

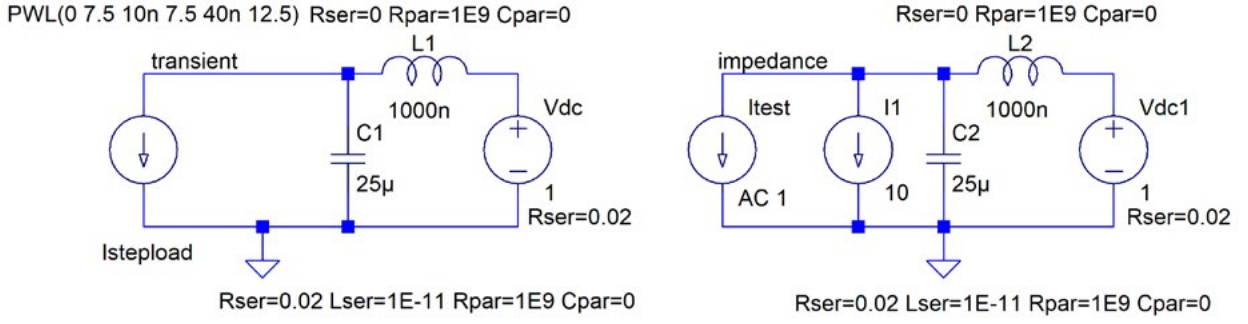

Figure 6: The circuit of Figure 3 with 1000 nH inductance and 25 mF capacitance.

the series inductance gets higher. For instance, we can increase the inductance to 10nH and leave everything else (including the parasitics) unchanged. The result is shown in Figure 5. In the frequency response we get a peak at 1 MHz going up to 100 mOhm and correspondingly we get a big 1 MHz ringing in the transient response. In a real system the 10 nH inductance may come from a connector or short wire, or may represent the equivalent output inductance of a very wide-band voltage regulator. To compensate for the increased inductance, our only choice is to increase capacitance proportionally. If we simulate the circuit of Figure 3 with 10 nH inductance and 25 mF capacitance (and leave everything else unchanged), we get back exactly the responses shown (Figure 4).

We can take the re-balanced circuit with 10 nH inductance and 25 mF capacitance as the new baseline and find out what happens if the

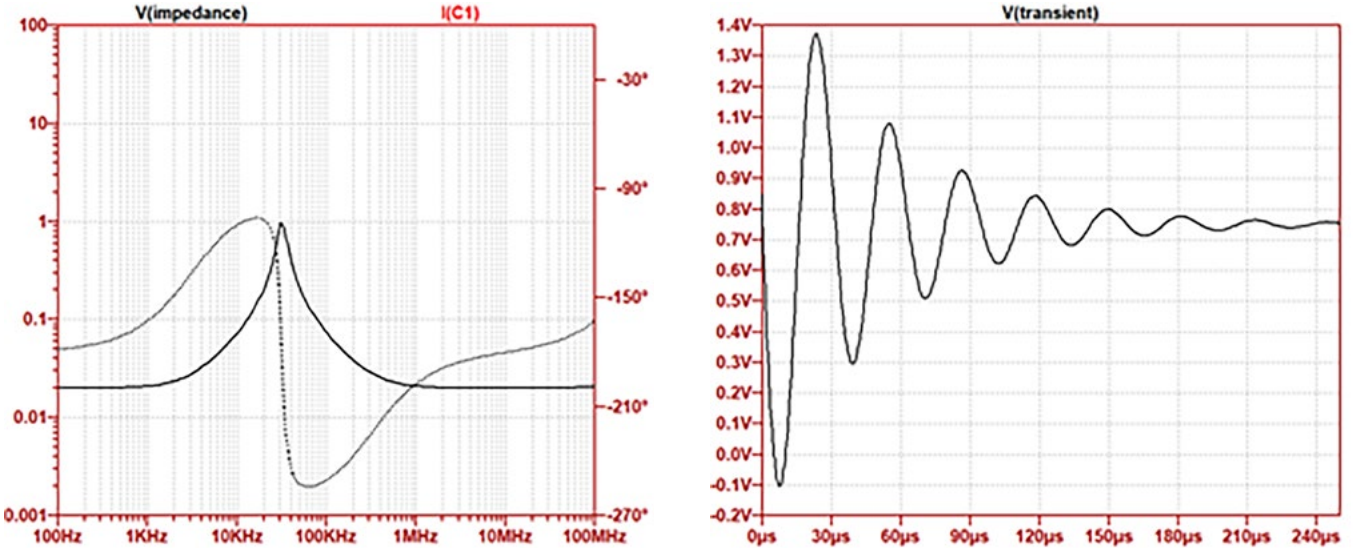

Figure 7: Impedance profile (on the left) and transient response (on the right) of the circuit in Figure 6.

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Allowed voltage fluctuation: 100mV
Current steps: 5A
>> Target impedance estimate: 20 mOhm
Current step rise/fall times: 30 ns
>> Excitation bandwidth ~ 10 MHz
DC current 10A
DC voltage: 1V
Assume sqrt(L/C) = Ztarget)

.tran 0 2500000ns 0 10ns
;ac dec 100 1E2 1E8

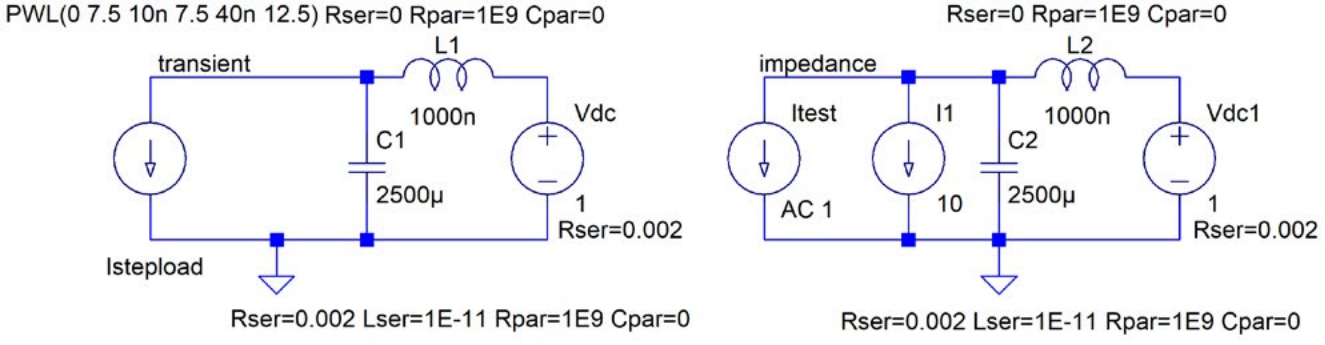

Figure 8: Illustration of the impact of AC losses.

inductance is increased further, from 10 nH to 1000 nH, or 1 mH. A 1 mH inductance could represent a one-meter-long wire-pair connecting our circuit to a bench supply. Since we changed several items along the way, in Figure 6 we capture the schematics and in Figure 7 we show the result. Note the expanded horizontal scale on the transient response: the 30 kHz peak in the impedance profile creates a huge ringing. If this was a real circuit, the voltage actually would swing negative for a short time.

We already know how to fix this: To balance a 1 mH inductance at 20 mOhm impedance level, we need 2500 uF capacitance. In a real system, when the 1 mH inductance is created by a long wire connection or a low-bandwidth active power source, we in fact need 2500 mF bulk capacitance to suppress the low-frequency

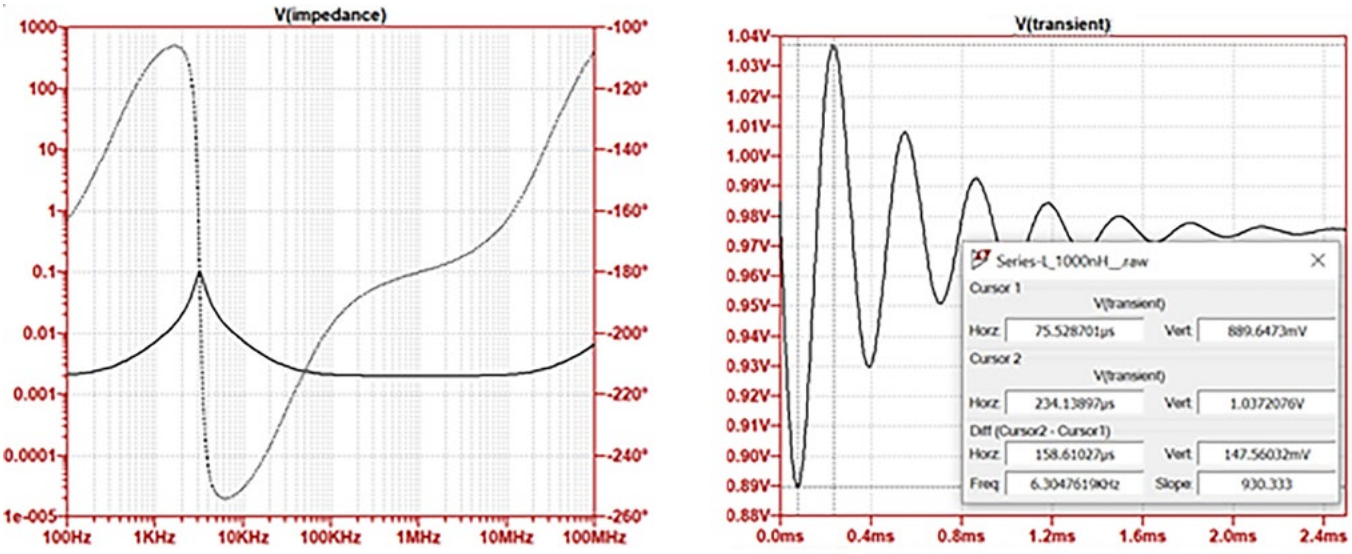

Figure 9: Impedance profile (left) and transient response (right) after we decrease AC losses by tenfold.

peaking. If we do that, the response will again be restored to what we see on Figure 4.

Finally, to illustrate further the usefulness of AC losses in power distribution systems, we show in Figures 8 and 9 what happens if we take the last design and just reduce the "losses," both the source resistance and the effective series resistance of the capacitor from 20 mOhms to 2 mOhms.

Instead of a 150mV constant drop and a 100mV transient, which can be calculated from the 20 mOhm source resistance and 7.5A and 12.5A current values, now we get a 10-times smaller DC shift and an approximately 150 mVpp ringing. While this may look like some improvement, we need to remember that the worst-case transient noise could be much higher. It happens when the current transients repetitively hit the 3.15 kHz resonance: after the 10th period, the sinusoidal ringing has a 638 mVpp value, which is 4/PI times the 100 mOhm impedance peak multiplied by the 5App transient current. The 4/PI multiplier represents the magnitude of the fundamental spectral component in the Fourier transform of a square-wave.

Summary

Inductance is inevitable in electronic circuits. To minimize voltage fluctuations on the power rail, we need to balance inductance with sufficient capacitance. The balancing capacitance we need is linearly proportional to the inductance and varies with the inverse square of the impedance we want to achieve. **DESIGN007**

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Istvan Novak is the principal signal and power integrity engineer at Samtec with over 30 years of experience in high-speed digital, RF, and analog circuit and system design. He is a Life Fellow of the IEEE, author of two books on power integrity, and an instructor of signal and power integrity courses. He also provides a website that focuses on SI and PI techniques. To read past columns or contact Novak, click here.

SolAero Technologies Powers OneWeb's Satellite Constellation

SolAero Technologies Corp. (SolAero), a leading provider of high efficiency solar cells, solar panels, and composite structural products for satellite and aerospace applications, congratulates the teams at OneWeb, Airbus OneWeb Satellites and Arianespace for the successful launch of 36 satellites of the OneWeb constellation. SolAero is proud to have supplied the solar panels for these satellites, launched from the Soyuz Launch Complex in Vostochny, Russia.

This mission brings the total fleet to 146 satellites in LEO (Low Earth Orbit). In 2021, the company is focused on scaling the satellite constellation to launch commercial services starting at the end of 2021 to the UK, Alaska, Canada, Northern Europe, Greenland, Iceland, and the Arctic Seas.

SolAero's high-efficiency solar cells, optimized to meet the performance demands of the OneWeb mission, power the constellation. To support the programs' production requirements, SolAero established the world's first vertically integrated, high-volume solar panel manufacturing facility at its headquarters in Albuquerque, NM. Established in 2018, the facility has now produced more than 1,000 individual solar panels that are powering over 200 satellites for a dozen different missions.

"This launch represents the culmination of over four years of close partnership with OneWeb and the Airbus OneWeb Satellites team and marks an important milestone in our collective efforts to provide worldwide broadband connectivity. The SolAero team is grateful to be a part of an endeavor that is transformational in so many ways and looks forward to the continued partnerships that have made this effort such a success," said Brad Clevenger, CEO of SolAero Technologies.

(Source: PRNewswire)

Why We Simulate

Feature Article by Bill Hargin
Z-ZERO

When I was cutting my teeth in high-speed PCB design some 25 years ago, speeds were slow, layer counts were low, dielectric constants and loss tangents were high, design margins were wide, copper roughness didn't matter, and glass-weave styles didn't matter. We called dielectrics "FR-4" and their properties didn't matter much. A fast PCI bus operated at just 66 MHz.

As speeds increased in the 1990s and beyond, PCB fabricators acquired software tools for designing stackups and dialing in target impedances. In the process, they would acquire PCB laminate libraries, providing proposed stackups to their OEM customers late in the design process, including material thicknesses, copper thickness, dielectric constant, and trace widths—all weeks or months after initial signal-integrity simulation and analysis should have taken place.

Speeds continued to increase in the 2000s; design margins continued to tighten, and OEM engineers began tracking signals in millivolts (mV) and picoseconds (ps). Figure 1 illustrates these trends starting in 2000, emphasizing the trajectory of PCI Express, from PCIe 3.0 in 2010 to PCIe 6.0, which is just on the doorstep.

In webinars and training events I often pose this question: "Why do we simulate?" I ask because the answers tell me a lot about the audience, and some wise older person long ago told me and my fellow students to "always know your audience."

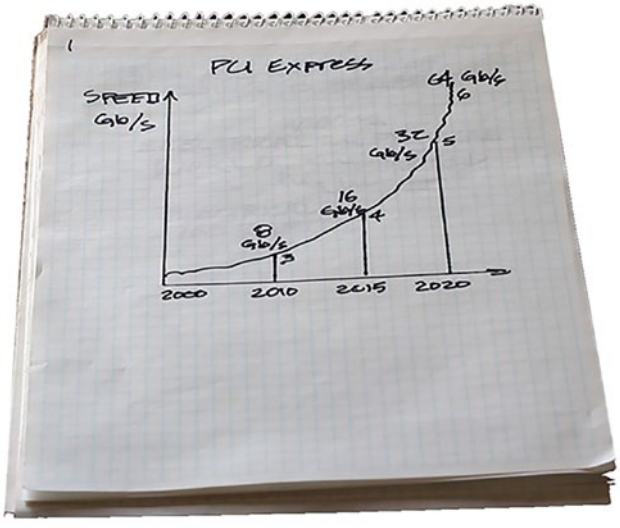

Figure 1: Interconnect speed increases in gigabits per second (Gbps) from 2000. (Artwork by yours truly.)

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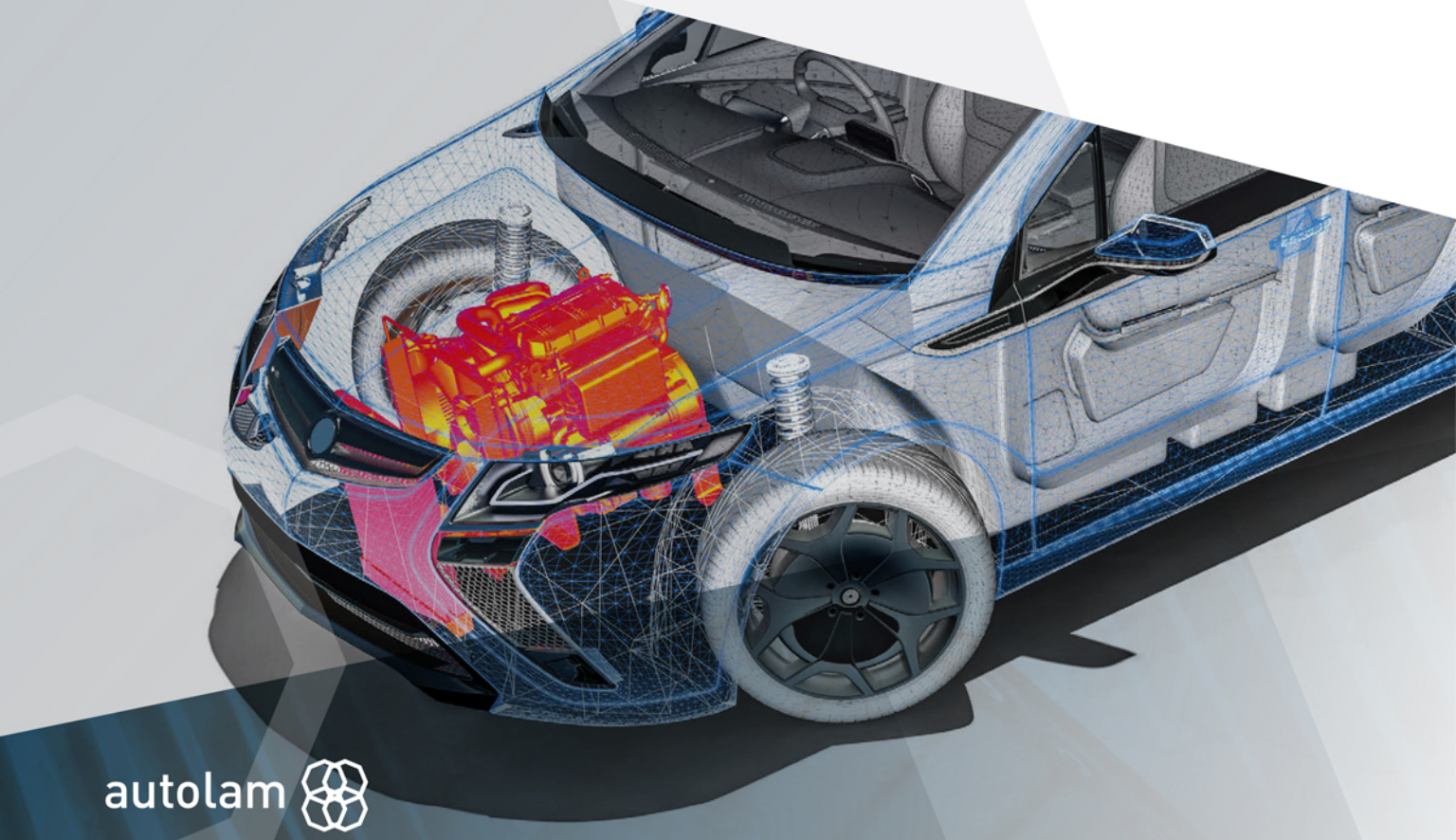

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Automotive electronics technologies are evolving at an increasing rate. Paying attention to the properties of materials at the substrate level is the first step towards achieving the most stringent performance targets of today's automotive manufacturers. autolam offers the solutions demanded by the diverse and unique requirements of automotive applications today and in the future.

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When I ask that, I get answers like faster signaling speeds, calculating impedance or loss, opening eyes and avoiding inter-symbol interference, controlling crosstalk, etc. These are all good answers, but a bit on the periphery in my view.

One astute signal integrity practitioner offered that we simulate for only two reasons:

1. To make design decisions (i.e., evaluate tradeoffs during design).
2. To verify a design before manufacturing (verification).

The only question that designers really care about is, "Will it work and by how much?" This implies that the simulation should be able to produce tangible metrics that can be related to design success or failure. Fair enough.

This is a good description for "why we simulate," but so far, I've never heard anyone mention the most fundamental reason, in my opinion, for signal integrity (SI) or power integrity (PI) simulation: To predict the negative impact that the physical world has on the electrical world, and to mitigate or prevent the negative effects proactively.

You can have hundreds of thousands of dollars' worth of VNAs, oscilloscopes, and simulation software, but simulations will be invalid unless you carefully model PCB fabrication details. The bridge between a high-speed design and a high-speed design that works across several fabricators goes through the backbone of the PCB—the stackup—which touches every single high-speed signal. My chicken scratch in Figure 2 illustrates this. (Yes, I know how to use PowerPoint.)

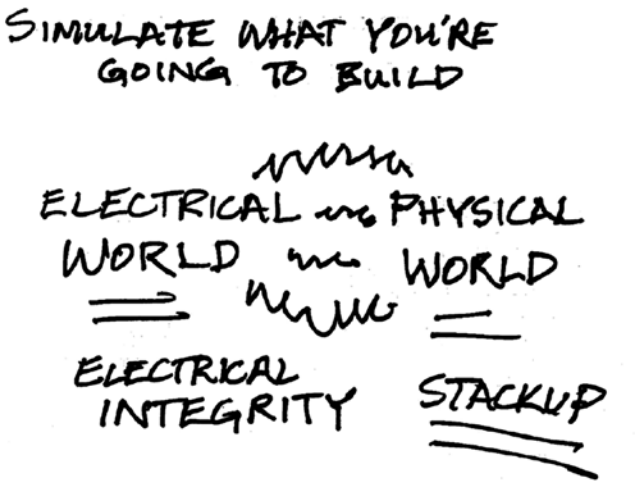

Figure 2: The fundamental reason for signal-integrity or power-integrity simulation is to predict the negative impact that the physical world has on the electrical world, and to mitigate or prevent the negative effects proactively. (Artwork by yours truly.)

To do this, we need to do our best to "simulate what we're going to build," as Figure 2 points out. A good simulator accelerates the rate at which you can experiment with alternatives, allowing engineers to optimize not only to signal quality, but also cost tradeoffs.

But it's about more than having expensive simulation tools. In my work, quite a number of PCB stackups cross my desk, and depending

The Progressive Evolution Toward Simulation

Over the years, I've tracked five different phases in the evolution toward simulating hardware performance, as illustrated in Figure 3.

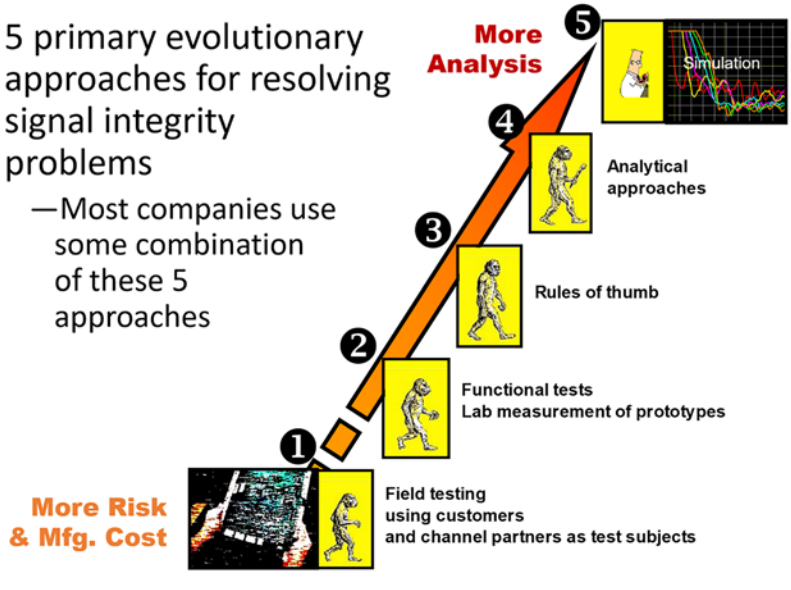

Figure 3: Most companies use some combination of these five approaches for resolving signal integrity problems.

on who or what tools were involved in a given design, there are manufacturing parameters that affect both impedance and signal loss that many design teams can improve upon. At progressively higher speeds, critical factors for signal integrity now include not only impedance, but loss, copper roughness, and glass-weave skew. Indeed, everything that happens in the process of physically building a PCB affects signal quality in a negative way and the details need to be accounted for across not just one PCB stackup, but across stackups from every PCB fabricator involved with a design.

Factors That Impact Impedance

EDA tools, including those made by my company, can be super useful, if you know what they are really modeling. Even here, the results are only as good as the data being put in. The primary parameters that affect impedance are shown in Table 1, including their relative contributions.

If you work this list from top to bottom, starting with getting a better handle on dielectric thicknesses and working your way down, you'll be better equipped to dial in your nominal parameters with enough margin to know that you're not going to fall off the cliff. And yet, every week I see engineering teams straining to perform complex analyses using datasets with questionable merit, and without fully grasping the parameters and priorities (1 through 7) noted above.

For example, I've never seen detailed, per-layer percent-copper values from actual PCB layouts being used by PCB fabricators to compute pressed prepreg thicknesses. And number 4 in Table 1 can be particularly problematic. I've searched far and wide amongst hardware OEMs, PCB manufacturers, and laminate manufacturers, and I would submit that dielectric constants are the least understood parameters in PCB fabrication. Trace width (#5) is closely tied to fabricator etching processes. Studies have shown that average PCB suppliers typically maintain roughly 0.25 mils of etchback for half-ounce copper and 0.5 mils of etchback for 1-oz. copper, respectively. Advanced PCB manufacturers can bring these numbers to 0.17 mils for half-ounce copper and 0.45 mils for 1-ounce copper. Knowing what your fabricator can maintain and modeling it in simulations can increase impedance accuracy by several ohms.

Copper thickness (#6), is another parameter that impacts impedance. I often see engineers,

Factors	Type	Rank	Description	Influence	Contribution
Dielectric Thickness	Material	**1**	Core	Thickness uniformity	**51%**
		2	Prepreg	Resin content; resin flow and % copper	
	Process	**3**	Lamination	Board thickness	
Dielectric Constant	Material	**4**	Core	Resin content; frequency; measurement method	**22%**
			Prepreg		
Trace Width	Process	**5**	Exposure	Exposure undercut	**18.5%**
			Etching	Etch factor	
Copper Thickness	Process	**6**	Plating and scrubbing	Distribution; current density	**5.5%**
Solder Mask Thickness	Material	**7**	Ink viscosity	Trace thickness; gaps/spacing	**3%**
	Process		Printing		
					100%

Table 1: Factors influencing impedance. (Data courtesy of Happy Holden.[1])

Copper Weight (oz.)	Nominal Thickness	After Fabrication	90% of Nominal
½ oz.	0.68 mils (17.1 µm)	0.6 mils (15 µm)	0.61 mils (15.5 µm)
1 oz.	1.35 mils (34.3 µm)	1.2 mils (30 µm)	1.22 mils (30.9 µm)
2 oz.	2.7 mils (68.6 µm)	2.4 mils (61 µm)	2.43 mils (61.7 µm)

Table 2: Copper foils are available in several thicknesses, measured by weight. The most common thicknesses used in multilayer PCBs are shown here, including nominal thicknesses, per IPC-4562A.

designers, and EDA tools rounding nominal copper thicknesses for half-ounce copper to 0.7 mils (18 µm), 1.4 mils (36 µm), and 2.8 mils (71 µm). I'm not normally against rounding, but when you're rounding in the wrong direction, it needs to be questioned. Table 2 lists actual thicknesses and conversions.

Board thickness, too, will be affected. On a four-layer design, the difference may not be significant, but on a 20-layer design using one-ounce copper throughout and the wrong assumptions, your board thickness will be off by as much as 4 mils. I'm pretty sure the mechanical engineers, if no one else, would appreciate it if PCB designers worked with a sharper pencil.

Conclusion

Whenever I talk in person with SI consultants—people who do SI consulting for a living—I ask them this question: "Of all the smoke-jumping projects you've been brought in for where there were serious SI problems, how many of those projects had stackup issues?"

So far, the only answer I've gotten back has been "100%." All told, the factors I've noted that impact impedance can put your designs near the edge of your tolerance targets. So, it's not just about having an expensive simulator, it's about feeding it the right parameter values, and that's much of what I've been focused on for the last few years with my company, Z-zero. Shoot me an e-mail if you have any war stories on the subject. I always like hearing from designers on the front lines. **DESIGN007**

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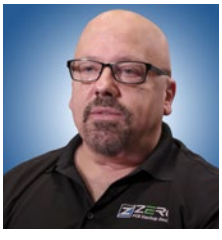

Bill Hargin is a veteran signal integrity engineer and the founder of Z-zero.

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Arlon Electronic Materials has successfully completed an intensive two-day recertification audit by IPC Validation Services. This audit was focused on validating Arlon's manufacturing processes and testing procedures. Arlon's success in passing IPC Validation Services' audit confirmed Arlon's status in the electronics industry as a trusted manufacturer of high-performance laminate and prepreg products.

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Insulectro to Acquire East Coast Electronic Material Supply ▸

Insulectro, the largest distributor of materials for use in manufacture of printed circuit board and printed electronics, has announced it will acquire competitor distribution company East Coast Electronic Material Supply (ECEMS), effective March 23, 2021.

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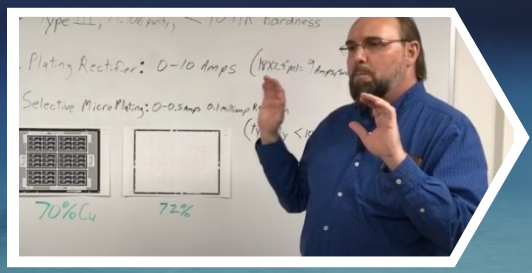

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Using Simulation to Assist With PCB Design

Lightning Speed Laminates

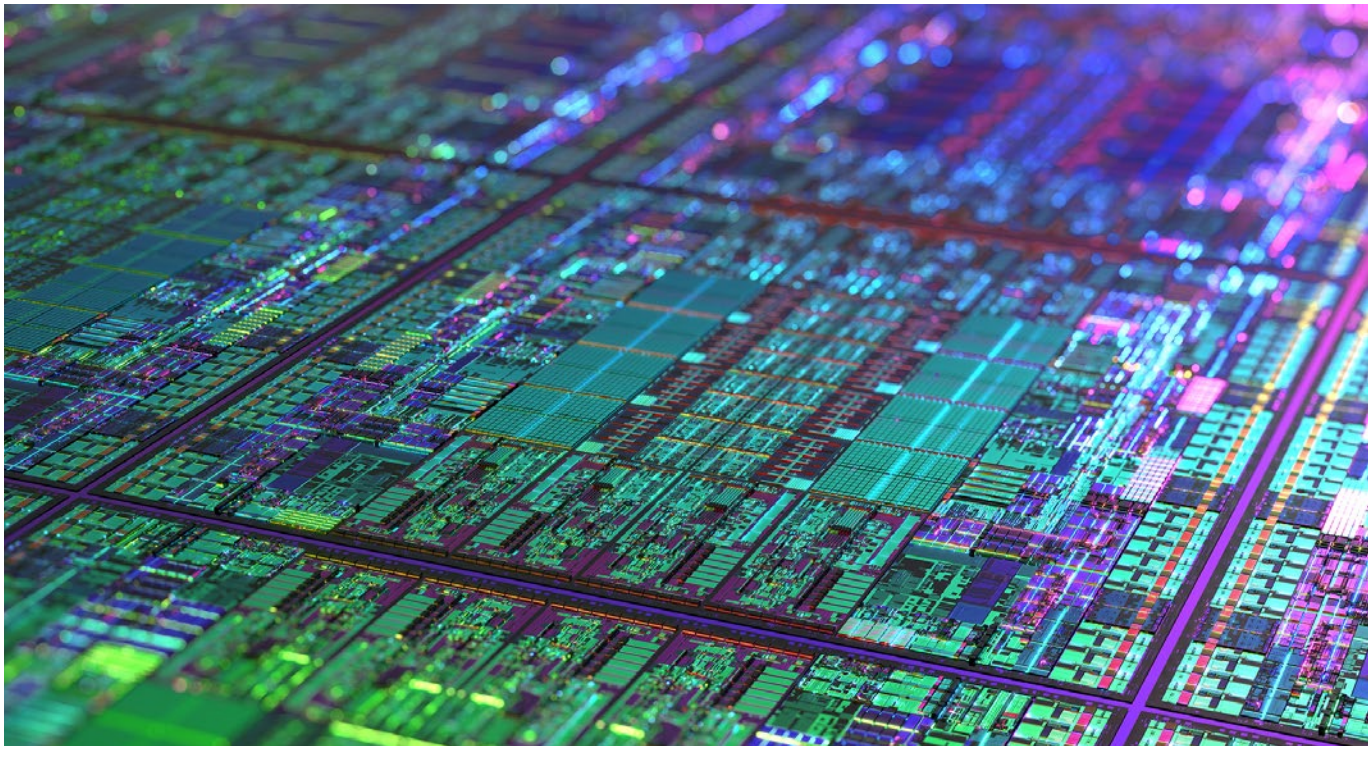
Feature Column by John Coonrod, ROGERS CORPORATION

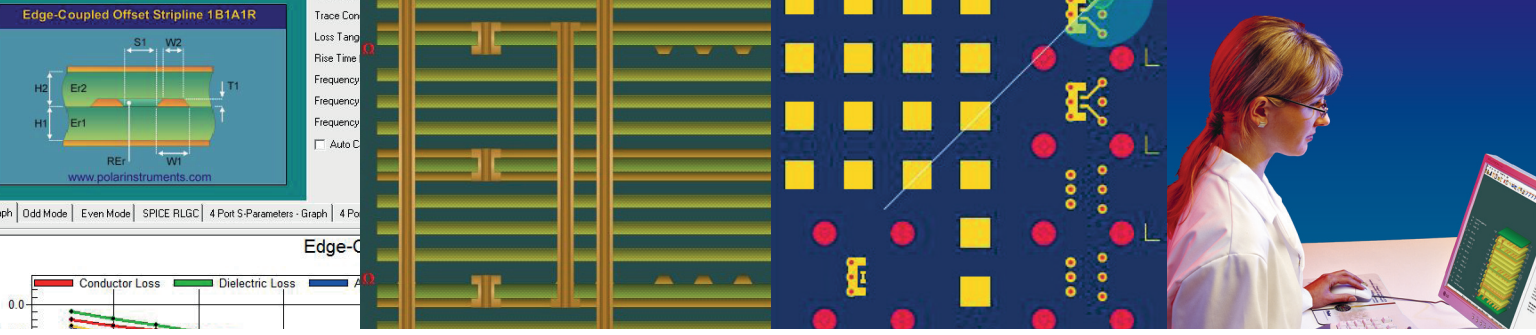
There are many different types of simulation software on the market, which can be very helpful for the PCB designer. Each tool has its own set of capabilities and limits. Understanding the basic attributes can help the designer choose the appropriate software for their design task. In general, the tool which most designers use for more complex structures, found in RF and high-speed digital (HSD) applications, is the field solver. However, there are several different types of field solvers.

Knowing the basic differences between simulation tools can be important for many reasons. In some cases, one type of field solving software will yield more accurate results than another type due to how the software performs the field solving and how the modeled structure is meshed. Additionally, the closed form equation software is usually much faster for generating results as compared to field solving software, but closed form equations are typically less accurate, and they have more limits for the type of structure to be modeled.

Software Options

There are several closed form equations programs which are used for some RF and HSD design considerations. One of these programs is available for free download from the Rogers Technology Support Hub.[1]. MWI-2019 uses many different closed form equations based





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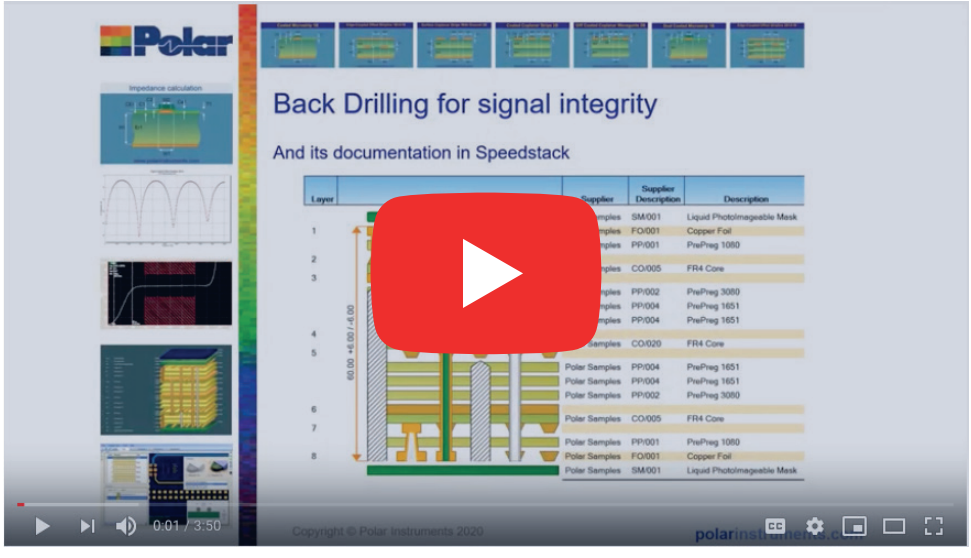

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on menu driven user-defined structures. The structures are simple transmission line circuits with configurations most used. The microstrip transmission line is a very common RF structure that is modeled using MWI-2019 and has proven to have accurate results, as compared to measured circuit performance. The software will solve for impedance, insertion loss, effective dielectric constant, wavelength, propagation delay, phase angle, and more.

The microstrip structure in MWI-2019 software yields results based on the closed form equations defined from a well-known paper published by Hammerstad and Jensen[2]. The basic procedure in this paper will solve for effective Dk, impedance, and insertion loss. The insertion loss calculation is a summation of dielectric loss and conductor loss. For frequencies greater than a few GHz, the conductor loss results need to be augmented for the effects of the copper surface roughness and specifically the roughness at the substrate-copper interfaces of the microstrip circuit. There are many different routines which can be used to account for copper roughness and the routine that works best for the type of closed form equations used in MWI-2019 is the Hall-Huray[3] model. This model allows MWI-2019 to account for the additional losses associated with roughened copper across a very wide range of frequencies.

Another item to consider with microstrip, and especially when using closed form equations, is transmission line dispersion. Microstrip circuits are known to be dispersive and basically dispersion is due to the fields of the propagating waves using both air and dielectric. Air will have no dispersion and the dielectric material will have dispersion. The dispersion associated with the dielectric material is essentially stating that the dielectric constant will change, given a change in frequency. This does not happen with air, and due to these differences, the microstrip transmission line will have different wave behavior at different frequencies—aside from the expected wave property changes with frequency, such as high frequency waves having shorter wavelength as an example. There is an excellent dispersion routine for microstrip from a paper by Deibele and Beyer[4] but considering how the closed form equations work with MWI-2019 software, a procedure by Kirschning and Jansen[5] has proven to be more accurate.

As a quick and general summary for software using closed form equations, they are much faster for generating results as compared to field solving, and they can be relatively accurate, but the accuracy is sometimes dependent upon special considerations for items related to copper surface roughness and dispersion for some models. There are other potential issues to consider for closed form equation software, however, the more accurate field solving software has its own set of issues to be considered.

There are other potential issues to consider for closed form equation software, however, the more accurate field solving software has its own set of issues to be considered.

A Field Solver Conversation

There are two types of field solvers: 2D and 3D field solvers. The 2D field solvers are best to use when the designer is considering a standalone circuit configuration on a parallel plate structure, such as a filter design on a PCB. However, if a designer would like to model the connector transition to the PCB which has the filter, then a 3D field solver would be best to use. The filter, itself on the PCB, is a parallel plate structure and 2D field solving will gener-

ate accurate results. However, the connector transition, from the connector(s) to the PCB, is a 3D problem to solve and a 3D field solver would be the right choice. For the experiments that I do, I understand the connector transition quite well (usually) from many years of experience; because of that I can use a 2D field solver to solve my design issues on the PCB that I'm evaluating.

The 2D field solvers nowadays are typically referred to as 2.5D or planar 3D and the true 3D field solvers are typically referred to as arbitrary 3D field solving. Again, these descriptions are admittedly simplified but a planar 3D field solver will solve Maxwell's equations using method of moments (MoM) and an arbitrary 3D field solver will also solve Maxwell's equations but the software may use finite element Analysis (FEA), using a mesh that is three-dimensional. The mesh is the analysis grid of the circuit to be modeled and is used to solve Maxwell's equations at discrete points, as well as how each of these points can interact with its neighboring point. These points make up the grid or mesh. An arbitrary 3D field solver will use a three-dimensional grid that will have the shape of a tetrahedron (four-sided) or maybe a hexahedron (six-sided) grid element. The arbitrary 3D solver will use these connected grid elements for everything in the circuit such as conductor layers, dielectric layers, air, etc. However, a planar 3D solver will use a planar grid (mesh) and it will be applied for the conductor layers only. The fields will still be solved in 3D for the planar 3D software, but solutions will be between the different conductor features, and so the dielectric material between these conductors will certainly have an influence. There are tricks that can be done with planar 3D field solving to get a circuit solution similar to arbitrary 3D software, such as for a circuit conductor; one can build up layers of conductors to form the overall circuit conductor which may be very thick and coupled to another thick conductor, as an example.

Conclusion

In summary (and how I typically use these programs), I will use the closed form equation software as an approximate tool and use the field solver for doing the detailed design work. I use the closed form calculators in the beginning of the design phase to go through the various tradeoffs when considering different high frequency circuit materials, thicknesses, conductor widths, RF structures, etc. Once I have the basic circuit defined from using the closed form equation software, the detailed work will be done using a field solver. However, when using MWI-2019 closed form equation software, and if I am just evaluating a simple microstrip transmission line circuit, I usually do not need a field solver because MWI-2019 is very accurate for that type of circuit and for many years I have received good correlation between the software and measured results. **DESIGN007**

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John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, click here.

Embedding Resistor Elements, Part 1

Designers Notebook

by Vern Solberg, CONSULTANT

Why is embedded resistor technology considered to be "new" and "growing" despite decades of history?

In fact, a broad number of established PCB fabricators are knowledgeable about the materials and processes for embedding resistor elements but not all may be prepared to alter procedures established for their more conventional multilayer circuit board customer base.

The next question is, "What is the motivation for embedding resistors?"

- PCB densification—a primary driver
- Functionality—a contributor
- Performance—an enhancement
- PCB assembly—simplified

The primary benefit of embedding resistor elements within the layers of the multilayer PCB is the ability to more efficiently arrange and interconnect the primary active components placed on the outer surface of the circuit boards surface. Furthermore, embedding most of the passive components can contribute to the development of a more robust PCB assembly, one that will not be physically impacted by environmental extremes or when the end product is exposed to excessive vibration and shock. Additionally, incorporating these passive resistor elements within the circuit board structure simplifies the logistics required for procurement, stocking, and assembly processing for multitudes of damage-prone ceramic-based components.

A key issue facing the PCB designer is to determine which resistors will be more suitable for embedding within the circuit board's structure and which resistor elements are more appropriate for placement onto the circuit board's outer surface. The printed board designer really acts as the facilitator and is

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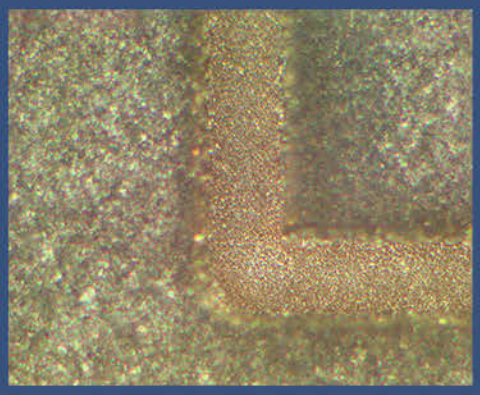

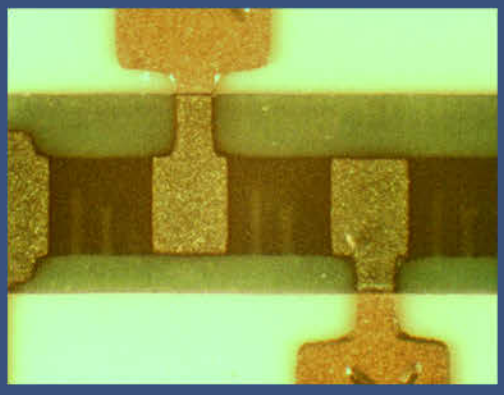

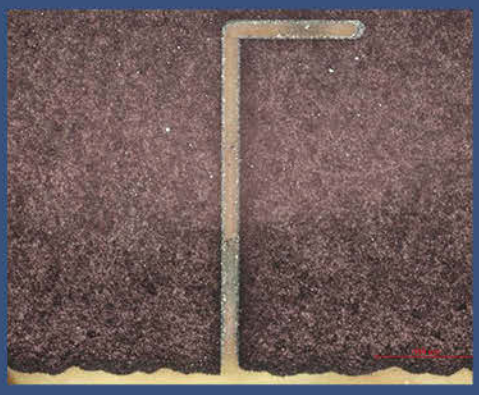

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rarely the sole decision maker for embedding components. Because of the potential cost impact on the printed circuit board, the decision to embed resistors is more likely an engineering and management level issue, typically justified by the restricted surface area reserved for mounting passive components and/or the potential for enhanced performance of the finished product.

In preparation for implementing embedded resistor technology the designer and/or program manager must first seek an experienced supplier company that can furnish practical guidance in selecting a process (thick-film or thin-film) that will meet both technical and budgetary (cost) goals established for the end product.

Formed resistor elements may be furnished as a printed thick-film composition or an imaged and chemically etched thin-film process.

- Thick-film resistor materials are formulated to furnish a wide range of primary values and have been successfully used for a broad number of commercial applications. The resistor formulations are based on carbon-filled polymer chemistry that enables screen printing or deposition to form elements directly onto pre-patterned termination lands furnished on a designated circuit board layer.
- Thin-film resistors are formed using copper foil material that is pre-coated with resistive material. The resist layer is deposited onto the copper sheet material using vapor disposition that provides uniformity of the resistor base value across the entire sheet. Thin-film resistor materials are supplied in a variety of base values using Grade 3 copper foil. The copper sheets developed for the thin-film resistor forming process are available in thicknesses of 18 µm (0.5 oz) and 35 µm (1 oz).

The information furnished in this installment of this series has been prepared to provide guidance to the circuit board design professional considering the implementation for embedding "thick-film" resistors.

When identifying candidate resistors for embedding, the designer must consider both resistor value range, the allowable tolerance bandwidth, and application. The thick-film resistor forming process is generally employed where tolerances are less critical, primarily used in digital and analog circuit applications for terminating resistors, current limiting, transistor biasing as well as for pull-up/pull-down resistors where precise value tolerances are not critical.

Resistor Functionality

Termination resistors are placed at the end of an electrical transmission line or when working with differential pair signals. Pull-up and pull-down resistors on, the other hand, are commonly used in logic circuit applications. For example, the function of the pull-down resistor is to hold the logic signal near to zero volts when no other active device is connected. The pull-up resistor's function is to ensure that the voltage between power and ground cannot be directly connected. Depending on the circuit logic type, typical values selected for termination, pull-up and pull-down resistors can vary in values that range from 500 ohm to 10K ohm and may tolerate value tolerance limits as high as ±20%. Resistor elements designated for "current limiting" are used for setting an upper limit to the amount of current that flows through a component while "transistor biasing" resistors are commonly used in combination with transistors and semiconductor components.

The overall performance of the thick film resistor materials is related to the optimized circuit design and fabrication process. The materials and process parameters of polymer thick-film resistor must be considered in order to successfully achieve the performance requirements of circuit designs. For example, the decision on what landsize-to-aspect-ratio to use for a particular resistor element depends

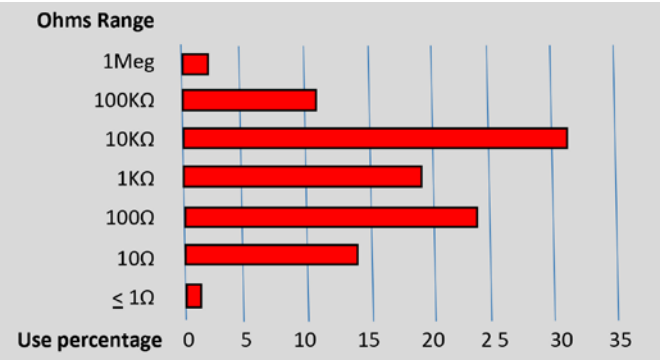

Table 1: Typical percentage distribution by resistor value.

on a number of factors. These include target resistance values, electrical considerations, available resistivity values, trimming requirements, and the distribution of resistances of all the resistors present on the same layer of the board.

In general, on most printed circuit board designs, resistor value distribution will vary between 1W at the low end and 10MW at the highest. Selecting the most practical composition for the thick-film resistors, the PCB designer should consider the most prominent base-value usage and select a material that facilitates the lower end of the value range. From a statistical standpoint, the greater number of resistors in a digital or analog circuit will likely fall into a range between 10W and 10KW (Table 1). With that in mind, selecting the 10W material as the base value will provide greater flexibility in expanding the resistor geometry to accommodate a wide range of finished resister values.

Geometry Principles

The geometry of the resistance material can be as simple as a square or rectangle, or for more complicated resistor values, a serpentine shape designed to maximize resistor element length while minimizing area. The values provided are based on the resistance measured between opposite edges of a square. For example, a single square of 1K material printed or deposited between two copper lands will provide a 1K resistor element while a pattern that is twice the length, or two squares, furnishes a 2K resistor.

The rectangular "bar" geometry (Figure 1) is most common for resistors with values close to the basic thick film composition selected while the serpentine geometry is employed when resistor values are significantly greater than the thick film materials base value. The "top-hat" shaped resistor geometry is commonly applied for elements that will likely require extensive laser trimming to reach their target value.

Suppliers recommend that designers furnish resistor widths and lengths greater than 0.25 mm (0.010 in). Larger resistor dimensions will reduce the reliance on the print variations or accuracy of the copper etching processes. Regarding terminating the resistor elements, the land pattern geometry provided for the resistor termination should allow for a nominal 0.25–0.50 mm overlap of the thick-film resist material and consider allowances for printing process variables.

As noted, the thick-film resistor ink formulations are based on a carbon-filled polymer chemistry. By adjusting the ratio of carbon content within the polymer medium, the material can be formulated to furnish a wide range of primary values. Following printing or deposition of the resist compound the circuit boards are transferred to an oven for curing at temperatures in a range between 150–250°C. Five

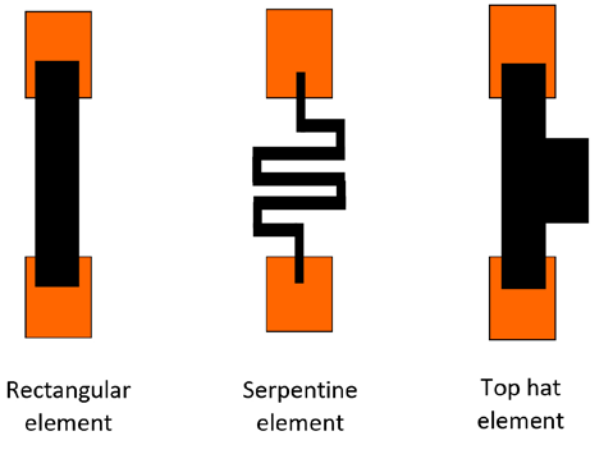

Figure 1: Thick film resistor pattern variations.

Source	Model / Series	Type	Base Value Range Ω /□	+/- % Tol.	Cure Temp.
Loctite	M2000RS	PTF	1, 10, 100, 1K, 10K, 100K	15	200ºC 30 min
FERRO (former ESL)	RS121xx	PTF	10, 100, 1K, 10K, 100K, 1M	25	150ºC 2 hours
MINICO	M2000RS MOD 2	PTF	1, 10, 100, 1K, 10K, 100K	15	200ºC 30 min.
Parker LORD	8600 Series	PTF	90-110, 900-1100, 9K-11K	20	210ºC 30 min.
Asahi	TU-00-8 Series	PTF	100, 1K, 10K, 100K	10	250ºC 2.5 min

Table 2: Thick film material selection guide. Note: The resistor value tolerance shown in column five represents the resistive material as printed and cured.

commercial sources for printable or deposited thick-film resistive materials and the base value range that they offer are furnished in Table 2.

When the application requires a value modification or a tolerance that is better than that noted in Table 2, laser trimming systems can be employed to make the necessary adjustments. The examples shown in Figure 2 illustrate thick film resistors that have been modified using laser technology to achieve a specific value or tolerance target.

Laser trimming systems developed for high volume PCB fabrication are equipped with multiple flying probe contactors that are pre-programmed to reach any component location, size, orientation and layout within the board or multi-unit panel. The probe contactors sweep across the board's surface contacting the embedded component lands or dedicated test point locations to measure and transmit the resistor value and tolerance as printed to direct the laser in making the required cut (Figure 3). Automated calibration routines ensure cut placement accuracy within 15 microns. Cut widths are typically in the 10–50-micron range.

Those considering thick-film resistor technology must understand that the process requires precise imaging and consistent mate-

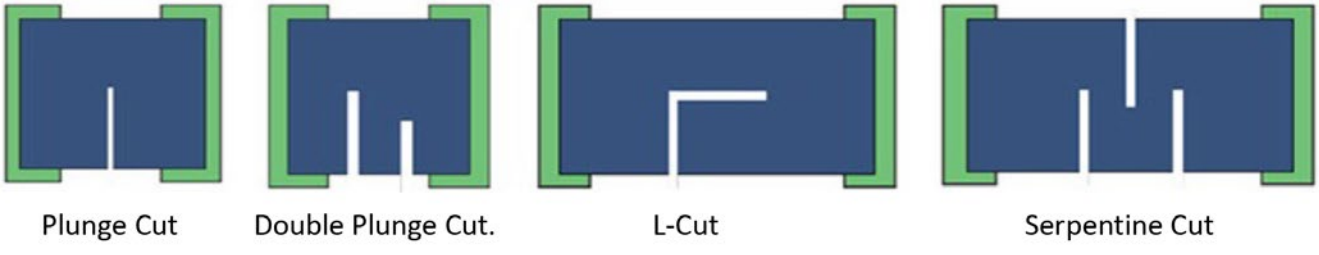

Figure 2: Laser trim variations for thick film resistor elements. (Trim examples courtesy of PPI Systems)

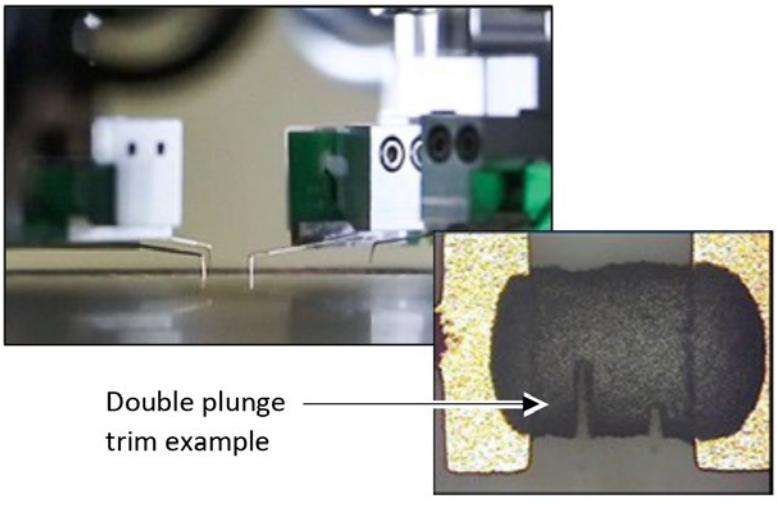

Figure 3: Laser trim system equipped with flying probe contactors. (Source: PPI Systems)

rial density to ensure that the printed image will meet the target resistor value range. And due to the printing and curing complexity for printed thick-film resistors, the printed board fabricator will prefer applying only one resistor base value material onto a single substrate layer. If the fabricator can use an inkjet-type of deposition process, however, they will have greater latitude in applying two or more base value resistive ink compounds onto a single circuit layer.

Although the thick-film resistor forming process has a long history and remains a popular, low-cost solution for embedding, many PCB fabrication companies may not offer this capability. This is because thick-film resistor forming is considered a wet process requiring controlled storing, careful mixing, printing and curing operations. PCB fabricators that do offer embedded resistor capability will often prefer to adopt alternative thin-film processing solutions.

In Part 2, I will review the materials, design rules, and process parameters for embedding formed thin-film resistors. **DESIGN007**

Vern Solberg is an independent technical consultant, specializing in SMT and microelectronics design and manufacturing technology. To read past columns or contact Solberg, click here.

Linde, Bluefors to Develop Cryogenic Cooling Solutions for Large-scale Quantum Computing Technology

Linde and Bluefors have joined forces to create cooling solutions for large-scale quantum computers. Linde is contributing its vast experience as the world leader in large cryogenic installations. Bluefors brings to the table its ultra-low temperature interface needed for quantum computing. Their combined effort supports this emerging industry by ensuring cryogenics are ready for the next steps in large-scale quantum computing, in terms of cooling power, efficiency and robustness.

In the initial phase of the partnership, the companies focused on identifying how the technologies work best together. Currently, both partners are collaborating on implementing the results to get their joint product ready for market.

"After our first meetings, it was clear to both Bluefors and Linde that this was a perfect match for the next phases," said Rob Blaauwgeers, CEO of Bluefors.

Quantum computers have the potential for computational power that is unattainable by current computers. They can operate exponentially faster than conventional computers and could, thereby, be the solution to today's insurmountable problems. Cryogenics is a critical component in harnessing this quantum power and the ability to cool down large-scale quantum circuits is essential. Together, Linde and Bluefors have embraced this challenge to ensure that the next stage in cryogenics is ready and able to meet this need.

(Source: PRNewswire)

MilAero007 Highlights

NASA Takes Steps to Reduce Aviation Emissions, Invigorate U.S. Economy ▸

NASA is seeking proposals for ground and flight demonstrations of integrated megawatt-class powertrain systems for subsonic aircraft.

IPC Commends President Biden for Executive Order on Industrial Supply Chains ▸

IPC commends President Biden for ordering a review of industrial supply chains critical to U.S. economic growth, innovation, and security.

NEOTech, Numerica Provide 3D Radar for C-UAS, Short-range Defense Missions ▸

NEOTech, a leading provider of manufacturing technology and supply chain solutions for brand name OEMs in the industrial, medical and mil/aero markets, is thrilled to congratulate Numerica Corporation on the announcement of their new short range surveillance radar system.

Sypris Wins Defense Contract Award ▸

Sypris Electronics, LLC, a subsidiary of Sypris Solutions, Inc., announced that it has recently received a follow-on award from a U.S. DoD prime contractor to manufacture and test electronic power supply modules for a mission-critical, long-range, precision-guided anti-ship missile system.

'Space Bridge' Helps UK, Australia Get Ahead in Global Space Race ▸

The world's first Space Bridge will unlock improved access to trade, investment and academic research opportunities, better advice to businesses and innovative bilateral collaborations.

Boeing: Southeast Asia Aviation Market Well Positioned for Recovery ▸

Boeing anticipates airlines in Southeast Asia will need 4,400 new airplanes valued at $700 billion to support expanding demand for air travel over the next 20 years.

It's Only Common Sense: 10 Ways to Bring the PCB Business Back to America ▸

The winds of globalism seem to be blowing in our direction, and I see indicators that we can bring at least a significant portion of the PCB market back to America in the next few years. That is, if we stick together and do things right.

Collins Aerospace Wins Contract to Support CH-47F Fleet for Royal Netherlands Air Force ▸

Collins Aerospace, a unit of Raytheon Technologies Corp., has been awarded a multi-year Performance Based Logistics avionics support contract to the Royal Netherlands Air Force's fleet of 15 CH-47F Chinook helicopters.

BAE Systems Acquires Pulse Power and Measurement Limited ▸

Pulse Power and Measurement Limited (PPM) and BAE Systems have announced that BAE Systems has acquired PPM, an independent developer and manufacturer of high-end electronics.

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The Power Behind the (PCB) Throne—Power Supply Design Tips

Connect the Dots

by **Matt Stevenson,** SUNSTONE CIRCUITS

Delivering the required power to each component on a PCB can be a complex challenge. Designers must manage converting AC to DC while also delivering the correct voltage and current to each component. A well-designed PCB results when the designer takes power supply seriously—paying close attention to the effects that power delivery can have on surrounding components, such as through heat management or signal interference.

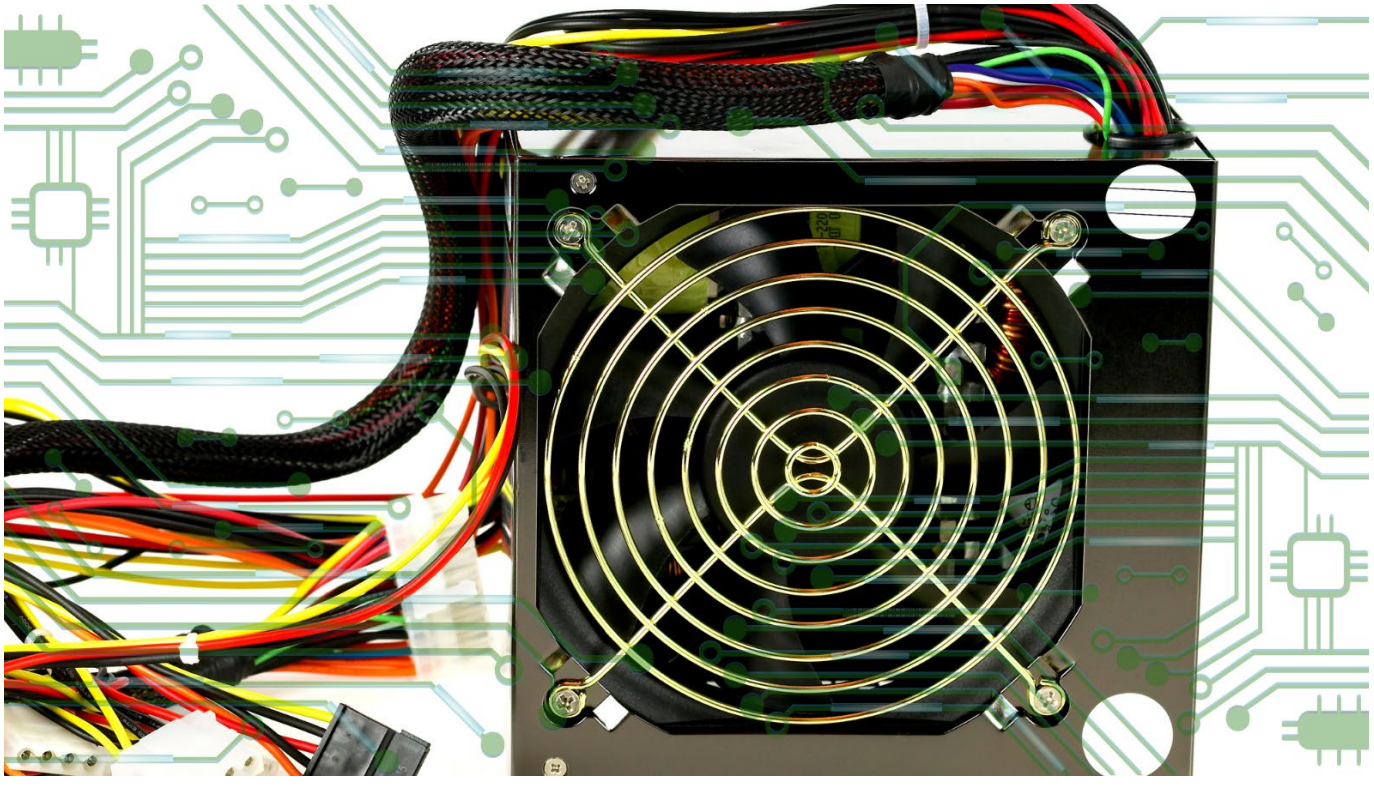
Maintaining Power Quality and Integrity

The International Electrotechnical Commission defines power quality as:

A set of parameters defining the properties of the power supply as delivered to the user in normal operating conditions in terms of continuity of supply and characteristics of voltage (magnitude, frequency, waveform).

No matter how well designed your power supply is, it can only control the quality of voltage. It cannot control the current that various loads might draw.

Power integrity is achieved when the quality of power delivered to a circuit remains constant and predictable. For a circuit to achieve its desired performance, it needs power to be effectively transferred from the power supply



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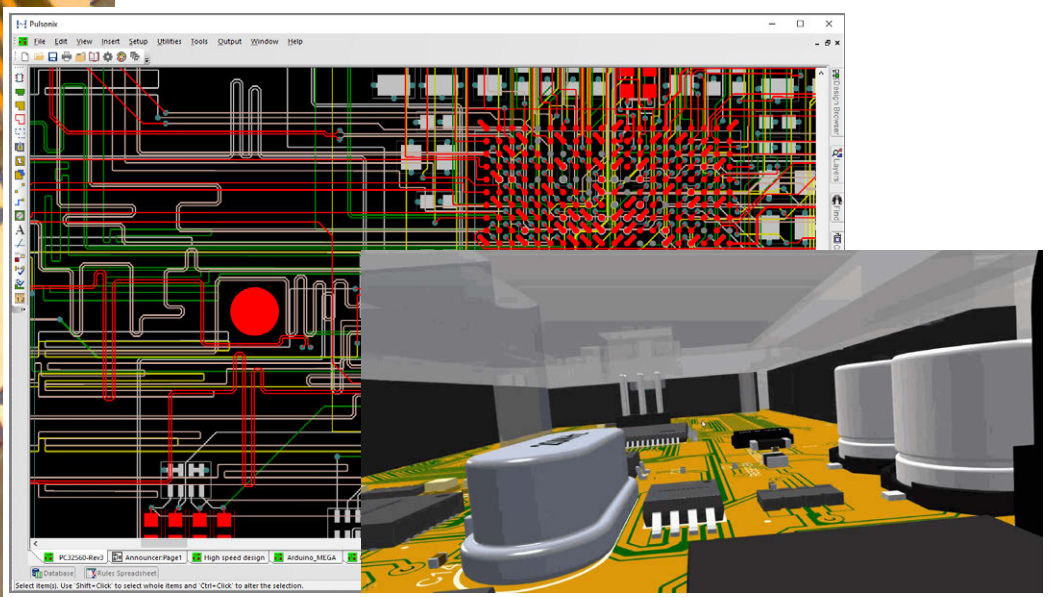

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to every component, circuit, and device as expected. Power integrity is measured by how effectively power is transferred from the power source to components in the system. A design needs to ensure that all components are supplied with the appropriate power level to achieve target performance of the entire circuit.

Power quality can be negatively affected by noise, so one important design goal is to minimize that noise. You should start, of course, by being familiar with the power supply requirements for all your ICs and components. Higher quality power supplies can produce less noise, as well.

Keeping It Inside

If your board has three or more layers, keeping the power and ground planes on one of the internal layers can make a lot of sense. Not only can this help add structure to the board, but it gives easy access to both power and ground from other layers while helping to keep your PCB design clean.

Since it is better to supply power to certain components in parallel rather than serial, designing your power plane on an internal layer can really help keep the layout clean on the outer layers. This can keep you from backing yourself into a corner with power delivery and forcing you to daisy-chain your ICs together. You will easily be able to create wide, solid, common power rails without interfering with the rest of your PCB design.

Separating your ground and power planes can also help reduce electromagnetic interference while distributing power. Not only will this reduce strange signal patterns, but it can help prevent unexpected voltage drops, too.

Thermal Regulation

Heat dissipation directly impacts the performance of a power supply. Almost every component will emit some amount of heat when current is applied, and the amount of heat depends on the level of power applied, the particular characteristics of the component, and impedance. Higher temperatures impact the performance of a circuit, which means that power supply design also includes cooling design.

If your design uses a linear regulator to maintain steady voltage and manage power quality, you may need to integrate a cooling method such as heat sinks or fans. However, the right regulator can reduce heat dissipation in a circuit. Switched regulators, in particular, can be helpful for this since they dissipate less heat.

Using Power Supply Problems to Diagnose Circuits

Remember that the power supply can only control the quality of the voltage it provides. It has no control over the current being pulled by various components or loads. Luckily, this means that sometimes power supply issues can help you locate faults in your PCB design. For instance, voltage sags or interruptions can indicate a fault or short circuit somewhere in your design.

Power spikes and unexpected voltage drops could indicate that certain components are drawing unpredictable amounts of power under certain loads. If you are seeing this behavior in your circuit, consider using decoupling and bypass capacitors to mitigate voltage drops and maintain power quality.

A decoupling capacitor reduces impedance between power and ground. It acts like a secondary power source for components by smoothing over voltage drops. Use a bypass capacitor to help reduce flutter, or power fluctuations, which are usually the result of too many ICs pulling voltage simultaneously. Bypass capacitors are usually placed closer to ICs or components.

Good Power Supply Design is a Core Practice

No matter how solid the rest of your PCB design is, without good power supply design, your circuit will not reach the level of reliability you would probably like. You will need to pay attention to not only the physical layout of the power supply on the PCB, but the way voltage fluctuates, spikes, and drops across segments of your circuit. You will also need to watch for heat issues and electromagnetic interference, all of which are core issues that good power supply design is intended to mitigate. **DESIGN007**

Matt Stevenson is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Stevenson, click here.

SEMI Applauds Initiatives to Bolster Semiconductor Manufacturing, Research in American Jobs Plan

SEMI, the industry association serving the global electronics design and manufacturing supply chain, applauded the inclusion of initiatives to strengthen U.S. semiconductor manufacturing and research and calls for investment in the Biden Administration's American Jobs Plan. In addition to calling on Congress to invest $50 billion in semiconductor manufacturing and research, in line with the bipartisan CHIPS for America Act, the plan lists semiconductors as a field of focus in its call for an investment of another $50 billion in the National Science Foundation (NSF).

"Reversing the 50% decline in the U.S. share of semiconductor manufacturing capacity over the past 20 years requires bold action, and the Biden administration's support for significant funding to bolster the industry in its American Jobs Plan is an important step forward," said Ajit Manocha, SEMI president and CEO. "Funding the authorized CHIPS For America Act provisions and enacting an investment tax credit to support investment in the U.S. semiconductor supply chain will make the United States a globally competitive location for new semiconductor facilities. The plan's focus on addressing workforce development in the industry is encouraging as well, as the competition for talent is intensifying to support projected growth."

(Source: SEMI)

PCEA Expands in its Sophomore Year

Interview by Andy Shaughnessy
I-CONNECT007

I recently spoke with PCEA's Scott McCurdy and Tomas Chester about the organization's plans for its second year. They explained that they plan to add new chapters and members, especially younger engineers like Tomas.

Andy Shaughnessy: How are you guys doing? For those who don't know, Scott is the chapter liaison and chairman for PCEA, and Tomas is the founder of the PCEA chapter in Ontario, Canada.

Scott McCurdy: I'm doing great in this work-from-home environment.

Shaughnessy: Nice to meet you virtually, Tomas.

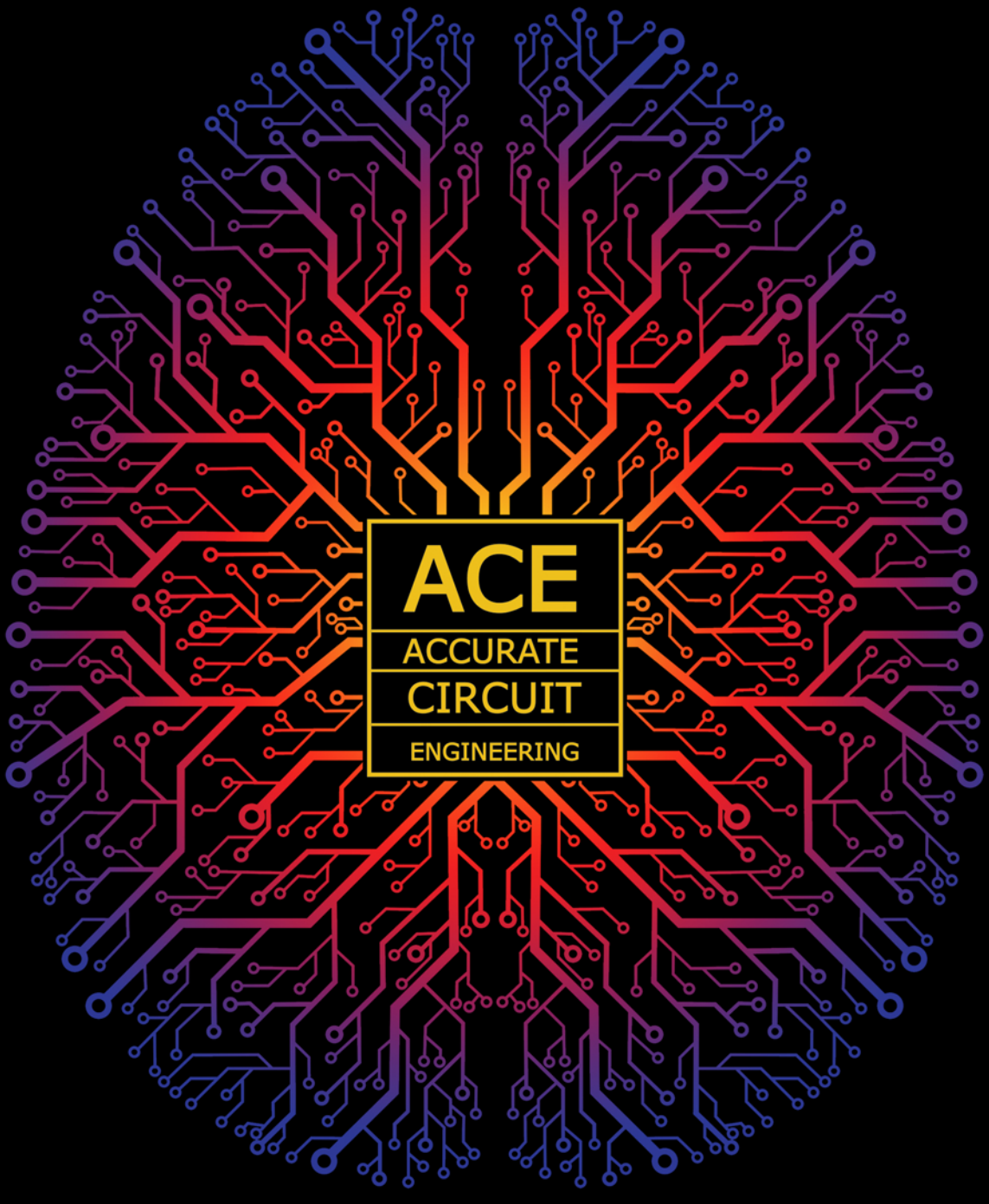
Tomas Chester: Nice to meet you, too, Andy. Working from home has been okay for me. I don't have to drive through four feet of snow to work every morning.

Shaughnessy: That alone makes it worthwhile. Scott, the PCEA is now in its second year. Give us an update on what you've been up to.

McCurdy: The PCEA (Printed Circuit Engineering Association) is an international network of engineers, designers, fabricators, assemblers, and anybody who is related to the printed circuit development world. We started in late 2019. It's a volunteer nonprofit organization. I got involved because I was one of the executive board members of the IPC Designers Council, and we were "orphaned." That led to the birth of a new organization with a bunch of the chapters that had no place to go. We formed a new organization around that, and it's been great.

I was president of the Orange County chapter of the Designers Council for 17 years, so we transitioned into PCEA and then immediately had to start doing virtual meetings. This led us to find new members or having them find us. Many people may not live in an area where there is much electronics activity, yet they were still looking for a place to collaborate.

Don't Overthink Your Prototype Builds



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Tomas Chester

Our mission is to collaborate, inspire, and educate; that's what our meetings are all about. We try to bring in interesting topics and speakers, and then get a good-sized group of folks to share with. It's been enlightening; it really has. We've grown quite a bit. I'm involved in the membership committee, so we're trying to help form these new chapters. And we've made alliances with other like-minded industry associations. We all promote each other for mutual benefit, which has been interesting.

Some of our people have been active in the standards committees at IPC and even leading some of the standards committee groups, so we all benefit from sharing information. We have a relationship with SMTA as well.

It's a volunteer organization, so it's all about getting new people to join. It was interesting that we came across Tomas in Canada, an area that we hadn't really paid a lot of attention to. I'm going to let him talk about how he drifted into our group and how much he's been able to accomplish since.

Chester: I had the good fortune to be introduced to Michael Creeden, and I'd asked him to be a mentor, right about the same time the PCEA was being formed. I think one of the things that is missing in this industry, which the PCEA does a very nice job with, is looking toward education. There aren't many mentors in this industry anymore who provide guidance and information, not just in a technical sense, but also in a general career sense, and understanding of the industry.

Through that, Mike had challenged me to create an Ontario chapter here in Canada. At the end of 2020, I was looking at doing that, and it was great because the PCEA leadership was very supportive. I remember meeting with Scott and Stephen Chavez, and a couple of other members. They said, "Okay, this is how you run your meetings. This is how you can get people involved. Now that we've launched your chapter and it's actually set up, we want to help you in running your events as well. To ensure that we have a great kickoff, let's bring in a couple of other new chapters together at the same time."

Then, at the beginning of January, we did a tri-city kick-off. We launched three chapters: Ontario, Canada; a Michigan chapter; and Minneapolis-St. Paul, Minnesota. By doing that, it really expanded our boundaries. It also means that we're going into these new areas and communicating with people who probably didn't realize there was an industry association like this that could help and support them. We're allowing that kind of connectivity among engineers, designers, and fabricators. We're building those connections.

Shaughnessy: The Designers Council had started using WebEx right before COVID, so the members in the middle of the country could feel like they were part of a chapter. That meant you were more or less ready to go with video meetings when the pandemic hit.

McCurdy: Yes. In my chapter we were recording and editing it, and then making that

available to even the people outside of our normal folks who showed up. But boy, was that timely. And it's not pre-recorded; we do the meeting live. That took a little bit of getting used to, but without this kind of technology, we wouldn't have been able to get this thing off the ground.

Shaughnessy: What's your impression of PCEA so far, Tomas? Are they putting you to work?

Chester: Yes, the challenges keep coming. We're looking at the present and where things are right now, but also looking toward the future and wanting to bring in new members, not only just in terms of forming chapters, but also start bringing in some of those new members toward the executive group—taking over and pushing this forward to the new generation of designers, engineers, and fabricators who are going to be coming through the industry.

McCurdy: Tomas has been invited to be on the executive board in a well-deserved position, and he'll bring a youthful exuberance and his knowledge base onto our team. We're excited to have him.

Shaughnessy: Well, congratulations, Tomas.

Chester: Thank you.

Shaughnessy: So, this year's IPC APEX EXPO was virtual. How did that change how you approached the show?

McCurdy: I think when you have a virtual presence, you just hope somebody comes into your virtual booth, and then you can start the discussion. Obviously, we are still looking for other people like Tomas who would be interested in having us help them form chapters in their area.

Chester: I think with APEX EXPO moving over to digital, you are, of course, trying to get

Scott McCurdy

somebody to come in and talk to you. But at the same time, by switching to a digital environment, it's now more widely available. I don't need to worry about the cost of travel or staying in a hotel in San Diego. I can easily access all the information I need, because I don't need to necessarily cross the show floor to interact with other people. Everybody is literally just a click away.

Shaughnessy: There are benefits to having a virtual show. Anyone on the planet can attend.

McCurdy: But meeting each other in person is the part that we really miss.

Shaughnessy: Let's hold a good thought for next year's show. Thanks for speaking with me.

McCurdy: Always a pleasure, Andy. Hopefully we'll have even more PCEA chapters by next year. **DESIGN007**

Simulating Stackup and Signal Integrity

The Pulse

Feature Column by Martyn Gaudion, POLAR INSTRUMENTS

Simulation and modelling are long-time friends of the engineer. I recently read *The Works of Isambard Kingdom Brunel* [1] (Pugsley). The math and modelling that accompanied his civil engineering works almost 200 years ago are quite humbling—even more so given that all his calculations were made by hand, devoid of the luxury of high-speed computing that bathes the engineer of this century in an abundance of tools.

But the purpose of modelling then was the same as now—to reduce the number of prototypes, to predict safety margins for structural loads, and, in Brunel's case as an engineer, he also had a head for marketing as his mathematical and engineering abilities allowed him to build bridges with fewer materials and shallower curves than had his peers doubting their longevity. However, here we are 200 years later, and high-speed trains and traffic are still using his elegantly designed structures with safety.

Just as with modern engineering challenges, the materials in his hands were not ideal, wrought iron was relatively new, and wooden structures, though well understood, were still natural materials and subject to the ravages of damp and decay over the life of the structure. Brunel had to understand both the math, and the limitations and inherent variability of the materials he deployed. This was especially the case in tunnelling operations where, despite geological surveys, the nature of the material being tunnelled was not always as predictable as expected.

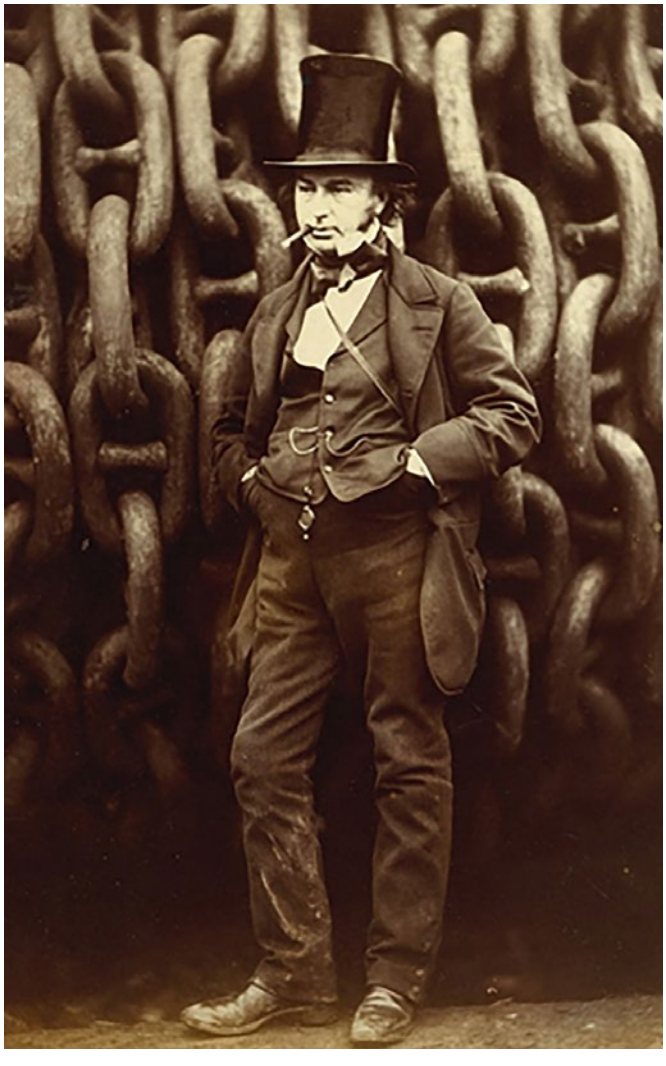

Figure 1: Isambard Kingdom Brunel. (Source: Wikimedia Commons.)

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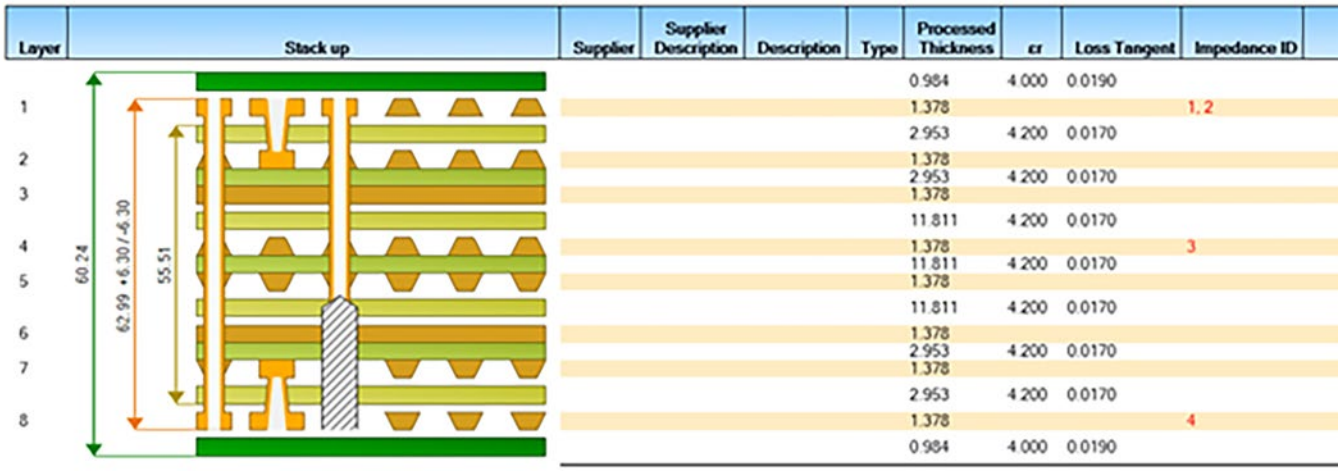

Figure 2: Virtual or generic materials. (Report: Polar Speedstack)

Electronic designs in which the architecture deploys the PCB are also subject to variation, and just like Brunel, when designing a PCB in today's computer simulated environment, it helps to have a thorough understanding of the foundation you are using to build your design. The unsung hero of electronic designs—the PCB—provides the mechanical, thermal, and electrical platform on which 90% of electronic designs are realised.

Simulation can only be as good as the source data, so the better understanding you have of the materials in your stack, the better the understanding of the effect of the PCB production process on those materials. This puts you a step ahead when you are modelling how the finished product will behave. Modeling stack-ups involves a mix of disciplines, the simulation tool needs to know the material types, the glass/resin ratios, and the target copper density of the finished design to predict how the materials will press and cure into the final finished height. Locations of drill ends are needed so that plating thickness can be accounted for.

Understanding Materials

Returning to the civil engineering analogy, when tunnelling it's a matter of life or death, so it is vital to understand the strata you are working in. With PCBs, careful consideration of the substrate materials can yield benefits. Working with spread glass reinforcement as opposed to

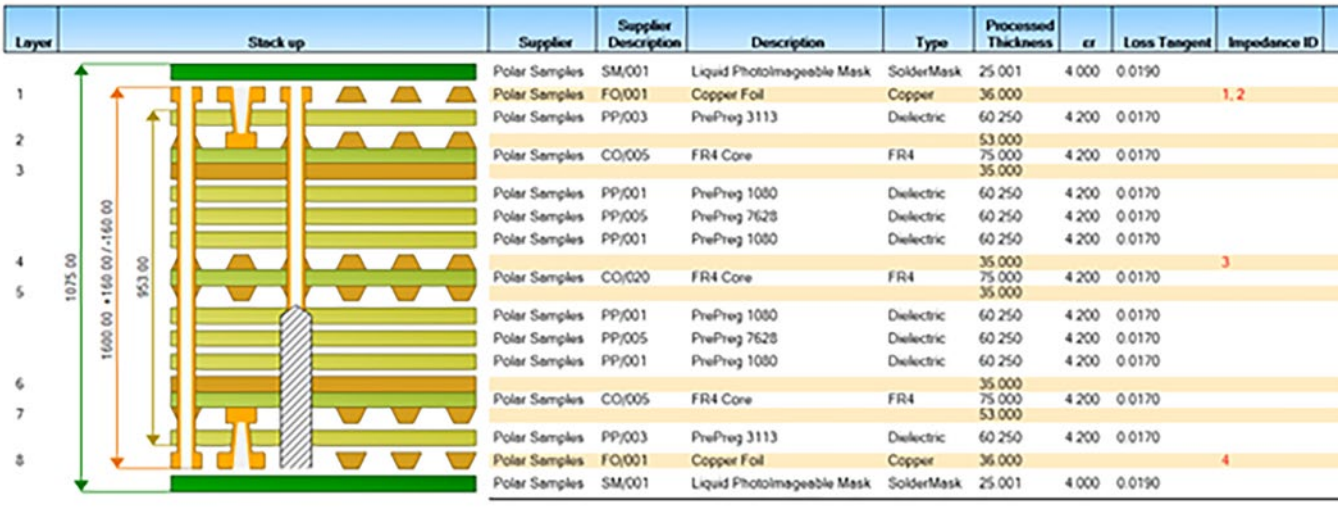

Figure 3: Mandated materials. (Report: Polar Speedstack)

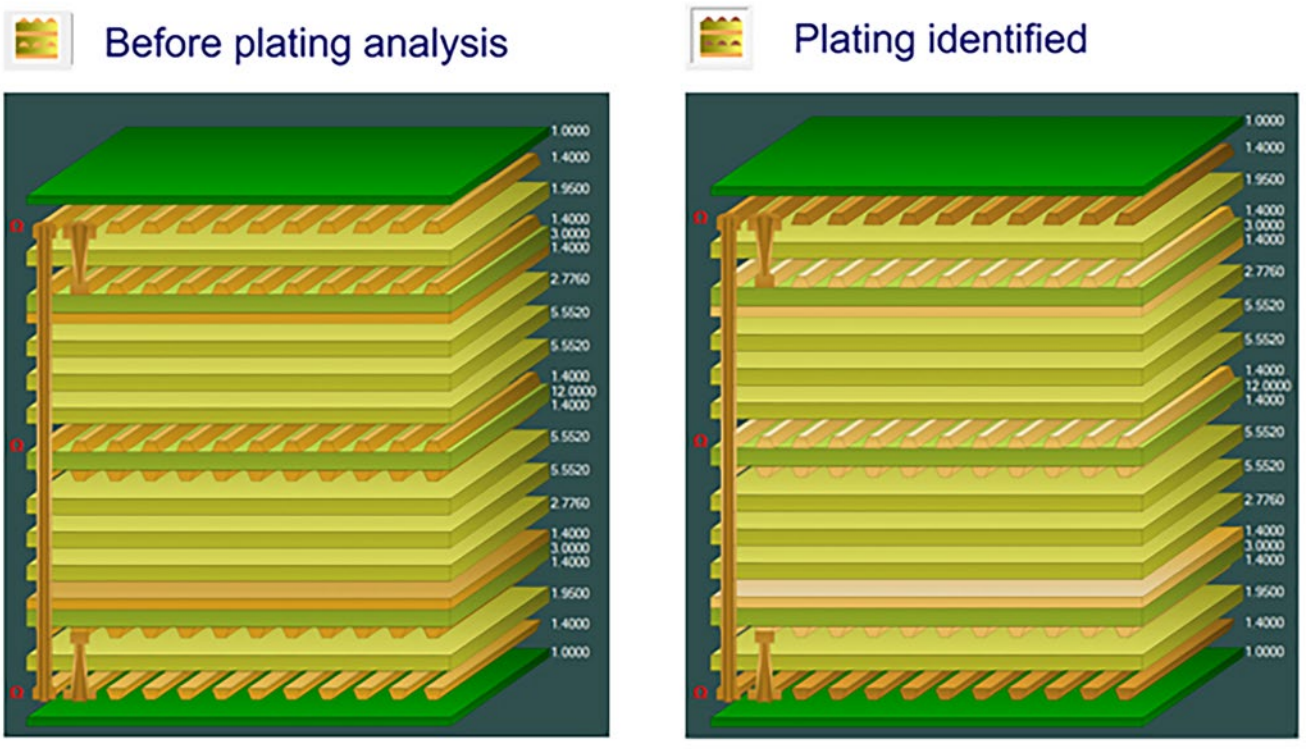

Figure 4: Traditional glass cloth/epoxy resin weave. (Source: Ventec International Group)

traditional open weave glass can yield signal integrity benefits as the transmission line runs in a "more" homogeneous medium. But you need to keep in mind the mechanical and fluid flow considerations, as the flat glass—while better for laser drilling and signal integrity— provides a barrier to resin flow across the reinforcement, so you need to ensure adequate resin content to avoid glass stop, or delamination.

Copper Characteristics

Moving from the dielectric medium to the copper plane and signal layers, new designers will often think they can use datasheet values for copper roughness. This is an understandable position if they don't have a knowledge of the PCB fabrication process, but a glance at Figure 4 shows that the PCB fabrication process adds plated copper to the surfaces

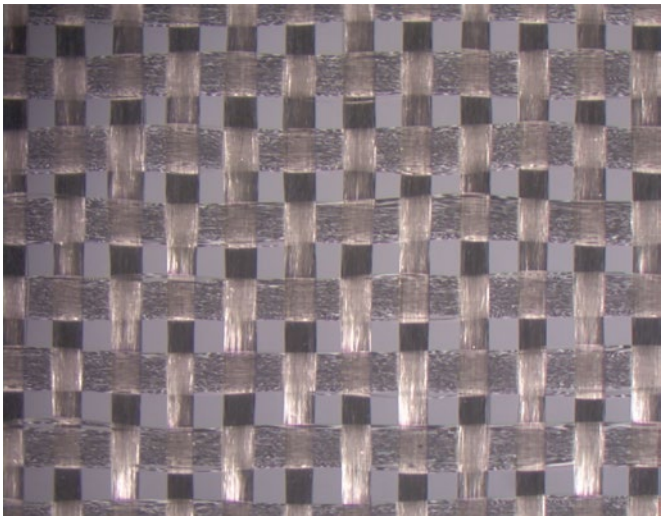

Figure 5: Traditional glass cloth/epoxy resin weave. (Courtesy of Ventec International Group)

Figure 6: Flattened glass cloth/epoxy resin weave. (Courtesy of Ventec International Group)

containing the drill ends to connect the vias in the PTH process. Therefore, the roughness needed for simulation is that of the plated layer and not of the base material. Simulation can only be as good as the input data fed to the simulator. The data does exist, but it is the job of the designer to know where to look, and when to take that data from a material data sheet, and when it needs to come from the fabricator.

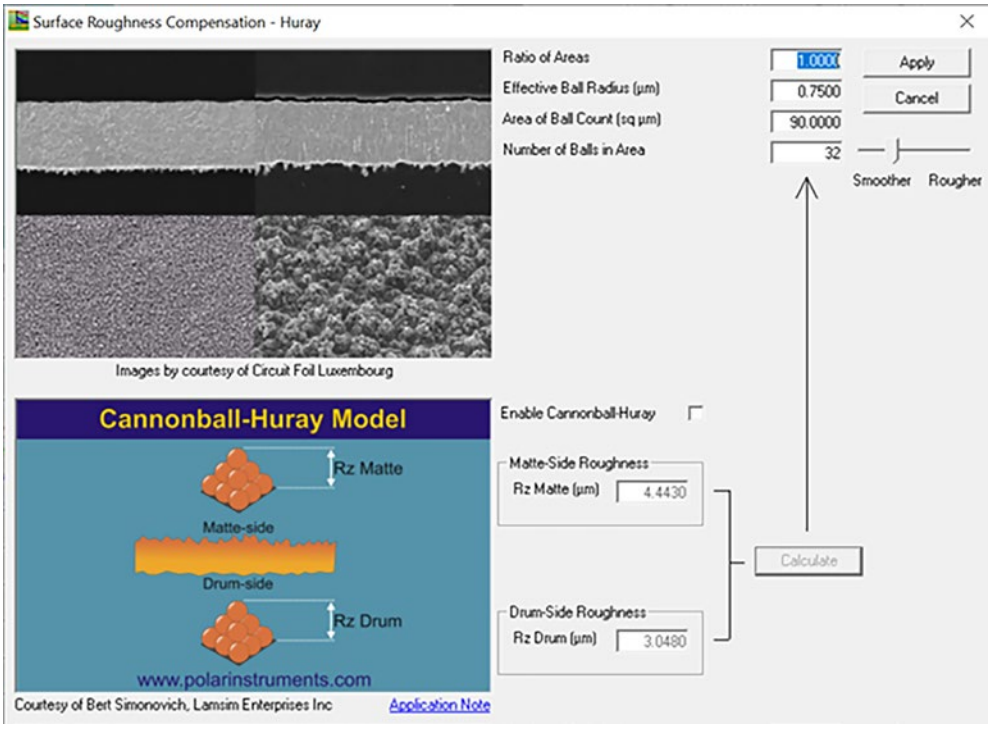

Figure 7: Modeling roughness with SEM or Cannonball model.

Once the correct input data is available, then even the roughness may be fed into the simulator and the effects on signal integrity modelled with ease.

Figure 7 presents the classic modelling and simulation dilemma. The Huray model is an excellent way of predicting the effect of copper roughness on signal losses along a transmission line, something which is inherently challenging. However, to "feed" the Huray model with good input data requires an SEM image of the finished plated or unplated copper surface. Not everyone has a scanning electron microscope on hand, and so a compromise in estimating the parameters is needed for day to day as opposed to laboratory use. Fortunately, Bert Simonovich of Lamsim Enterprises has provided a method which translates the matte and drum side roughness into Huray input parameters which are "good enough" to make a very usable model for predicting roughness impacted insertion loss.

Simulation Models

Whenever simulating, keep in mind the words of Polar's favourite eminent British statistician, George Edward Pelham, "All models are wrong—but some are useful." This is a piece of advice that engineers and fabricators need to take to heart; while the mathematical models we use for modelling save time, make better product, and increase yields, we only get the best from them by applying them with a good understanding of the input data and the limitations of the base materials used, and the manufacturing processes of pressing, plating, curing, and chemical adhesion promotion treatments applied to the finished article. **DESIGN007**

References

1. *The Works of Isambard Kingdom Brunel,* edited by Sir Alfred Pugsley, Institute of Civil Engineers, London/University of Bristol.

Martyn Gaudion is managing director of Polar Instruments Ltd. To read past columns or contact Gaudion, click here.

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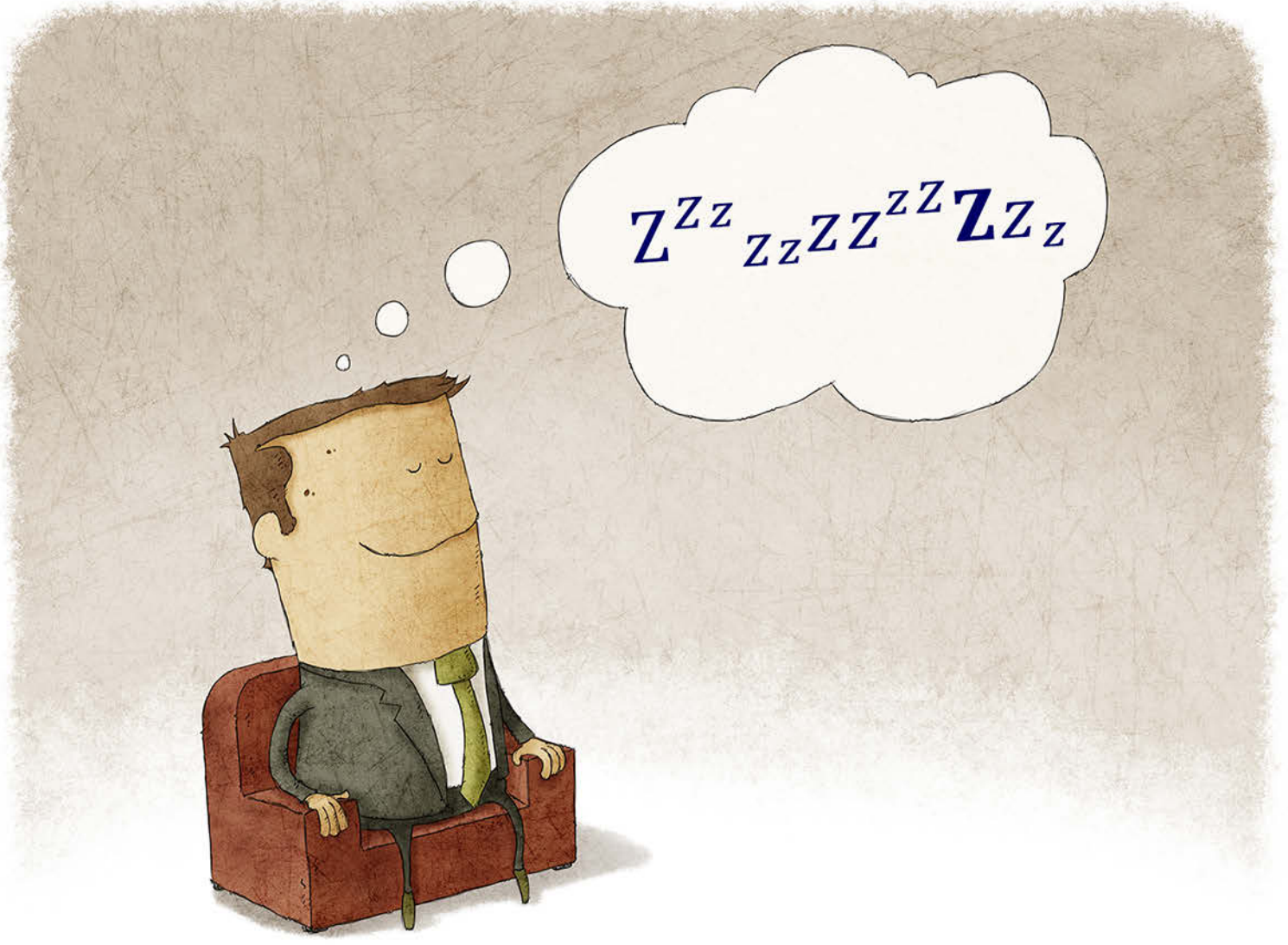

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Back-to-Back Chapter Meetings and More

The Digital Layout

by Kelly Dack, CIT, CID+, PCEA

Introduction

In this month's column, I extend an overview of two recent PCEA chapter meetings and give a nod to the presenters who gave of their time to cover some very interesting and relevant topics. Next, I hand it off to our PCEA Chairman Stephen Chavez who relates a recent, personal career "crossroads" experience and shares what gave him the hope and confidence to carry on. This month, I conclude with a growing list of upcoming events in 2021.

PCEA Updates

The Michigan Chapter held a highly anticipated kickoff meeting on February 24. Chapter chairman Dugan Karnazes welcomed an international, online audience to the meeting and spoke about their excitement and anticipation of bringing local area printed circuit engineers together to fellowship and learn with a wider audience. The featured speaker was Terry Munson, owner of Forsite Inc., whose topic was "The Forensics of Dendrite Shorting." Terry outlined Forsite's definition of cleanliness, described no less than 16 sources of contamination which can cause dendritic shorting on PCBAs, and offered mitigation techniques.

Attendees were captivated by the presentation (Figure 1), which included explanations for a variety of PCB residue factors and

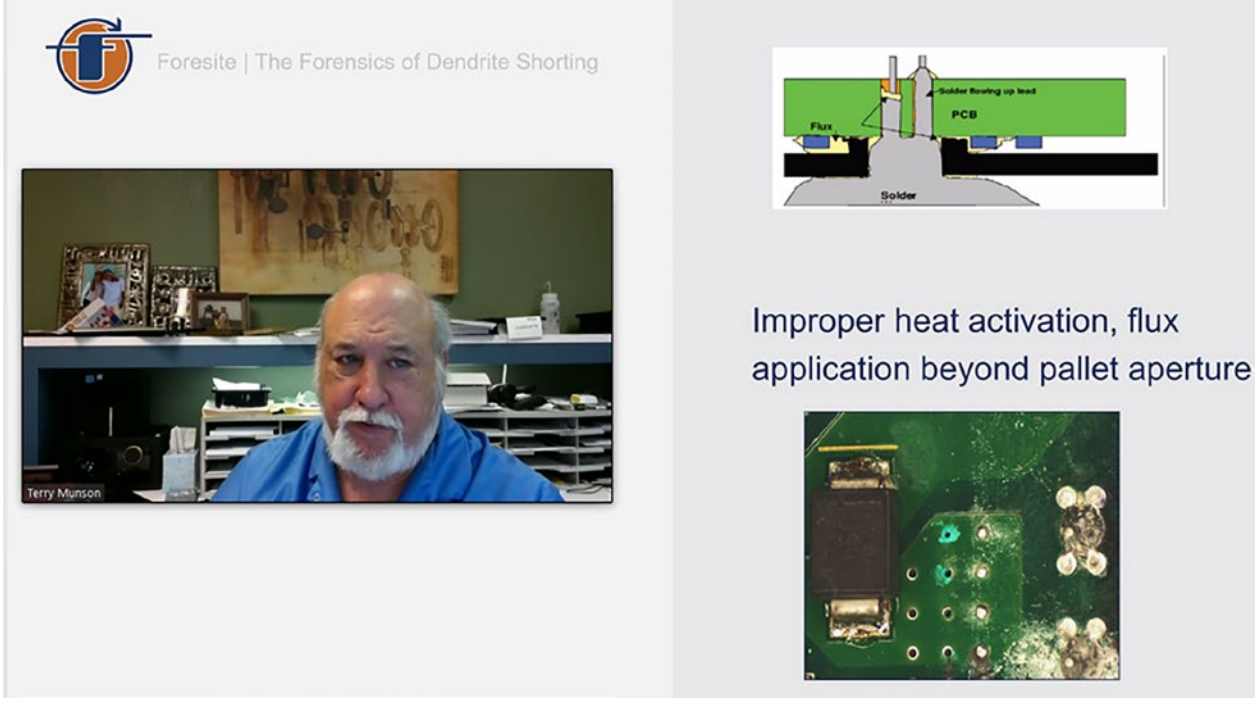

Figure 1: Images from a presentation by Terry Munson at the Michigan Chapter meeting.


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Figure 2: Joe Bevan, Insulectro product manager of lamination.

sources which can contribute to the underlying causes for failure. Process malefactors include a disregard for bare board and component cleanliness, incomplete heat-activation of no-clean fluxes, poor cleaning system performance, flux and/or cleaning agent entrapment under low standoff component packages, and outside contamination. There were many follow-up questions, which validated the interest in his topic. The meeting concluded with a raffle for $200 in prizes from our generous PCEA sponsors.

The Silicon Valley Chapter hosted an online meeting February 25, featuring Joe Bevan, product manager of lamination for Insulectro, who spoke on PCB materials and their applications. Chapter chairman Bob McCreight welcomed the attendees to the "crowded" Zoom presentation meeting hall, gave a brief history of the long-standing Silicon Valley Chapter, and then introduced the speaker. Joe was supported by PCEA's own Mike Creeden, director of education for Insulectro, to queue up and relay the many questions which streamed in during the presentation. Joe covered many valuable topics including an overview of copper foil categories, production methods, the mSAP process, and a discussion on the rewriting of IPC-4562 Metal Foil for Printed Board Applications.

During the business portions of these back-to-back meetings, Chairman Stephen Chavez showcased two new PCEA chapters, both of which had leaders attending the meetings: Luis Saracho, chairman of the Monterrey, Mexico Chapter, and Zachariah Peterson, who recently started the Portland, Oregon Chapter.

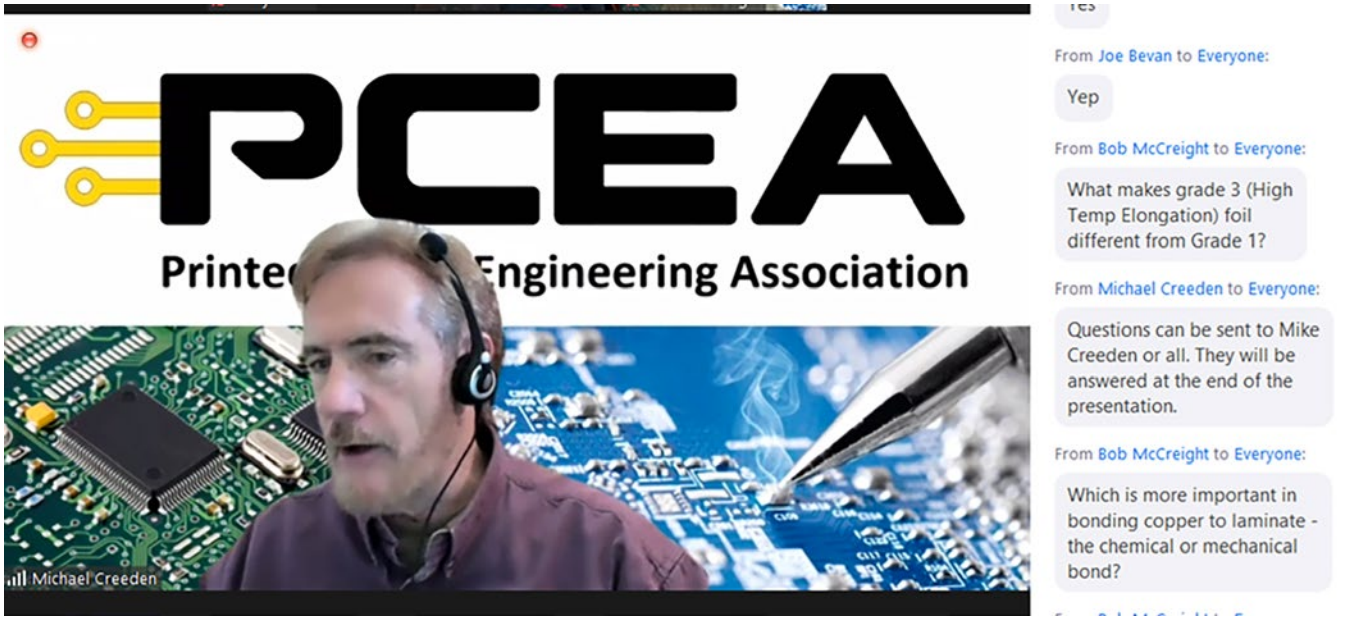

Figure 3: Mike Creeden, director of education at Insulectro.

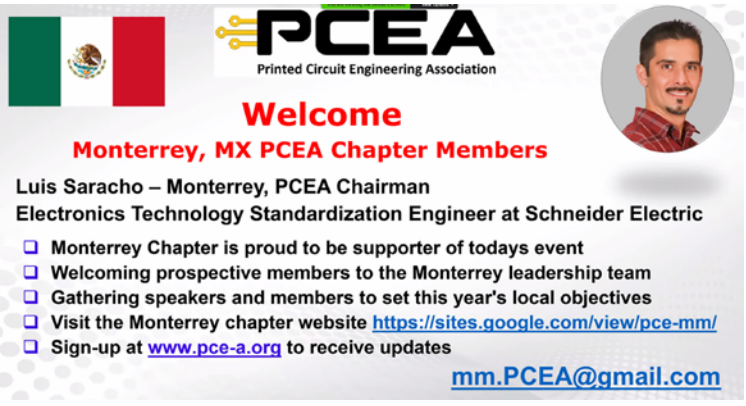

Figure 4: An overview of the Monterrey, Mexico Chapter.

Figure 5: An overview of the Portland, Oregon Chapter.

Message from the Chairman

by Stephen Chavez, MIT, CID+

This month, I reflect on the essence of PCEA and the benefits of membership within the PCEA collective. More specifically, are you experiencing the value of giving and receiving as a PCEA member? I want to share a recent experience of mine that I think many of you can relate to. It spotlights the true value of PCEA membership.

"Collaborate, Educate, and Inspire" is the core mission of PCEA. As we come off a tough year for our industry, 2021 has many companies adjusting, adapting, and making tough decisions about how to survive, move forward, and be successful. This calls for changes that may potentially be either good or bad, depending on what side of the decision you fall on.

Like most of you, I have a day job. I bring my A-game every time I strap into my "cockpit" here in my office, where I conduct business as a printed circuit engineer. I am always confident and have no hesitation when wielding my CAD system to either design complex PCB circuits solo or while integrating and collaborating with global engineering teams. My 30+ years of industry experience provides me with a certain level of confidence, allowing me to walk with a swagger. Yet, I am not invincible by any means! I'm not impervious to changes or tough decisions that are beyond my control.

Recently, I found myself contemplating the direction of my future and I needed to make decisions which could seriously impact the trajectory of my career path—each option had its potential pros and cons, which made the decisions even more difficult. I am sure many of you can relate to what I am talking about. If you're early in your career and have not yet experienced this, you will at some point come to a crossroads in your career. I know many industry veterans would agree.

As I evaluated my situation and contemplated my options, hoping I was seeing things from every angle, I realized that, even with all my experience, I could benefit from advice and a support network where I could discuss ideas and seek advice from others like me. So, what did I do? I tapped into my immediate PCEA network, which consisted of many industry veterans and professionals who have been at these similar crossroads. As I worked the situation alongside my established network, I realized they have become lifelong, personal friends as well. They provided solid advice as we worked the problem together. You see, I was not alone! More importantly, I had the horsepower of the PCEA collective there to support me. The core PCEA mission was in full effect: collaborate, educate, and inspire. I was

collaborating with other members to work the situation. I was being educated by members who have been at these crossroads before and could provide solid advice. Lastly, I was being inspired by my longtime mentors who were counseling me, while at the same time I was inspiring others around me on how I handled myself and how I was addressing the situation as an industry professional.

The best thing about this level of support was having others reach out and put me at ease; I knew I had a safety net through PCEA to rely on.

You may be in a similar situation, in one form or another. Some have no idea what to do or which direction to go in; even worse, they might not have anyone to reach out to for advice. But when I think about what I just went through, as well as the early years of my career coming out of the Marine Corps in 1995 with no civilian industry experience and no support network to tap into, I had no choice but to go down the road of "hard knocks." That was a tough and long road indeed, and I know many of you can relate to this.

Many of us coming out of the military or college, or who are industry veterans like myself, may be facing similar crossroads in their careers. Knowing what I know now and knowing what PCEA offers as an industry association is simply awesome! The three words in our mission statement say it all, and I am very happy PCEA exists today. I wish I had had something like PCEA early on in my career path. I hope that those who have not yet become a PCEA member will join us and tap into this tremendous professional trade association. For our current members, please take advantage of the PCEA collective, join a chapter for awesome professional development, and gain great professional networking.

Refer to our column and the PCEA website to stay up to date on industry events. There are a lot of free webinars being offered, so take advantage of these opportunities. If you have not yet joined the PCEA collective, please visit pce-a.org for details on becoming a PCEA member.

I wish health and safety to you and your families. Best of success to all as 2021 continues to unfold.

Warmest Regards,

Steph

Next Month

How do you hone your printed circuit engineering skills? Are your skills measurable? The PCEA has much in store for our readers regarding career training and certification that you will not want to miss.

Upcoming Events

Below is a newly seeded list of upcoming events which is sure to get you excited about travelling again. We must each do our best to follow CDC guidelines and take the precautionary measures—including hand-washing, masking and vaccination as possible—to squash the spread of COVID-19 and its variants. We're still in this together!

Nepcon China
April 21–23, 2021
Shanghai, China

(Canceled) SMTConnect 2021
May 4-6, 2021
Nuremberg, Germany

(Canceled) IPC High Reliability Forum
May 11–13, 2021
Baltimore, MD

PCB East 2021
June 15–17, 2021
Marlborough, MA

Zuken Innovation World 2021 (Virtual)
August 4-5, 2021

DesignCon 2021
August 16–18, 2021
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SMTA International 2021
Nov. 1–4, 2021
Minneapolis, MN

Productronica
Nov. 16–19, 2021
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PCB Carolina 2021
Nov. 10, 2021
Raleigh, NC

Del Mar Electronics & Manufacturing Show
May 4–5, 2022
Del Mar Fairgrounds, San Diego, CA

Spread the word. If you have a significant electronics industry event that you would like to announce, please send the details to kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Conclusion

Sometimes we can find ourselves at the crossroads of several career unknowns. During these times, we need comfort and confidence that things will work out regardless of which path is followed. Thankfully, we have various opportunities to join a network of peers who can help us pivot if the road begins to spiral downward. Belonging to any or many of the electronics industry's meaningful trade organizations can help us to chart our paths onto the high road for success through communication and collaboration, which can lead to opportunities to be educated, then to educate—to be inspired and then to inspire.

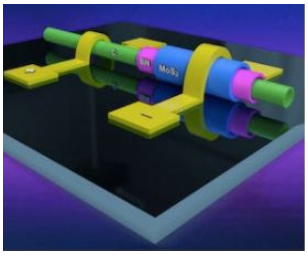
See you next month or sooner! **DESIGN007**

Kelly Dack, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). To read past columns or contact Dack, click here.

Sushi-like Rolled 2D Heterostructures May Lead to New Miniaturized Electronics

The recent synthesis of one-dimensional van der Waals heterostructures, a type of heterostructure made by layering two-dimensional materials that are one atom thick, may lead to new, miniaturized electronics that are currently not possible, according to a team of Penn State and University of Tokyo researchers.

Engineers commonly produce heterostructures to achieve new device properties that are not available in a single material. A van der Waals heterostructure is one made of 2D materials that are stacked directly on top of each other like Lego-blocks or a sandwich. The van der Waals force, which is an attractive force between uncharged molecules or atoms, holds the materials together.



The team's research, published in ACS Nano, suggests that all 2D materials could be rolled into these one-dimensional heterostructure cylinders, known as hetero-nanotubes. The University of Tokyo researchers recently fabricated electrodes on a hetero-nanotube and demonstrated that it can work as an extremely small diode with high performance despite its size.

"Diodes are a major type of device used in optoelectronics — they are in the core of photodetectors, solar cells, light emitting devices, etc.," Rotkin said. "In electronics, diodes are used in several specialized circuits; although the main element of electronics is a transistor, two diodes, connected back-to-back, may serve as a switch, too."

This opens a potential new class of materials for miniaturized electronics.

"It brings device technology of 2D materials to a new level, potentially enabling a new generation of both electronic and optoelectronic devices," Rotkin said.

Rotkin's contribution to the project was to solve a particularly challenging task, which was ensuring that they were able to make the one-dimensional van der Waals heterostructure cylinder have all the required material layers.

(Source: Pennsylvania State University)

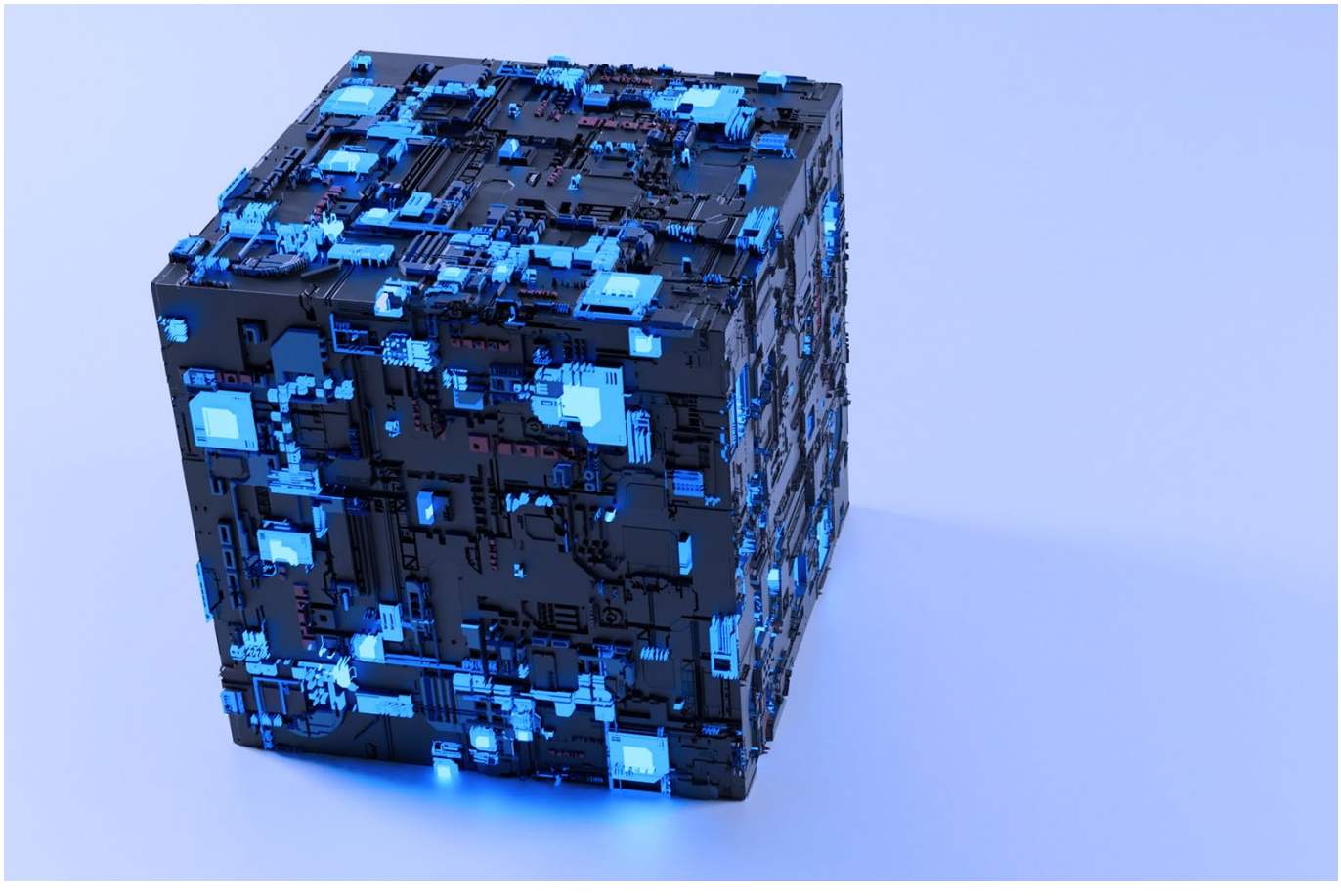
Additive Electronics—
Next Generation PCB Capabilities

PCB Talk

by Tara Dunn, AVERATEK

Exciting news! This column marks the launch of a series of columns diving into semi-additive PCB (SAP) manufacturing processes. We will explore topics ranging from SWaP (space, weight, and packaging) benefits, signal integrity benefits, materials characterization, reliability testing, and even the search to find a calculator that is compatible with straight conductor sidewalls and line width and space at 1.0 mil and below.

Although more people are becoming familiar with the term SAP, specifically as it relates to PCB manufacturing, this technology is new to most people. It seems that mSAP (modified semi-additive processes) make headlines for enabling volume consumer applications such as our smartphones, to be produced with roughly 35-micron feature sizes. Yet we have not heard a lot about semi-additive PCB processes for applications outside of this specific market.



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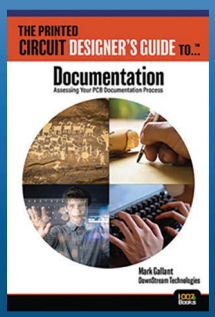

This book, written by Mark Gallant of DownStream Technologies, explains how an automated documentation solution like BluePrint-PCB® can eliminate post-processing errors and speed up time to market.

This book is a must-read for any PCB designers or design engineers who would like to adopt 21st-century PCB documentation processes.

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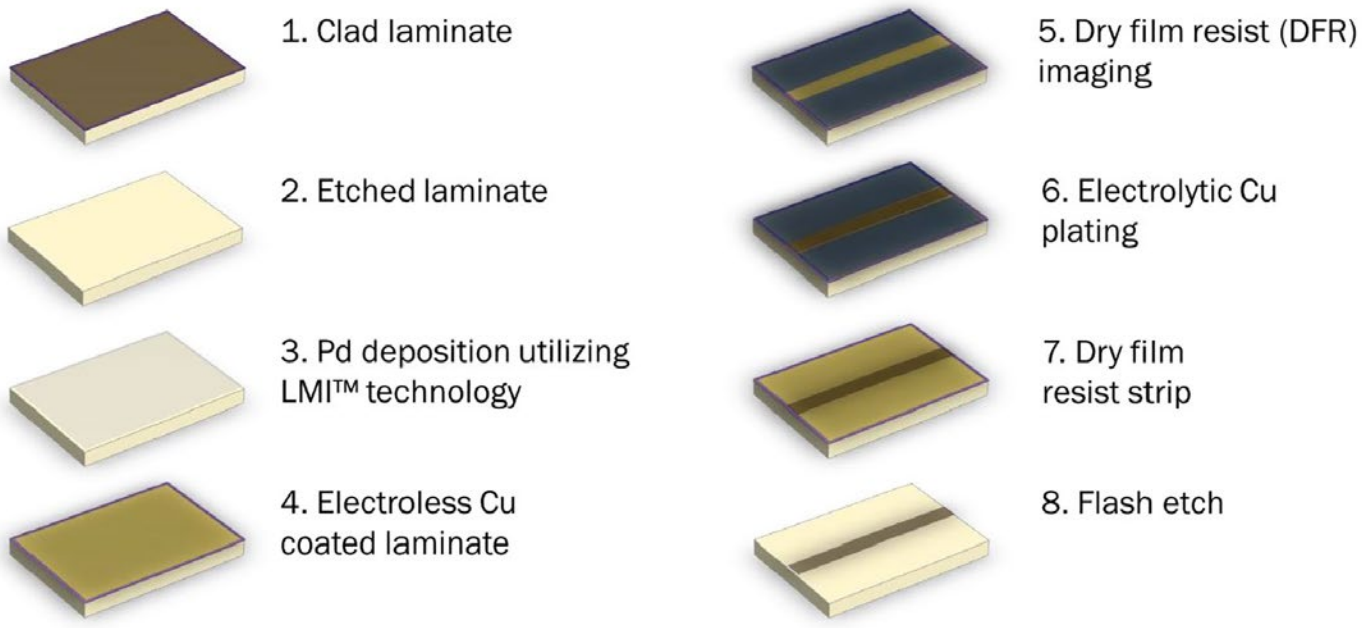

Figure 1: A-SAP™ process flow diagram.

The really exciting news is that there are now a handful of U.S.-based fabricators offering this technology for low volume/high mix applications. This opens so many new opportunities previously unavailable for PCB designers and at the same time generates a myriad of questions from the design community as well as the fabrication community. Before we dive in and start addressing these questions, let's step back and discuss the semi-additive PCB process flow and how that is being integrated into existing subtractive etch PCB processing lines.

Semi-Additive PCB Process

This process flow from Averatek (Figure 1) gives a simplistic view of the semi-additive PCB process flow. I do not want to assume that all are familiar with the subtractive etch process and want to point out that with steps two and three, these are the same process steps used to manufacture with traditional processes. Rather than etching away the copper that is not required for the circuitry, with this process, all copper is etched from the manufacturing panel. From there, a palladium deposition using LMI™ technology is coated on the panel. The next step is electroless copper, typically the same electroless chemistry being used by the fabricator for the subtractive process.

This step is critical to understanding the benefits of the semi-additive process. The thin LMI coating enables a very thin, conformal layer of electroless copper, 4–20 µin, which is much thinner than typical electroless copper plating. More to come on the significance of this.

Following electroless copper, panels move to dry film resist imaging, followed by electrolytic copper and dry film resist strip, all standard manufacturing processes. The final step in the circuit creation process is to flash-etch the electroless copper layer. Circling back to the thickness (or actually, thinness) of that electroless copper layer, it is important to point out that the flash-etch of the very thin electroless copper layer has very little impact on the trace itself. Etching of thicker copper results in the trapezoidal effect that we are all aware of. With semi-additive processing, the trace sidewalls remain straight, and the line width tolerance is tighter. In future columns we will discuss the impact of this on impedance control.

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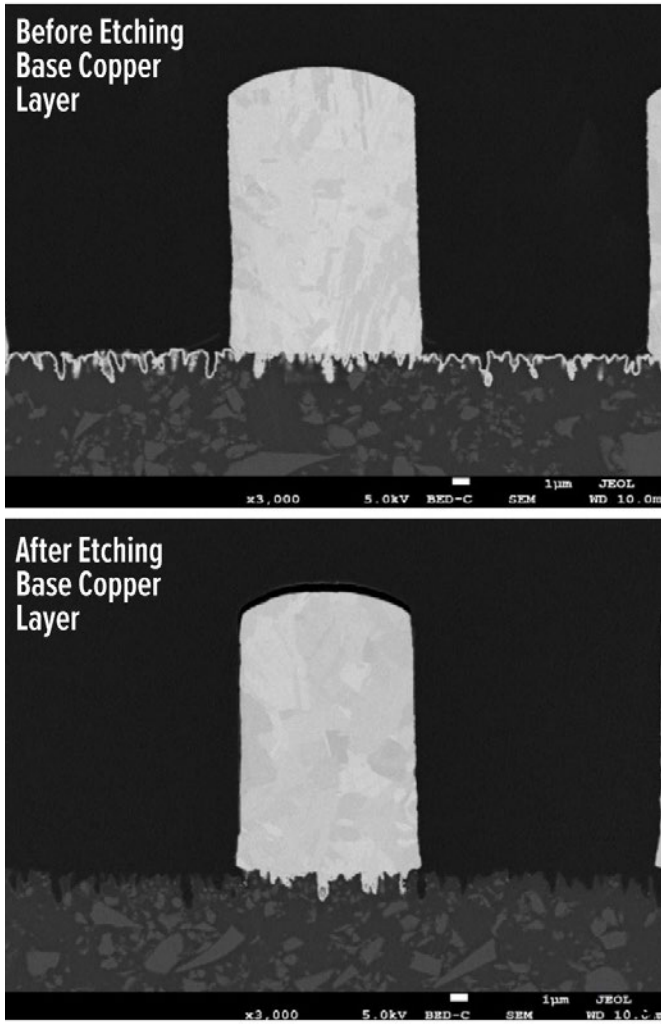

Figure 2: Before and after etching the base copper layer. (Images courtesy of MEC Corporation)

Following these wet process steps, the semi-additive manufacturing panels will follow the same process flow that subtractive etch panels follow including solder mask, surface finish plating, electrical test, and inspection.

Why Is This Important to PCB Design?

Traditional subtractive etch processing, at least in the U.S., becomes very difficult for feature sizes below 3 mils (75 microns). As electronics packages shrink, this forces PCB designs to become much more complex—adding extra routing layers, adding microvia layers, and increasing lamination cycles required, all which impact yield, reliability, and cost.

The semi-additive process jumps this technology curve. Within a few weeks, fabricators previously able to offer 3-mil line/space, can now offer 1-mil line/space and below. That is a complete game changer for PCB design. Some of the benefits are easily seen:

- The ability to shrink the overall size of a circuit
- The ability to route additional traces between pads can reduce the overall number of layers required for a design and subsequently the ability to reduce the number of stacked or staggered microvias

Over the next few months, we will review use cases to help spur ideas.

There are also significant signal integrity benefits from semi-additive processing. There is tighter line width control and straight conductor sidewalls greatly improve impedance control. Another feature to additive processing creating a buzz within the design community is the ability to create higher aspect ratio traces than available with subtractive etch or even mSAP options.

We are just scratching the surface on how to best apply these new capabilities to PCB design, and I am looking forward to collaborative discussion and creativity. It is tempting to ask for "design rules" but in my opinion, that may limit the creativity in approaching design challenges in a new way and my hope is that we can develop a community of interest followed by a community of design expertise around this new technology. Please reach out to me with your questions and stay tuned as we start a deeper dive into this exciting technology. **DESIGN007**

Tara Dunn is the vice president of marketing and business development for Averatek. To read past columns or contact Dunn, click here.

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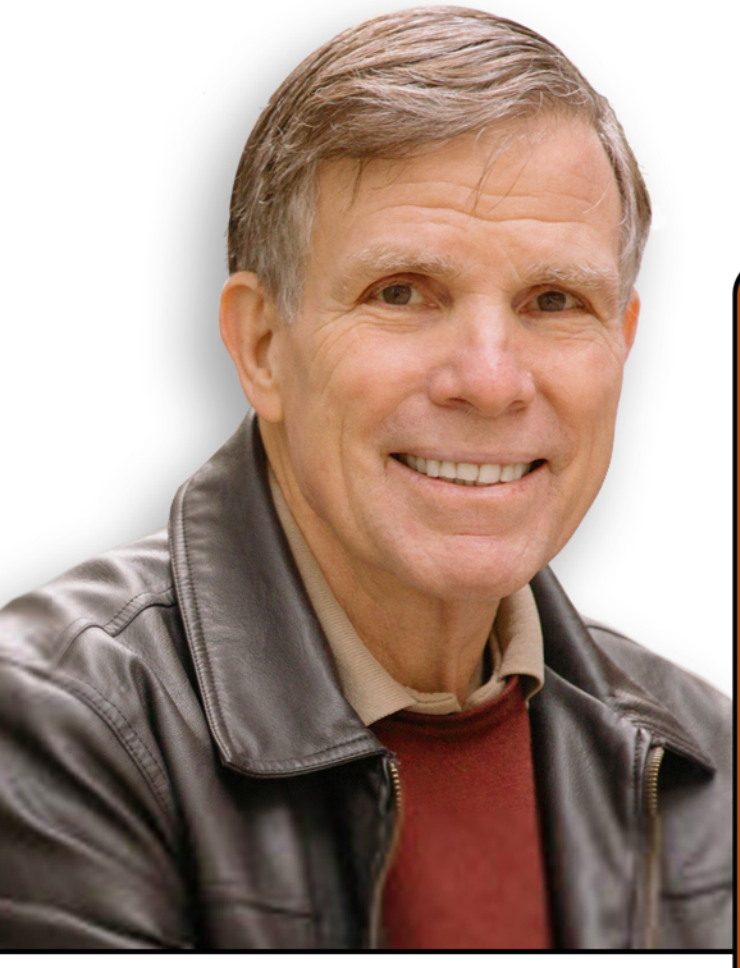

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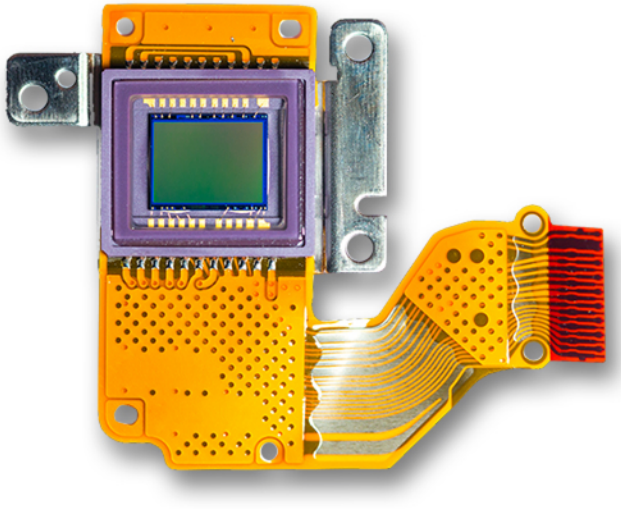

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Consider This

by John Talbot, TRAMONTO CIRCUITS

There are many possible connectors that are manufactured specifically for use with flexible circuits to connect from a flex circuit to a rigid PCB. Many use typical, military secure twist connectors which require reinforcement of the flex to solder to the connector pins (Figure 1). Also, a good choice is zero insertion force (ZIF) connectors for thin flex to rigid applications. Additionally, pierce type connectors are used (Figure 2). Direct copper fingers which plug into rigid header connectors can be used (Figure 3).

Many different types of connectors offer inexpensive and reliable methods to connect a flexible circuit to a rigid PCB. Consideration for flexibility always needs to be addressed. Examine the bend radius and possibly add cover coat reinforcement in higher stress areas. Almost any connector that can be utilized on a rigid PCB can also be installed on a flexible

Figure 1: Reinforced flex for soldering to military connector.

Figure 2: Pierce type connector for flex to rigid header.

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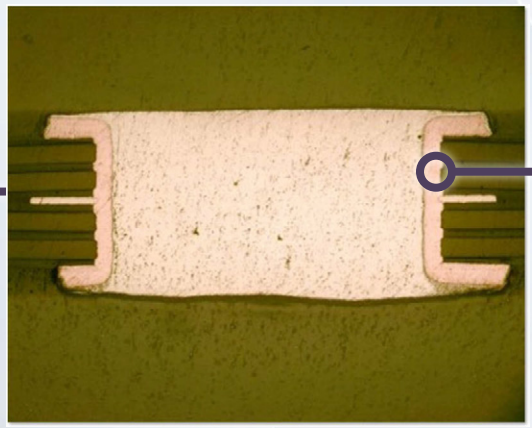

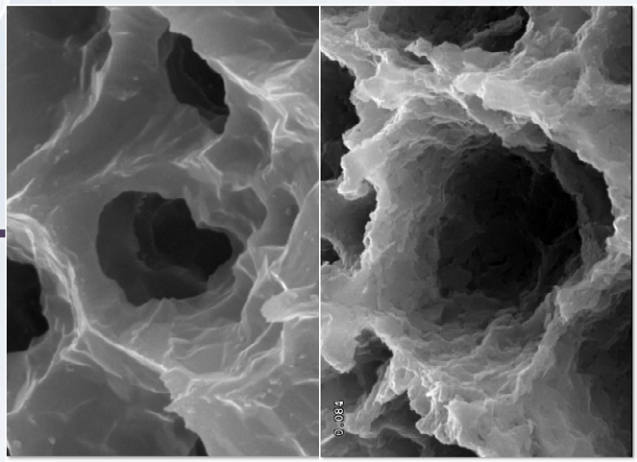

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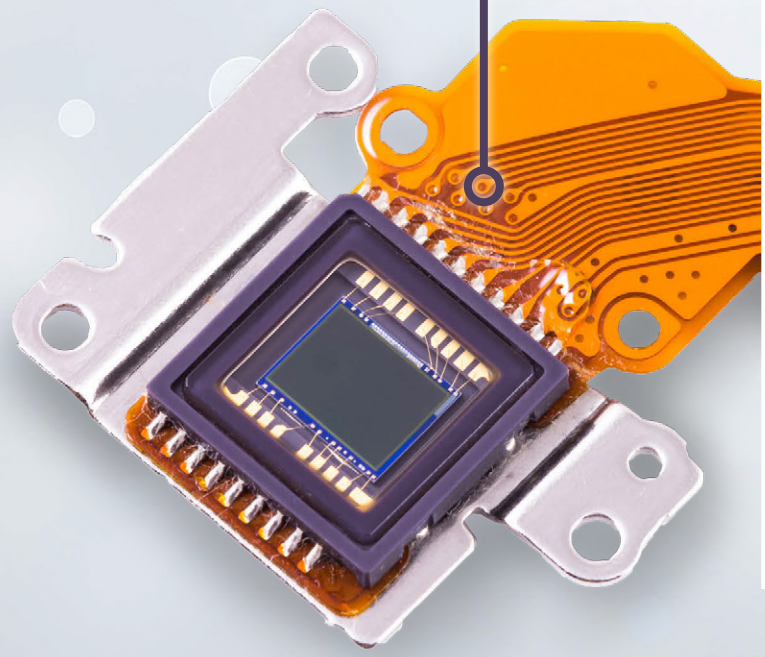

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Figure 3: Finger flex connector for insertion into connector on rigid PCB.

circuit. Using a through-hole style connector (Figure 1), the flexible circuit should have reinforcement in the connector area with either a FR-4 stiffener or a cover coat on the same side as the connector. However, when using an SMT type connector, a higher, stiffness reinforcement, such as thin FR-4, should be laminated to the opposite side of the flex circuit, away from the solder side.

There are many ways to terminate and connect flexible circuits to a rigid PCB. The most widely used technologies fall into four main categories: reinforced male finger contacts, unreinforced male finger contacts, standard through-hole and surface mount PCB connectors, and insulation displacement connectors. Unreinforced fingers are typically an extension of the copper traces with the insulation removed or thicker metallic fingers that are attached to the circuit traces. The copper fingers can be bent for angled installation or remain straight for a vertical installation. Depending on the size and copper weight of the copper fingers and clamping force of the connector, a secondary support method is suggested. Consider using a mechanical clamp-down to limit bending at the connector. As in all flex applications, bend radius and flexibility must be considered to ensure the copper traces are not bent, exceeding the crack radius or number of bend cycles.

The use of flex suggests that the connection may at some point be under stress. That stress must be accounted for, as failure to limit the bending will result in a stress concentration point between the connector frame on the rigid PCB and the flex circuit, resulting in intermittent or broken connections. Unreinforced fingers are typically used in applications which use the method of soldering the fingers directly into a plated through-hole or onto a pad. Unreinforced fingers are often used with a hot-bar soldering process to eliminate the need for a connector.

Reinforced copper, gold plated fingers are most used in ZIF or low insertion force (LIF) connector applications. When using reinforced fingers in a ZIF connector application, it is required to specify imperative circuit features on the drawing. Critical items, such as overall thickness in the finger areas, as well as circuit edge-to-finger tolerance is important as the flex must mate correctly with the narrow fingers in the connector. When the flex circuit is designed and manufactured properly, ZIF connectors can be an inexpensive and reliable option. An additional method for flex or silver-screened membrane to a rigid connection is through anisotropic Z-axis, conductive adhesive bonded directly to rigid PCB traces.

Insulation displacement connectors use barbs to pierce through the cover insulation and make contact with the copper conductor below (Figure 2). Many times, the bent-over barbs are soldered to the flex traces to improve reliability. Insulation displacement connectors are not as popular these days, moving more to standard through-hole and SMT connections.

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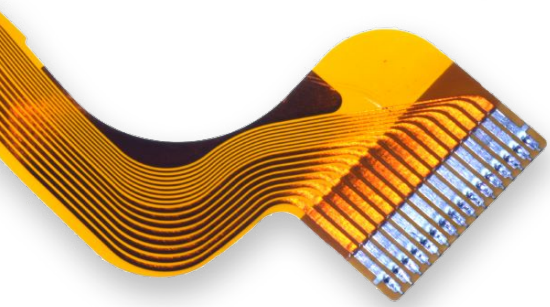

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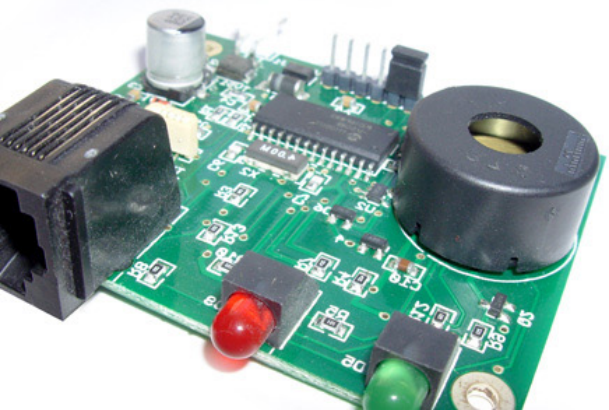

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PCB connectors utilizing through-hole and SMT connection methods are the most common and lowest cost method of connecting a flex circuit. By utilizing the more common varieties such as D-sub or micro-D, you can save money and be assured of a constant supply. You can design or use a custom PCB connector for your flexible circuitry. However, keep in mind custom connectors will probably be very expensive, with long lead times. Having a single supplier for a flex connector can prove to be fatal. The lead times on having a custom designed connector manufactured can be quite long, with two to four months being typical.

As experience has taught, many various connectors can have unexpected and exceedingly long lead times. It is always wise to check suppliers for alternative connectors and lead times. Many times connector designs change quickly. One should check whether the particular connector is stocked by other suppliers or if supply is limited because the connector has limited sales.

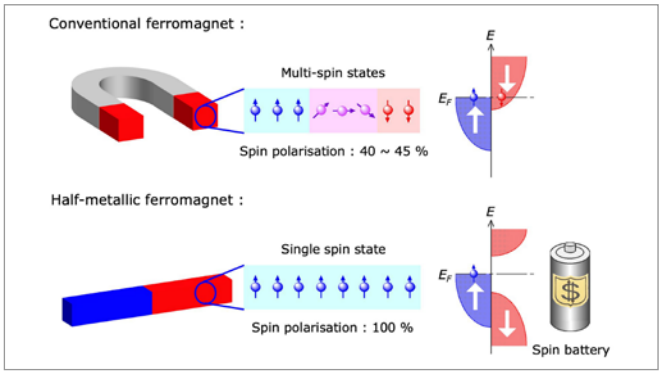
Typically in almost every design of a product, the flex circuit is the last part to be examined and designed into the system. It is not uncommon to hear stories that designers just thought of flex as an off-the-shelf item, as it is such a nondescript part. Many of the connector termination choices would have already been confirmed using typical rigid PCB connectors before the flex is even designed. To prevent future problems in assembly and parts procurement, it is vital to begin the design by locking down the interconnect technology that you plan to use. You need to roughly design the flex interconnection circuits, define the connectors, and look at stress and flexibility which all play an important part in the early design process. This is the time to define and set quality and reliability parameters. Whatever method you choose, your flex circuit provider can guide you in the selection process. **FLEX007**

John Talbot is president of Tramonto Circuits. To read past columns or contact Talbot, click here.

Putting a Spin on Heusler Alloys

A study published in the journal Science and Technology of Advanced Materials summarizes the major achievements made to-date in Heusler alloy research. "Our review article can serve as an ideal reference for researchers in magnetic materials," says Atsufumi Hirohata of the University of York, UK, who specializes in spintronics.

A category of materials showing great promise in this area is Heusler alloys: materials formed of one or two parts metal X, one part metal Y, and one part metal Z, each coming from a distinct part of the periodic table of elements. Over the last few decades, scientists have been working on approaches to grow Heusler alloy films at room temperature on special substrates with crystal lattices that are similar to the alloy's. The interaction between the two lattices can lead to the development of half-metallicity in the Heusler alloy.



Researchers need to be able to measure the properties of materials in order to conduct their investigations. The atomic structure of Heusler alloys can be directly observed by X-ray diffraction and indirectly measured through examining the relationship between the material's resistance to an electric current and temperature changes. Other techniques are also available for measuring their magnetic properties. (Source: ACN Newswire)

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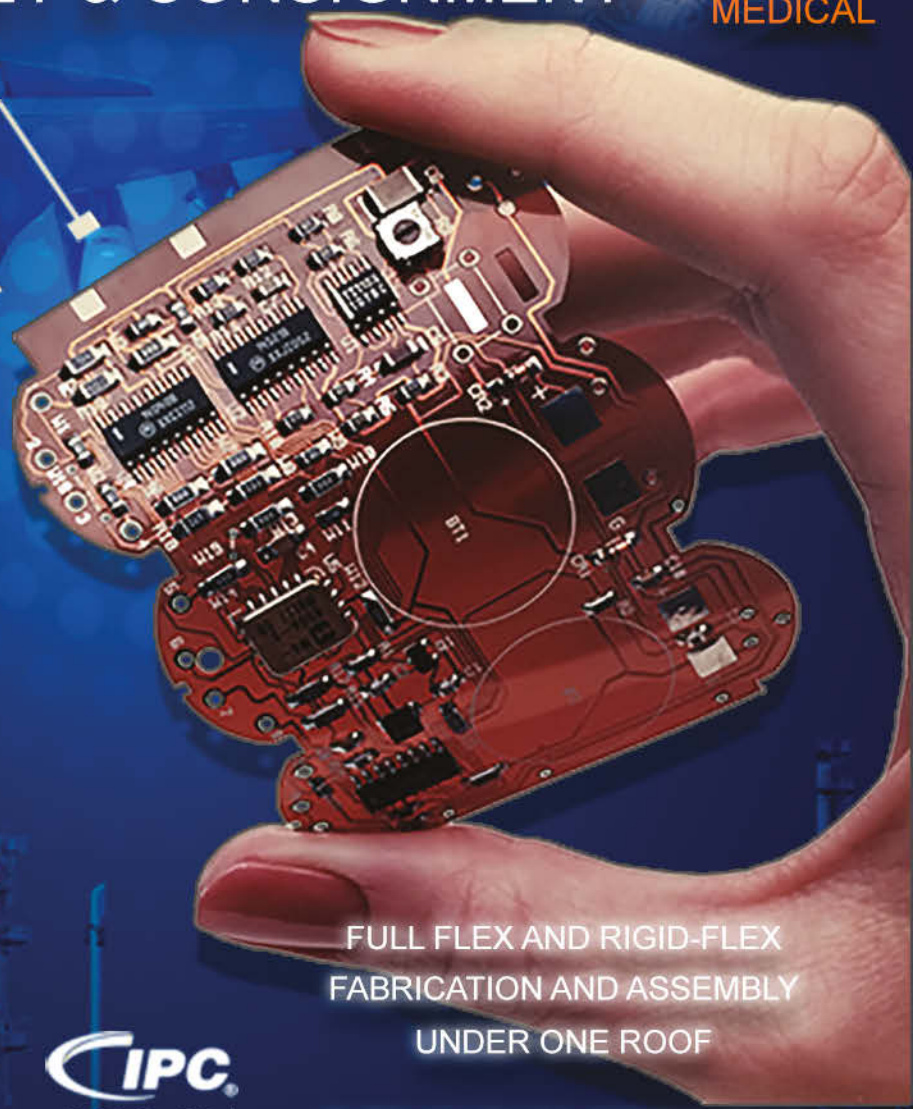

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Flex007 Highlights

2020: A Year of Learning, Innovation for Taiyo America ▸

Pete Starkey has a virtual visit with John Fix, director of sales and marketing at Taiyo America, where they discuss the changes taking place because of COVID-19 restrictions, and some of the new products Taiyo will be presenting at this year's IPC APEX EXPO.

Lenthor Engineering Announces Year End 2020 Financial Results ▸

Lenthor Engineering, Inc., a California based designer, manufacturer and assembler of flex and rigid-flex printed circuit boards, announces its 2020 year-end financial results.

Eltek Secures Grant from Israel Investment Authority ▸

Eltek Ltd. provided an update regarding its award of a grant from the Israeli Investment Authority that will fund 15% of Eltek's expected $1.5 million investment in Advanced Manufacturing Equipment fit to Industry 4.0 standards, which focuses on interconnectivity, automation, machine learning, and real-time data.

Taiflex February 2021 Revenues Up 54% ▸

Taiflex Scientific Co. Ltd, a Taiwan-based manufacturer of flexible PCB materials such as flexible copper clad laminates (CCLs), coverlay, and bonding sheets, has announced that consolidated revenue for February 2021 totaled NT$680 million ($24.34 million at $1:NT$27.93), down by 9.3% from the previous month, but up by 54% year-on-year.

Flex Talk: Simplified Assembly of Aluminum Flexible Circuits ▸

Tara Dunn sits down to discuss Mina™ with Divyakant Kadiwala, vice president of manufacturing for Averatek. He has been instrumental in the development of this assembly process.

Arlon EMD Completes IPC Validation Recertification Audit ▸

Arlon Electronic Materials has successfully completed an intensive two-day recertification audit by IPC Validation Services. This audit was focused on validating Arlon's manufacturing processes and testing procedures. Arlon's success in passing IPC Validation Services' audit confirmed Arlon's status in the electronics industry as a trusted manufacturer of high-performance laminate and prepreg products.

IPC Honors Calumet Electronics Corp., GM China with Corporate Recognition Awards ▸

IPC bestowed its highest corporate honors on two IPC member companies, Calumet Electronics Corporation and General Motors (GM) China.

DownStream Focused on Rigid-Flex and Embedded Component Support ▸

Guest Editor Kelly Dack and Joe Clark, co-founder of DownStream Technologies, discuss trends in PCB design and how this has led to the company's introduction of rigid-flex design support for their tools.

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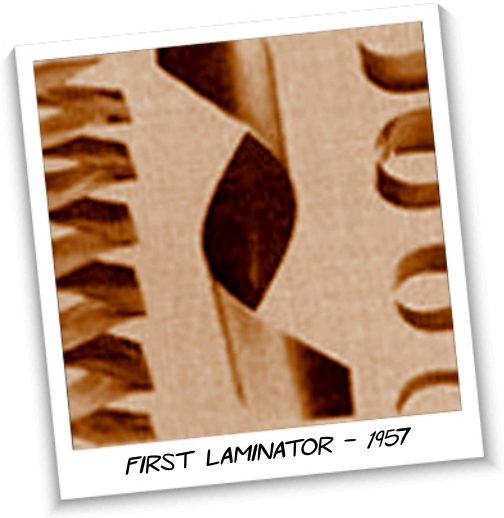

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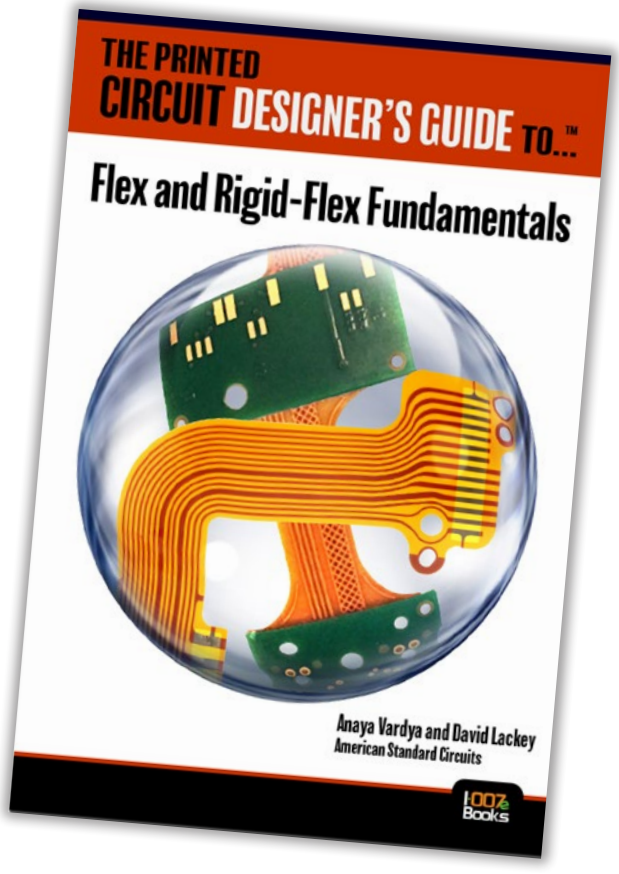


Chapter 2: Designing Flex Circuits for First-Pass Success

Article by Dave Lackey and Anaya Vardya
AMERICAN STANDARD CIRCUITS

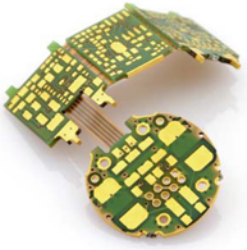
The design process is arguably the most important part of the flex circuit procurement process. The decisions made in the design process will have a lasting impact, for better or worse, throughout the manufacturing cycle. In advance of providing important details about the actual construction of the flex circuit, it is of value to provide some sort of understanding of the expected use environment for the finished product.

The electronics industry serves several different markets that do not always share the same product acceptability or reliability expectations. For this reason, the electronics industry, through IPC and other standards organizations, has developed a classification system that specifies what is expected of products for different classes. The system of classification is not intended to be a measure of quality. Rather, quality is a matter of conformance to a set of established requirements for a product in a given application. Therefore, quality products can be created in each of the classifications within the system. It is generally accepted that there are three classes of product. These have been defined by IPC standards as follows:

- **Class 1**—Consumer products and products for non-critical applications where cost is normally the primary driver.
- **Class 2**—Higher-order products in terms of quality and reliability expectations, including telecommunications, computers and general industrial.
- **Class 3**—High-reliability applications including military, aerospace, automotive, and medical products.

By defining the class of the product being designed, the purchaser is letting the manufacturer know what added controls to apply to the manufacturing process and the level of care they will need in the inspection process to

Focused on Flex



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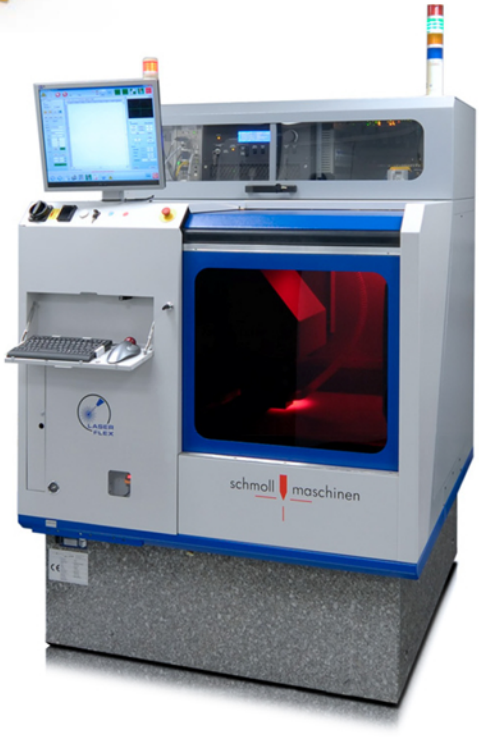

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ensure that the customer gets the product that is best suited to the application.

The following are discussions on matters of high importance to achieving first-pass success in securing quality flexible circuits from a flex circuit vendor.

It is important to provide some information about the operational requirements for the flex circuit, especially if the circuit is to be used in a dynamic flexing application, such as for a disk drive read/write head assembly. The reason for this is the circuit vendor needs to provide a plan for proper layout strategy for manufacturing; a plan which accounts for the grain direction of the copper foil during the manufacturing process. This is because there is a measurable difference in terms of flexing performance between the machine and transverse directions of the copper foil.

Fabrication Specification Details

After the basic circuit design layout is completed, the next most important piece of information required is the fabrication specification. This document communicates to the fabricator all the pertinent details for the physical construction of the circuit and what is needed and expected in the final product. If this information is incomplete or inaccurate, or if a customer has requirements that cannot be reasonably met by a competent manufacturer, time will be unnecessarily lost, at a cost to both the customer and the vendor. For this reason, it is vitally important that the fabrication specifications are checked and rechecked before putting them out for bid. In the sage words of the master carpenter, "Measure twice, cut once."

Manufacturing Tolerances

Manufacturing system operators need not only the dimensions of the part they are to manufacture, but also the tolerance for the important features of the product. With flexible circuits, this is something that must be done with thought, care, and consideration of the realities of flexible circuit materials.

With some features, design tolerances may be critical for the performance, fit, or further processing of the product (line widths, spaces, hole sizes, physical separation of features, positional accuracy, etc.). In these cases, the manufacturer can often employ methods to deal with the requirement on a localized basis. In the case of other features, the tolerance may be less critical, significantly less critical, or even non-critical. An important thing to keep in mind is that flexible materials are not as dimensionally stable as rigid materials, and while local features may be held in tight tolerance relative to each other, features from end to end may be less predictable. Given that flexible circuits are normally installed in some 3D form after assembly, the tight tolerances on planar measurements are often not necessary. If there are questions about a tolerance callout, the designer should contact the manufacturing engineer. It is always best to solve the problem before it becomes a problem.

If there are questions about a tolerance callout, the designer should contact the manufacturing engineer. It is always best to solve the problem before it becomes a problem.

Unclear Layer Designation (Rigid or Flex) The purpose of a product specification is to provide clear, unambiguous instructions on the product's construction. In the case of a multilayer circuit design, this is vitally important. The relationship of internal circuit layers relative to one another has become increasingly important in not only assuring that correct interconnections are being made, but also in product performance, especially with con-

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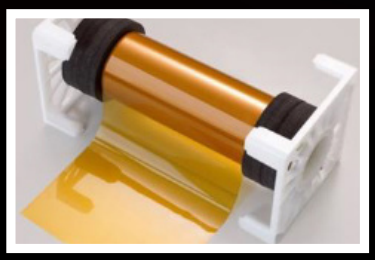

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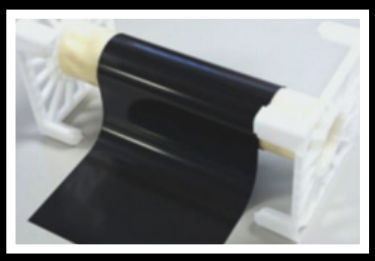

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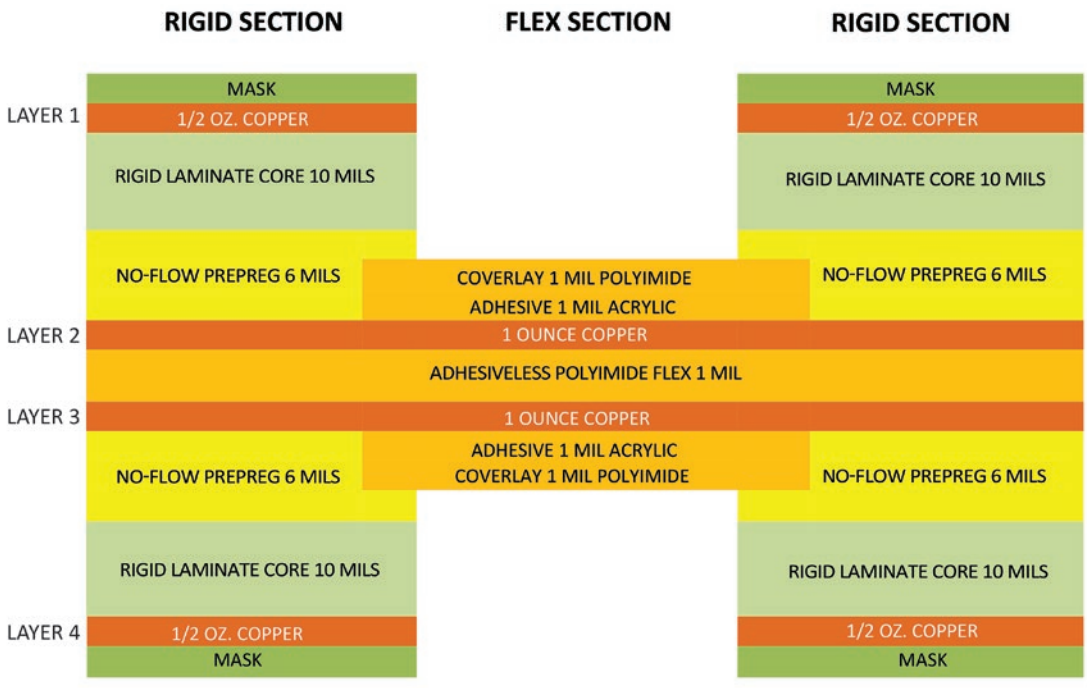


Figure 1: Example of four-layer flex construction.

trolled impedance designs and signal integrity issues. Several different systems have been developed over the years to help assure that there is no uncertainty in the order of the circuit layers in the final construction. The fabricators engineering staff can provide recommendations if needed. Note the thickness and construction of each core in Figure 1.

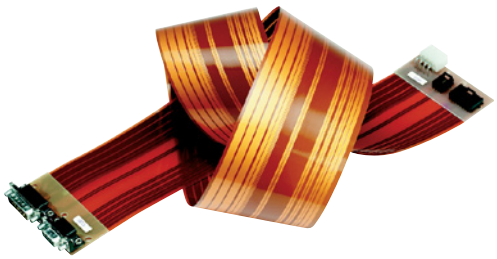
Coverlayer Requirements Not Properly Called Out or Defined

Coverlayer and cover coat are terms normally reserved for flexible circuit constructions and they are by default a defining structural element of both flex and rigid flex circuits. Coverlayers serve as a flexible solder mask of sorts, protecting the delicate circuits from damage and potential wicking of solder along circuit traces, while leaving open access to design features where interconnections are to be made to components by soldering.

It is important to determine the thickness of a coverlayer to allow for maximum flexibility when desired and ensure you have chosen a coverlayer with a sufficient amount of adhesive on it to accommodate the copper weight. Coverlayers are also of importance in the design of areas where the circuit is to be bent either just one time, intermittently, or dynamically, millions or even billions of times over its useful life. The latter case, the dimensions and make of the flexible circuit coverlayer is critical. In dynamic flex circuits, there is need to balance the number of flexible materials on the sides of the conductors where flexing is to occur. It is important to know and understand that there are different types of materials available for use as coverlayer materials, and that there is no single, ideal solution. These material choices include materials that are laminated to the copper circuits using heat and pressure; materials that can be laminated and then photoimaged, like solder mask, to define points of connection; and materials that are simply screen printed on to seal traces, while leaving open features of interest for further processing or for making interconnections.

Number of Flex Layers

The clear majority of flexible circuits have just one or two metal layers. However, an increasing number of high-performance prod-



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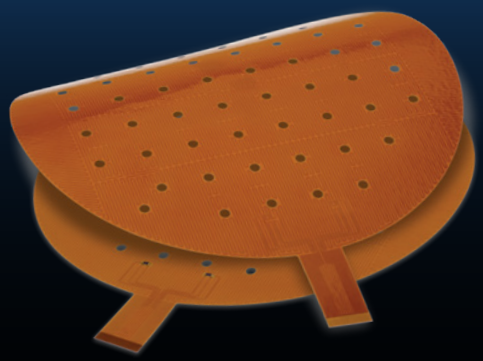

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ucts now require high layer counts and high-density interconnect (HDI) design techniques. As layer count increases, so does the need for control in design generation to accommodate manufacturing process realities. It is also worth noting, while on the topic of layer count, that stiffness increases as a cube of thickness. That is, if one doubles its thickness, the stiffness goes up eightfold ($2^3 = 8$), and thus small increases in thickness due to increases in layer count can greatly decrease circuit flexibility. The converse is also true, of course. The following are some key concerns to be understood and addressed in the design process relative to flex layer count.

As is the case with any multilayer construction, core thickness must be provided with the assumption that copper is clad on at least one surface. The core thickness is generally understood to be the thickness of the dielectric material between the copper layers. The core material can be a simple single-sided piece of copper clad polymer, or it can be clad with copper on both sides. Many different core thicknesses are commonly available for flexible circuits, but the most common is 75 mm, typically comprised of 25 mm of base polymer (e.g., polyimide, polyester) with 25 mm of adhesive (e.g., acrylic, modified epoxy) on either side to bond copper foil to the surface of the base polymer. Thinner and thicker core materials can be procured both with and without adhesive. It is recommended that designers check with their flex vendors for both their recommendations and the availability of the chosen material.

While the discussion so far has been limited to flexible circuit core material, rigid materials are employed in the fabrication of rigid-flex circuits. Of course, any of the myriad core materials used in rigid multilayer circuits are also available to make rigid-flex circuits. However, once again, it is advisable to check with the flex manufacturer for advice as to what options are most common and readily available.

Separation Distance Between Flex Circuit Cores

When a product requires two or more cores, there is a need to define in the specification what the spacing requirements are between cores. The spacing can impact product performance (physical and electrical) and, most obviously, thickness. In some designs, the spacing between flex circuit cores may be filled with dielectric material, but with other designs the dielectric between flex cores in

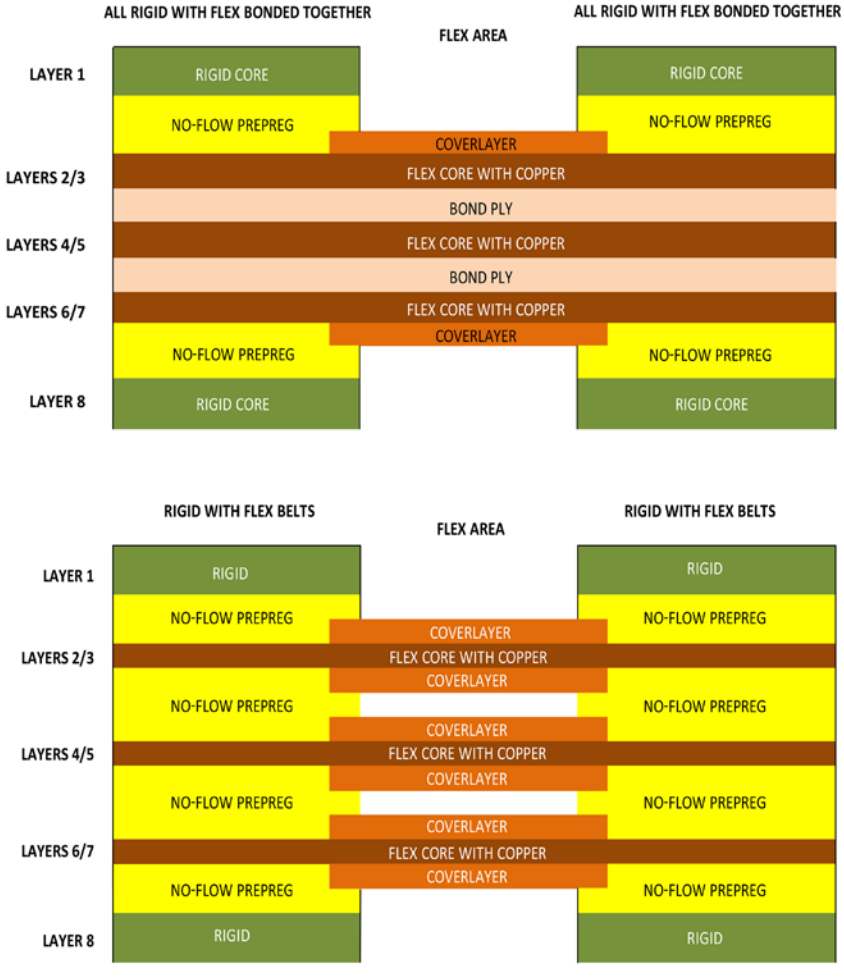

Figure 2: Bonded vs. unbonded flex areas.

the flex area may be omitted to assure maximum flexibility (Figure 2).

If the core layers must be unbonded, this should be noted in the documentation. Those areas where bonding is to be avoided should be identified in the design artwork package. The unbonded areas must have a coverlayer applied to each exposed side (Figures 2 and 3). In laminated areas, it is not required and arguably a liability when plated through-hole reliability through the assembly process is considered. Obviously, in areas where interconnection is required between multiple layers of internal circuits, a dielectric is required as shown in Figure 2.

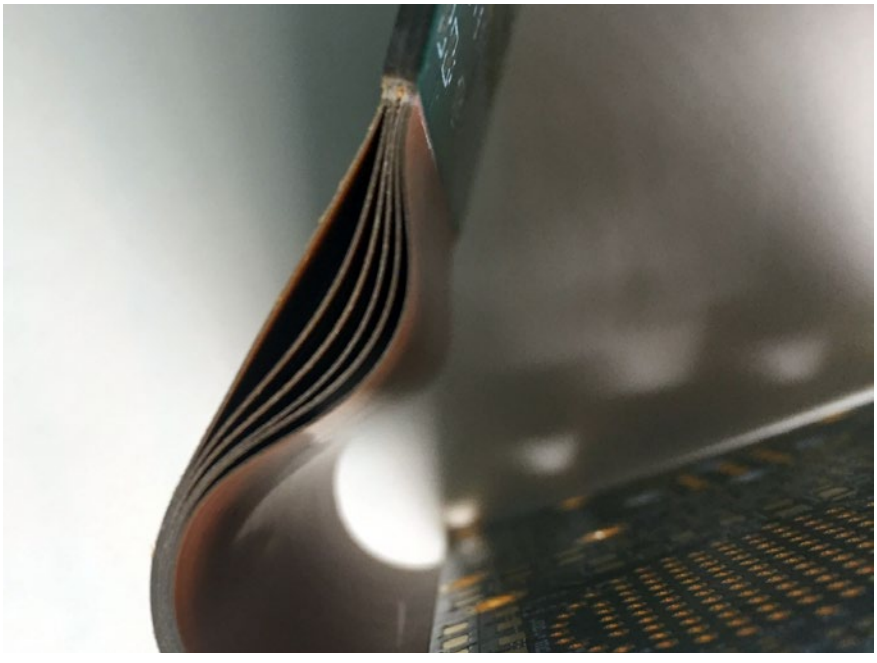

Figure 3: Completed PCB flex belts separated.

Circuit Layup Symmetry

It is a long-standing practice to design multilayer circuit structures with special attention given to the symmetry of the layers in the circuit. That is, the construction should be balanced from center to surface on both sides of the circuit board, whether rigid or flex. Balanced construction is for the rigid section of rigid-flex. It is preferred that flex cores be balanced, too; however, it is not mandatory. This is most easily accomplished by choosing core materials that feature two metal layers. It's more difficult to control this balance when using core materials with an odd number of metal layers.

The symmetry requirement applies to the layer count as well as the overall copper area of the different layers. In this regard, the retention of maximum copper in the circuit pattern is beneficial to manufacturing, because copper is a dimensionally stable element of the construction. The base polymer is by its very nature flexible, and not intrinsically dimensionally stable.

Designing for Bending—Understanding the Important Issues

Bending and flexing are hallmark functions of a flex circuit, whether the circuit is bent once or flexed millions of times. Understanding specific design rules for flex circuits is crucial for success in the field. The first thing to keep in mind is perhaps the most obvious: The thicker the cross-section of the material stack in the bend area, the less flexible it will be. It is important to keep the area where bending or flexing is to occur as thin as possible. Ideally it should be a single metal layer, if possible. This is especially true for dynamic flex circuit applications. **FLEX007**

To download your copy of *The Printed Circuit Designer's Guide to...Flex and Rigid-Flex Fundamentals,* click here.

Dave Lackey is vice president of business development at American Standard Circuits. **Anaya Vardya** is CEO of American Standard Circuits.

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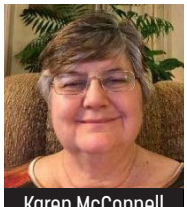
Anaya Vardya

1 Karen McConnell: Recipient of the IPC Raymond E. Pritchard Hall of Fame Award ▸


Karen McConnell

Karen McConnell after being inducted into the Raymond E. Pritchard Hall of Fame: "At the time, in the late '80s and early '90s, there were rumors going around that printed circuit boards were going to disappear, and ASICs were going to take over the world. But something in printed circuit boards fascinated me."

2 The Magnitude of Stackup Considerations ▸

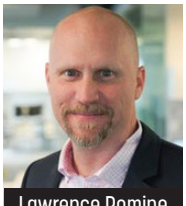

Mike Creeden

"It is similar to the framework used to pour concrete cement—you need to get the framework right because the framework has such a big impact on the final outcome. Such is the case with shaping the success or failure of our circuits."

3 Sensible Design: The Role of Resins and Conformal Coatings in Your Applications ▸

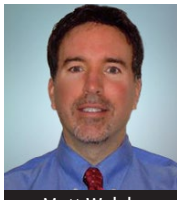
This month, Phil Kinner examines some of the key differences between conformal coatings, encapsulation resins, and potting compounds to help designers make more informed decisions, and ultimately help to increase the performance, reliability and lifetime of your electronic circuitry.

4 Altium Introduces New Subscription Model ▸


Lawrence Romine

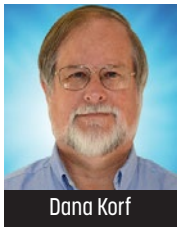
Andy Shaughnessy chats with Lawrence Romine about Altium's new subscription model for their Altium 365 platform. They discuss what this means for existing and future Altium customers, and some of the drivers leading to this development, including evolving use patterns among customers during the pandemic.

5 Managing Footprints With Integrated EDA Tools ▸


Matt Walsh

Electronics companies are always under great pressure to continually grow and innovate. In addition to navigating ever-accelerating design cycles, they must also address and overcome generational complexities associated with their products, the underlying components they use, and the human capital accountable for delivering on time and on budget.

6 Dana on Data: Factory 4.0 NPI Compatible Industry Specification Format ▸


Dana Korf

IPC APEX EXPO's emphasis on the Connected Factory Initiative based on CFX and IPC-2581 is underway in a virtual mode this month. One area that has not been addressed is the automation of industry technical specifications from organizations like IPC, ASTM, UL, IEC, etc.

7 Averatek Corporation Launches the A-SAP 'Community of Interest' ▸

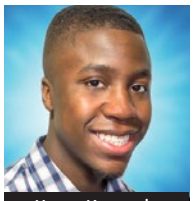
Averatek Corporation has launched the A-SAP™ Community of Interest. This web-based content platform was developed as a central resource for the industry: so that all members of the supply chain—from designers to end users—can exchange information and insights about the A-SAP™ leading-edge PCB fabrication process.

8 DownStream Focused on Rigid-Flex and Embedded Component Support ▸


Joe Clark

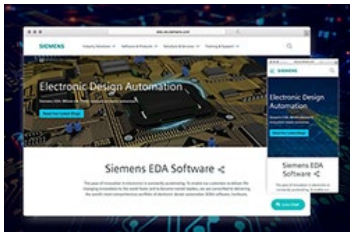
Editor Kelly Dack and Joe Clark, co-founder of DownStream Technologies, discuss trends in PCB design and how this has led to the company's introduction of rigid-flex design support for their tools.

9 Fresh PCB Concepts: Mitigating the Increasing Prices of PCBs ▸


Harry Kennedy

By now, you might have noticed that the cost of PCBs is increasing. What's worse is that there are also supply chain issues causing additional delays on PCBs. You can't redesign every board in order to reduce cost. Instead, try these tips to reduce manufacturing costs.

10 Siemens EDA Launches New Home Website ▸



Siemens EDA (formerly Mentor, A Siemens Business and now part of Siemens Digital Industries Software) is proud to announce our new home website, located at https://eda.sw.siemens.com.

PCBDesign007.com for the latest circuit design news and information.

Flex007.com focuses on the rapidly growing flexible and rigid-flex circuit market.

Career Opportunities

How Do Your Team Members Stack Up?

Find industry-experienced candidates at I-Connect007.

For just $750, your 200-word, full-column ad will appear in the "career opportunities" section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs, and suppliers.

In addition, your ad will be featured in at least one of our newsletters, and your posting will appear on our **jobConnect007.com** board, which is also promoted in every newsletter.

Potential candidates can click on your ad and submit a resume directly to the email address you provide or be directed to the URL of your choice. If you wish to continue beyond the first month, the price is the same per month.

No contract required. We even include your logo in the ad, which is great branding!

To get your ad into the next issue, contact:
Barb Hockaday at barb@iconnect007.com or +1 916.365.1727 (-8 GMT PST)

I-Connect007
GOOD FOR THE INDUSTRY

smt007 pcb007 pcb design007

Career Opportunities

Micropack Private Limited
Sales Representatives

Micropack is a leading Indian PCB manufacturer with a state-of-the-art facility in Bangalore. Our focus on quality and reliability is demonstrated by the fact that we are certified to Nadcap, MIL 31032 & AS9100, apart from many customer approvals.

Catering to both quick-turn and medium volume requirements, our product range covers:

- Double-sided & multilayer PCBs, up to 30 layers
- Rigid-flex PCBs
- High-copper PCBs
- Hybrid PCBs with FR4+ Hydrocarbon Ceramic Substrates
- Heatsink Multilayer PCBs—Metal core and thermal plate PCBs

We are looking beyond our borders for sales representatives to expand our customer reach in the United States, Europe & South America.

Candidates must have previous PCB sales experience and should understand the technical aspects of printed circuit board manufacturability.

Contact us for more information.
mp3@micropack.in

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We're Hiring!
Atlanta Georgia Facility

ADVANCED CIRCUITRY INTERNATIONAL is a world class supplier of RF/microwave and antenna PCBs. We have four state-of-the-art facilities on three continents to serve our customers. From rapid prototype development to large scale production ramp-ups, we supply many notable OEMs and EMS companies around the world.

As we are anticipating rapid growth for 2021 and beyond, we are recruiting for the following positions:

- Manufacturing manager
- Process engineering
- Sales and business development
- Maintenance management

Qualifications:

- 5-10 years' experience working in the PCB industry
- The ability and drive to learn about our unique product offering
- Excellent written and oral communication skills
- Strong, honest work ethic
- Degree in engineering, operations management, or related field preferred but not required

What We Offer:

- Excellent salary and benefits commensurate with experience

If you want to be part of the upcoming ***5G*** revolution and the growth in RF/microwave and antenna PCB manufacturing, consider a career at **ACI**. Were located in the Northern Atlanta suburbs, where you will enjoy a moderate climate, affordable housing, low taxes, quality school systems and numerous recreational opportunities. Please send your resume in confidence to: Career@aciatlanta.com

apply now

Career Opportunities

Circuit Engineering

Planning Engineer

Experience

- Minimum of 5 years' working within printed circuit board manufacturing industry

Responsibilities

- Review Gerber data and talk with the customer when necessary
- Create production traveler based on Gerber data to release the order
- Improve process capability, yields and cost while maintaining safety and improving quality standards
- Work with customers in developing cost-effective production processes

Quality Engineer/Manager

Experience

- Minimum of 2 years' working within printed circuit board industry
- Possess working knowledge of the IPC requirements and submitting PPAP reports
- Should have knowledge of working with the A16949 certification

Responsibilities

- Perform defect reduction analysis and activities
- Participate in the evaluation of processes, new equipment, facility improvements and procedures

Sales Associate/Customer Service

- Should have a minimum of 2 years' experience
- Salary plus commission

All positions will be on location at Circuit Engineering, 1390 Lunt Ave., Elk Grove Village, Illinois, not remote!

Contact: Felix Simon: (847) 867-7942

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Indium Corporation: Field Sales Representative

Field Sales Representative serves as lead sales contact and customer advocate to maintain existing sales and to drive new qualifications and sales of products and services through effective account management and coordination of efforts throughout Indium Corporation's Metals, Compounds, Solar and Reclaim (MCSR) organization. This position is ideal for a sales- and customer-focused individual with an engineering degree.

- Develop, cultivate, and follow-up with prospective and existing customers to generate orders
- Develop an in-depth expertise of product offerings
- Work to gain insight into customer activities for future R&D developments
- Respond to customer requests for product data, specifications, and service information
- Identify customer requirements, priorities, and opportunities
- Build strong, trusting relationships with key decision-makers and influencers at target accounts
- Gather competitive insight, including pricing, delivery, and performance information
- Visit customer facilities to observe manufacturing processes and exchange information
- Promote industry recognition of Indium Corporation, its products, and its services
- Be a key member of overall team, including worldwide sales organization, product management, operations, engineering, R&D, etc.
- Submit required paperwork in timely manner
- Work within established budget, while increasing market share
- Perform other duties and projects as assigned

Click below for more details on job responsibilities and requirements.

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Career Opportunities

SUMMIT INTERCONNECT

Senior Account Manager
Midwest Region

Summit Interconnect, a leading North American manufacturer of advanced technology printed circuit boards across all end-user markets, is seeking an experienced, dynamic leader to drive new business in the Midwest Region of the U.S.

Headquartered in Anaheim, Calif., with additional locations in California and Toronto, Can., Summit's manufacturing features facility-specific expertise in rigid, flex, rigid-flex, RF/MW, and HDI PCBs.

The ideal candidate is highly motivated and should possess in-depth market knowledge, deep contacts across multiple markets and extensive experience in PCB sales with a demonstrated aptitude in proposing engineered solutions to complex requirements.

Reporting to the VP of Sales, the Midwest Senior Account Manager will be the primary hunter in the region and responsible for monitoring customer, market and competitor activity to build appropriate sales strategies for the region, create a strategic plan to grow existing and new business in the region, and be responsible for interfacing across all levels of the organization.

Preference is for the applicant to reside in region and be located within one-day travel to key accounts in the metropolitan business areas. However, the proven professional able to demonstrate reach into the region will be considered regardless of physical location.

Compensation will be a combination of salary and commission, with a comprehensive, competitive benefits package.

apply now

SUMMIT INTERCONNECT

Our Summit Anaheim, CA, division currently has multiple open positions for planning engineers.

The planner is responsible for creating and verifying manufacturing documentation, including work instructions and shop floor travelers. Review lay-ups, details, and designs according to engineering and customer specifications through the use of computer and applications software. May specify required manufacturing machinery and test equipment based on manufacturing and/or customer requirements. Guides manufacturing process development for all products.

Responsibilities:

1. Accurately plan jobs and create shop floor travelers.
2. Create documentation packages.
3. Use company software for planning and issuing jobs.
4. Contact customers to resolve open issues.
5. Create TDR calculations.
6. Assist in the training of new planning engineers.
7. Review prints and purchase orders.
8. Create stackups and order materials per print/spec.
9. Plan jobs manufacturing process.
10. Institute new manufacturing processes and or changes.

Education/Experience:

1. High school diploma or equivalent
2. Minimum five (5) years' experience in the printed circuit board industry with three (3) years as a planning engineer.
3. Must be able to cooperate and communicate effectively with customers, management, and supervisory staff.
4. Must be proficient in rigid, flex, rigid/flex, and sequential lam designs.

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Career Opportunities

American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, penalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

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EAGLE electronics Inc.
MANUFACTURERS OF QUALITY PRINTED CIRCUIT BOARDS

Pre-CAM Engineer

Illinois-based PCB fabricator Eagle Electronics is seeking a pre-CAM engineer specific to the printed circuit board manufacturing industry. The pre-CAM Engineer will facilitate creation of the job shop travelers used in the manufacturing process. Candidate will have a minimum of two years of pre-CAM experience and have a minimum education level of an associate degree. This is a first-shift position at our Schaumburg, Illinois, facility. This is not a remote or offsite position.

If interested, please submit your resume to HR@eagle-elec.com indicating 'Pre-CAM Engineer' in the subject line.

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Process Engineer

We are also seeking a process engineer with experience specific to the printed circuit board manufacturing industry. The process engineer will be assigned to specific processes within the manufacturing plant and be given ownership of those processes. The expectation is to make improvements, track and quantify process data, and add new capabilities where applicable. The right candidate will have a minimum of two years of process engineering experience, and a minimum education of bachelor's degree in an engineering field (chemical engineering preferred but not required). This is a first shift position at our Schaumburg, Illinois, facility. This is not a remote or offsite position.

If interested, please submit your resume to HR@eagle-elec.com indicating 'Process Engineer' in the subject line.

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Career Opportunities

Now Hiring

Director of Process Engineering

A successful and growing printed circuit board manufacturer in Orange County, CA, has an opening for a director of process engineering.

Job Summary:

The director of process engineering leads all engineering activities to produce quality products and meet cost objectives. Responsible for the overall management, direction, and coordination of the engineering processes within the plant.

Duties and Responsibilities:

- Ensures that process engineering meets the business needs of the company as they relate to capabilities, processes, technologies, and capacity.
- Stays current with related manufacturing trends. Develops and enforces a culture of strong engineering discipline, including robust process definition, testing prior to production implementation, change management processes, clear manufacturing instructions, statistical process monitoring and control, proactive error proofing, etc.
- Provides guidance to process engineers in the development of process control plans and the application of advanced quality tools.
- Ensures metrics are in place to monitor performance against the goals and takes appropriate corrective actions as required. Ensures that structured problem-solving techniques are used and that adequate validation is performed for any issues being address or changes being made. Develops and validates new processes prior to incorporating them into the manufacturing operations.
- Strong communication skills to establish priorities, work schedules, allocate resources, complete required information to customers, support quality system, enforce company policies and procedures, and utilize resources to provide the greatest efficiency to meet production objectives.

Education and Experience:

- Master's degree in chemical engineering or engineering is preferred.
- 10+ years process engineering experience in an electronics manufacturing environment, including 5 years in the PCB or similar manufacturing environment.
- 7+ years of process engineering management experience, including 5 years of experience with direct responsibility for meeting production throughput and quality goals.

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Now Hiring

Process Engineering Manager

A successful and growing printed circuit board manufacturer in Orange County, CA, has an opening for a process engineering manager.

Job Summary:

The process engineering manager coordinates all engineering activities to produce quality products and meet cost objectives. Responsible for the overall management, direction, and coordination of the engineering team and leading this team to meet product requirements in support of the production plan.

Duties and Responsibilities:

- Ensures that process engineering meets the business needs of the company as they relate to capabilities, processes, technologies, and capacity.
- Stays current with related manufacturing trends. Develops and enforces a culture of strong engineering discipline, including robust process definition, testing prior to production implementation, change management processes, clear manufacturing instructions, statistical process monitoring and control, proactive error proofing, etc.
- Ensures metrics are in place to monitor performance against the goals and takes appropriate corrective actions as required. Ensures that structured problem-solving techniques are used and that adequate validation is performed for any issues being address or changes being made. Develops and validates new processes prior to incorporating into the manufacturing operations

Education and Experience:

- Bachelor's degree in chemical engineering or engineering is preferred.
- 7+ years process engineering experience in an electronics manufacturing environment, including 3 years in the PCB or similar manufacturing environment.
- 5+ years of process engineering management experience, including 3 years of experience with direct responsibility for meeting production throughput and quality goals.

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Career Opportunities

LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Sales Account Manager

Sales Account Management at Lenthor Engineering is a direct sales position responsible for creating and growing a base of customers that purchase flexible and rigid flexible printed circuits. The account manager is in charge of finding customers, qualifying the customer to Lenthor Engineering and promoting Lenthor Engineering's capabilities to the customer. Leads are sometimes referred to the account manager from marketing resources including trade shows, advertising, industry referrals and website hits. Experience with military printed circuit boards (PCBs) is a definite plus.

Responsibilities

- Marketing research to identify target customers
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Providing ongoing service to the customer
  - Develop long-term customer strategies to increase business

Qualifications

- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is a leader in flex and rigid-flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Senior Process Engineer

Job Description

Responsible for developing and optimizing Lenthor's manufacturing processes from start up to implementation, reducing cost, improving sustainability and continuous improvement.

Position Duties

- Senior process engineer's role is to monitor process performance through tracking and enhance through continuous improvement initiatives. Process engineer implements continuous improvement programs to drive up yields.
- Participate in the evaluation of processes, new equipment, facility improvements and procedures.
- Improve process capability, yields, costs and production volume while maintaining safety and improving quality standards.
- Work with customers in developing cost-effective production processes.
- Engage suppliers in quality improvements and process control issues as required.
- Generate process control plan for manufacturing processes, and identify opportunities for capability or process improvement.
- Participate in FMEA activities as required.
- Create detailed plans for IQ, OQ, PQ and maintain validated status as required.
- Participate in existing change control mechanisms such as ECOs and PCRs.
- Perform defect reduction analysis and activities.

Qualifications

- BS degree in engineering
- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is the leader in Flex and Rigid-Flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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Career Opportunities

Manncorp™

SMT Operator
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:

- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:

- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision
- Ability to lift up to 50 lbs. repetitively

We Offer:

- Competitive pay
- Medical and dental insurance
- Retirement fund matching
- Continued training as the industry develops

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Manncorp™

SMT Field Technician
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

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Career Opportunities

BLACKFOX
Premier Training & Certification

IPC Instructor

Longmont, CO; Phoenix, AZ; U.S.-based remote

Independent contractor, possible full-time employment

Job Description

This position is responsible for delivering effective electronics manufacturing training, including IPC Certification, to students from the electronics manufacturing industry. IPC instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC Certification Programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will conduct training at one of our public training centers or will travel directly to the customer's facility. A candidate's close proximity to Longmont, CO, or Phoenix, AZ, is a plus. Several IPC Certification Courses can be taught remotely and require no travel.

Qualifications

Candidates must have a minimum of five years of electronics manufacturing experience. This experience can include printed circuit board fabrication, circuit board assembly, and/or wire and cable harness assembly. Soldering experience of through-hole and/or surface-mount components is highly preferred.

Candidate must have IPC training experience, either currently or in the past. A current and valid certified IPC trainer certificate holder is highly preferred.

Applicants must have the ability to work with little to no supervision and make appropriate and professional decisions.

Send resumes to Sharon Montana-Beard at sharonm@blackfox.com.

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MivaTek Global

MivaTek Global: We Are Growing!

MivaTek Global is adding sales, technical support and application engineers.

Join a team that brings new imaging technologies to circuit fabrication and microelectronics. Applicants should have direct experience in direct imaging applications, complex machine repair and/or customer support for the printed circuit board or microelectronic markets.

Positions typically require regional and/or air travel. Full time and/or contractor positions are available.

Contact **HR@MivaTek.Global** for additional information.

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Career Opportunities

APCT
Passion | Commitment | Trust

APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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eptac
TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Career Opportunities

U.S. CIRCUIT

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

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YOUR JOB AD HERE

For information, please contact:
BARB HOCKADAY
barb@iconnect007.com
+1 916.365.1727 (PACIFIC)

I-Connect007
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I-007eBooks

Distinctly different.

Our books are written by recognized industry experts.
At around 8,000 words, they are unique in that they are able to be incredibly focused on a specific slice of technology.

"I-007ebooks are like water in the desert
...it's up to you to drink it in order to survive!"

Stephen V. Chavez
PCEA Chairman, MIT, CID+

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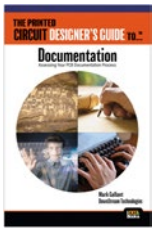
NOW AVAILABLE:
***Implementing "Digital Twin" Best Practices From Design Through Manufacturing with Expert Jay Gorajia*, a 12-part micro webinar series.**

I-007eBooks The Printed Circuit Designer's Guide to...

Thermal Management: A Fabricator's Perspective

by Anaya Vardya, American Standard Circuits

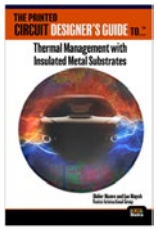
Beat the heat in your designs through thermal management design processes. This book serves as a desk reference on the most current techniques and methods from a PCB fabricator's perspective.



Documentation

by Mark Gallant, Downstream Technologies

When the PCB layout is finished, the designer is still not quite done. The designer's intent must still be communicated to the fabricator through accurate PCB documentation.



Thermal Management with Insulated Metal Substrates

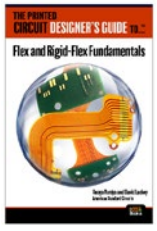
by Didier Mauve and Ian Mayoh, Ventec International Group

Considering thermal issues in the earliest stages of the design process is critical. This book highlights the need to dissipate heat from electronic devices.

Fundamentals of RF/Microwave PCBs

by John Bushie and Anaya Vardya, American Standard Circuits

Today's designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing radio frequency/microwave PCBs. This micro eBook provides information needed to understand the unique challenges of RF PCBs.



Flex and Rigid-Flex Fundamentals

by Anaya Vardya and David Lackey, American Standard Circuits

Flexible circuits are rapidly becoming a preferred interconnection technology for electronic products. By their intrinsic nature, FPCBs require a good deal more understanding and planning than their rigid PCB counterparts to be assured of first-pass success.

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