THE pcb design MAGAZINE

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January 2016

MEDICAL ELECTRONICS

Medical PCB Design:
Not Just Another High-Rel Board

Interview with Kenneth MacCallum, p. 10

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THIS MONTH'S FEATURE ARTICLES

MEDICAL ELECTRONICS

Circuit board designers and fabricators are paying more attention than ever to the global medical electronics market, which is slated to reach $56 billion in the next five years. But medical PCBs come with their own unique technological and regulatory challenges. This month, we bring you interviews with some of the movers and shakers in the world of medical PCB design and manufacturing: Kenneth MacCallum of StarFish Medical, Anaya Vardya of American Standard Circuits, and Amir Davoud of Innovative Circuits Inc. Happy new year!

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THE SHAUGHNESSY REPORT

Doing my Part for Medical Electronics

by Andy Shaughnessy
I-CONNECT007

If you're like me, and most of you are, you've started getting mail from AARP. You exercise, because if you don't, you feel like a fat slob. Your body hurts more often, and you just deal with the pain until it gets bad enough to go to the doctor. This is especially true for men; tough guys like us don't like going to the doctor, unless we've actually severed an artery. Otherwise, we don't need no stinkin' doctors!

So when I first suspected I might have a hernia, I thought, "What is this thing poking through my stomach? I'll just ignore it, and it will go away, like a noise in my car's engine." It hurt the most when I cut the grass on my riding mower, so I quit mowing the lawn. I liked that part!

But the pain didn't go away. Eventually, when the pain got worse, my fledgling men's common sense kicked in and I visited my local sawbones. "Not a big deal. Just routine outpatient surgery," the doctor opined. "You'll be in and out in a couple of hours, with a cool scar to boot, and some great painkillers."

The surgeon couldn't operate on my timeline; it had to be the week before Thanksgiving, or right before Christmas. I picked the former, so I'd be more or less healed by Christmas.

On operating day, a nurse got me all prepped and ready for the scalpel. They gave me a shot of something similar to Valium (the Propofol came later), and wheeled my bed down the hall. All I could see were ceiling lights going by, just like on "House."

Then we entered the operating room. The middle of the operating room was empty, because my rolling bed was going to be parked there. But the walls were ringed with dozens of beeping and pinging electronic monitors. I've never seen so many electronic devices together in my life. I saw one Agilent monitor, and a bunch of others with names I couldn't make out. It reminded me of the IT room in most companies. I guess they had to be set up to handle routine surgery like mine, and the not-so-routine operations as well.

Then it was lights out. I woke up to the surgeon handing me a pill. "This is Dilaudid. Take it now." I did. I didn't feel much discomfort that day, but the next few days were pretty painful, despite my Percocets. But it was healing. On the fourth day, our acoustic band had a gig. I propped myself up on a stool and played for four hours. It's easy to play the blues when you're trying not to hurt your lower stomach area!

I'm glad I was able to do my part, however small, for the medical electronics market. And with humans living longer each year, medical is one segment that's destined to keep growing. This month, we focus on medical electronics, and those who design and manufacture PCBs for medical devices.

In our cover story, Kenneth MacCallum of StarFish Medical explains what goes into designing PCBs for medical devices, and some of the regulatory hurdles associated with that market. Editor Dan Beaulieu and Anaya Vardya of American Standard Circuits discuss ASC's approach to fabricating medical PCBs and the technical challenges of creating these high-reliability boards. And Amir Davoud of Innovative Circuits explains how the company's focus on flex and rigid boards allows them to meet their medical customers' evolving requirements.

For more coverage of medical PCB manufacturing, check out our sister magazines, *The PCB Magazine* and *SMT Magazine*.

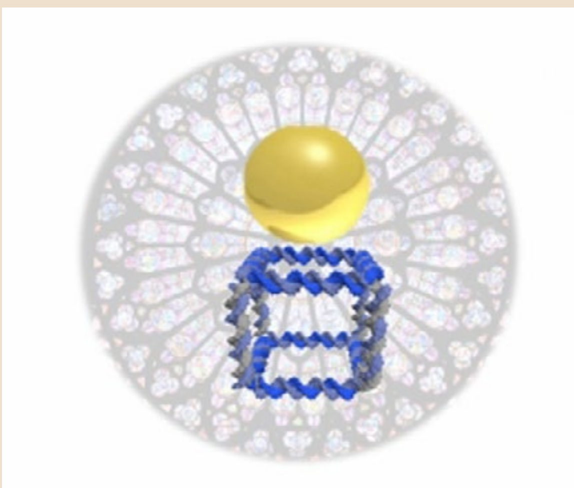
As 2016 gets underway, we'll be bringing you coverage of trade shows, just in case you can't be there. Look for our coverage of the industry's movers and shakers making news at CES, DesignCon, NAMM, IPC APEX EXPO, and CPCA, just to name a few. I hope to see you at an event soon.

It's going to be quite a year! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 16 years. He can be reached by clicking here.

A "Printing Press" for Nanoparticles

Some of the most interesting properties of nanoparticles emerge when they are brought close together—either in clusters of just a few particles or in crystals made up of millions of them. Yet particles that are just millionths of an inch in size are too small to be manipulated by conventional lab tools, so a major challenge has been finding ways to assemble these bits of gold while controlling the three-dimensional shape of their arrangement. Since DNA strands are programmed to pair with other strands in certain patterns, scientists have attached individual strands of DNA to gold particle surfaces to create a variety of assemblies. But these hybrid gold-DNA nanostructures are intricate and expensive to generate, limiting their potential for use in practical materials. The process is similar, in a sense, to producing books by hand.



In results reported online in Nature Chemistry, researchers from McGill's Department of Chemistry outline a procedure for making a DNA structure with a specific pattern of strands coming out of it; at the end of each strand is a chemical "sticky patch." When a gold nanoparticle is brought into contact to the DNA nanostructure, it sticks to the patches. The scientists then dissolve the assembly in distilled water, separating the DNA nanostructure into its component strands and leaving behind the DNA imprint on the gold nanoparticle.

First author Thomas Edwardson says the next step for the lab will be to investigate the properties of structures made from these new building blocks. These could be put to use in areas including optoelectronic nanodevices and biomedical sciences, the researchers say.

Medical PCB Design:

Not Just Another High-Rel Board

by Andy Shaughnessy

Some of the coolest new electronic products have come courtesy of the medical market. I wanted to find out more about this fast-growing segment, so I contacted Kenneth MacCallum, an engineering physicist with StarFish Medical. StarFish is a medical device design company that's created some major electronic medical innovations, and they're about as cutting-edge as you can get.

I asked Kenneth to talk about the medical electronics industry, medical PCB design, and some of the unique challenges that technologists face in this fascinating market. Plus, what does digital health mean for electronics designers?

Andy Shaughnessy: Kenneth, please give us a quick background on StarFish Medical.

Kenneth MacCallum: StarFish is a consulting design engineering firm that specializes in the development of medical devices. Unique for a boutique design firm, we have a full complement of manufacturing services. We work for all sorts of companies, big and little, all across North America and Europe. Many are serial entrepreneurs that have launched and sold medical device start-ups to industry leaders. We work on products as varied as ultrasound systems, lab on a chip, and orthopedic surgery assist devices. Digital health is a rapidly growing segment.


Kenneth MacCallum

Shaughnessy: You're a principal engineering physicist at StarFish, and you're involved in PCB design. Tell us about your work there.

MacCallum: I do two things. I'm an engineering physicist and a project manager. That means I'm a technical guy, but I also make sure projects stay on the rails. From a technical standpoint I behave like an engineer. I design PCBs

and circuits. The engineering physicist part of me adds basic principles analysis of all sorts of fun stuff including optics, algorithmic processing for ultrasound, or image processing. Like most electrical engineers, I also work on firmware and logic design.

***Shaughnessy:** How is designing a medical PCB different than designing any other high-reliability board?*

MacCallum: Although the medical industry is fairly heavily regulated, designing a medical PCB is not that different than designing for lab equipment or a consumer device. There are still safety standards to meet. The medical standards are more stringent and they span a bit more.

“There are still safety standards to meet. The medical standards are more stringent and they span a bit more.”

I've worked in metrology, general engineering (remotely operated vehicles), and consulting engineering for consumer and dental devices. I've seen a bit about what is required for various product sectors, developed products and gone through regulatory hurdles for each. They all have regulatory requirements—especially in Europe—but the requirements are generally harmonized around the world. We meet ISO 60601 for medical and ISO 61010 for laboratory equipment. These are standards we must comply to or we can't sell in the various markets.

***Shaughnessy:** How important is simulation and analysis of medical PCB designs?*

MacCallum: I'm a big fan of simulation, and analysis is sort of my bread and butter. I also like walking into the lab and trying something, but I start at an intuitive level: How do I believe a circuit is working? Then I back it up with simulation to see if it works the way I expect it to work. Often a circuit will see an evolution or even a total rip-up and re-do based upon simulation results.

I apply a sort of quality filter in my head because many times simulation will take you into the weeds. You never know, because simulation doesn't smoke. Simulation is only as good as the quality of the component models you use and often there are a lot of inherent assumptions based in those models.

I'm a big fan of FEA (finite element analysis) to compute impedances of traces, like differential pairs, rather than using some of the analytical solutions. FEA allows me to accurately model the right PCB stack and allows me the flexibility to adjust my space and trace settings depending on whether I've got a nearby plane below or maybe just a fill on each side. One strategy I use often is to make the fills to the side dominate and therefore I need less control over the dielectric and plane below.

Whenever I'm developing circuits or applying rules in circuit layout, I like to think of it at a basic principle level and do a thorough analysis. I don't like apply a rule of thumb unless I've already hashed out in my mind or on paper the purpose of that rule and what problem it's really trying to solve. In many cases there's a big trade-off in all the requirements of any circuit. Whether it is EMC, power, cost or noise, I want to understand all of the tradeoffs and how they may impact all the other circuits that are around, under or on the same board. It's important to understand how all those fit together, putting the right emphasis on the right requirements and not just arbitrarily saying there must always be a certain space trace clearance, component spacing or whatever.

***Shaughnessy:** The medical electronics field is so heavily regulated. What sort of "hoops" do you have to jump through, such as certifications and standards, when dealing with medical PCBs?*

MacCallum: There are a number of regulatory bodies we are concerned with aside from the typical UL, CSA, and FCC. We have to worry

about the FDA in the U.S., Health Canada in Canada, and the Medical Device Directive for Europe. They all have requirements and guidances for how a medical device must be developed. They care deeply about the efficacy and safety of the device. If we don't comply, we're not allowed to sell the device.

For instance, one big part of our development process is repeatedly analyzing risk of harm either to the patient or the user. Risks must be evaluated and mitigated as required. All of this process must be documented correctly. This is something that doesn't often get much consideration for a consumer product. Many of the decisions we make in the design process take risk of harm into account: Are we creating a potential hazard and how can we best mitigate it? You have to consider the probability of failure modes that might change the level of risk and potentially mitigate those too.

None of the other industries I've worked in require this risk-based approach to safety. None of the others care about the safety of a patient. The patient is important because they must trust that the doctor and product really have their best interest at heart. They don't necessarily understand what the device is doing and what the risks are. In some cases they are not even conscious.

***Shaughnessy:** What trends are you seeing in medical PCBs?*

MacCallum: More and more devices want touchscreens and full-on embedded processors whether they are running Android or Linux, etc. Users expect the same sort of interfaces they see with their phones and tablets. We're also seeing a lot of RF, Bluetooth and Wi-Fi. Network connectivity is big. That means suddenly you've got RF sub-circuits. Broadly speaking, phones, laptops, and tablets are all converging. Lots of clients would love if their primary interface to the device was an iPhone.

That trend has interesting implications from a safety perspective. The FDA has guidances which relate to using smartphones and tablets for that purpose.

As we jam more things into our medical devices, the complexity, density and quantity of PCBs increase. Manufacturing requirements and tolerances will become more stringent, and it's going to be great. We're going to have electronics all over the place.

With phones, we've seen that the more sensors they put on, the more apps you can get and suddenly your phone is not only your pocket computer. Sometimes it even works as a phone. It's your notebook, weather predictor, navigation system and all sorts of fun stuff.

The more sensors become inexpensive and available, the more tricks we develop to obtain medical information from these sensors and the more we're going to jam them into a single device. There will continue to be special purpose devices mind you; I don't expect to see an MRI in a phone, not just for the basic geometric reasons. As people invent new technologies, they seem to start as single-purpose devices. As those evolve they get smarter, cheaper, and lighter.

Eventually they'll converge with some other existing technology. I suspect that just as quickly as we can take older technology, mea-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surement techniques, and sensors and combine them into a single "tricorder-y" thing, we're going to be developing new ones. So there's going to be this trajectory of technology and modalities slowly converging and combining, with new ones springing up and living on their own until that technology is combined up into a multipurpose device.

Along that trajectory, there is more and more call to connect in a digital health way. Even if you can't jam the physical elements together into the same package right away, you can at least jam the data together. And that's happing all over the place. Think Fluoroscope data with patient physical data with surgical navigation being jammed together to allow the doctor to provide better care. Eventually the modalities that generated the information will also combine.

Shaughnessy: ***People seem to be living longer. Do you think the medical segment will continue to grow?***

MacCallum: As you live longer your medical requirements increase. The medical segment will definitely continue to grow. There's a big push (especially in the U.S.) to make care less expensive. The effort is relying quite heavily on technology. They want to do the same types of treatments and diagnoses cheaper and faster. The technology required for those purposes must grow to meet that need or we're going to stop living longer.

Shaughnessy: ***Thanks for the information, Kenneth.***

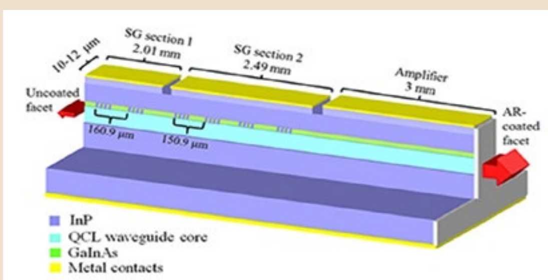
MacCallum: Thank you. **PCBDESIGN**

Single-Chip Laser Delivers Powerful Result

From their use in telecommunication to detecting hazardous chemicals, lasers play a major role in our everyday lives. Now a Northwestern Engineering team has made this ever-important tool even simpler and more versatile by integrating a mid-infrared tunable laser with an on-chip amplifier. This breakthrough allows adjustable wavelength output, modulators, and amplifiers to be held inside a single package.

With this architecture, the laser has demonstrated an order-of-magnitude more output power than its predecessors, and the tuning range has been enhanced by more than a factor of two.

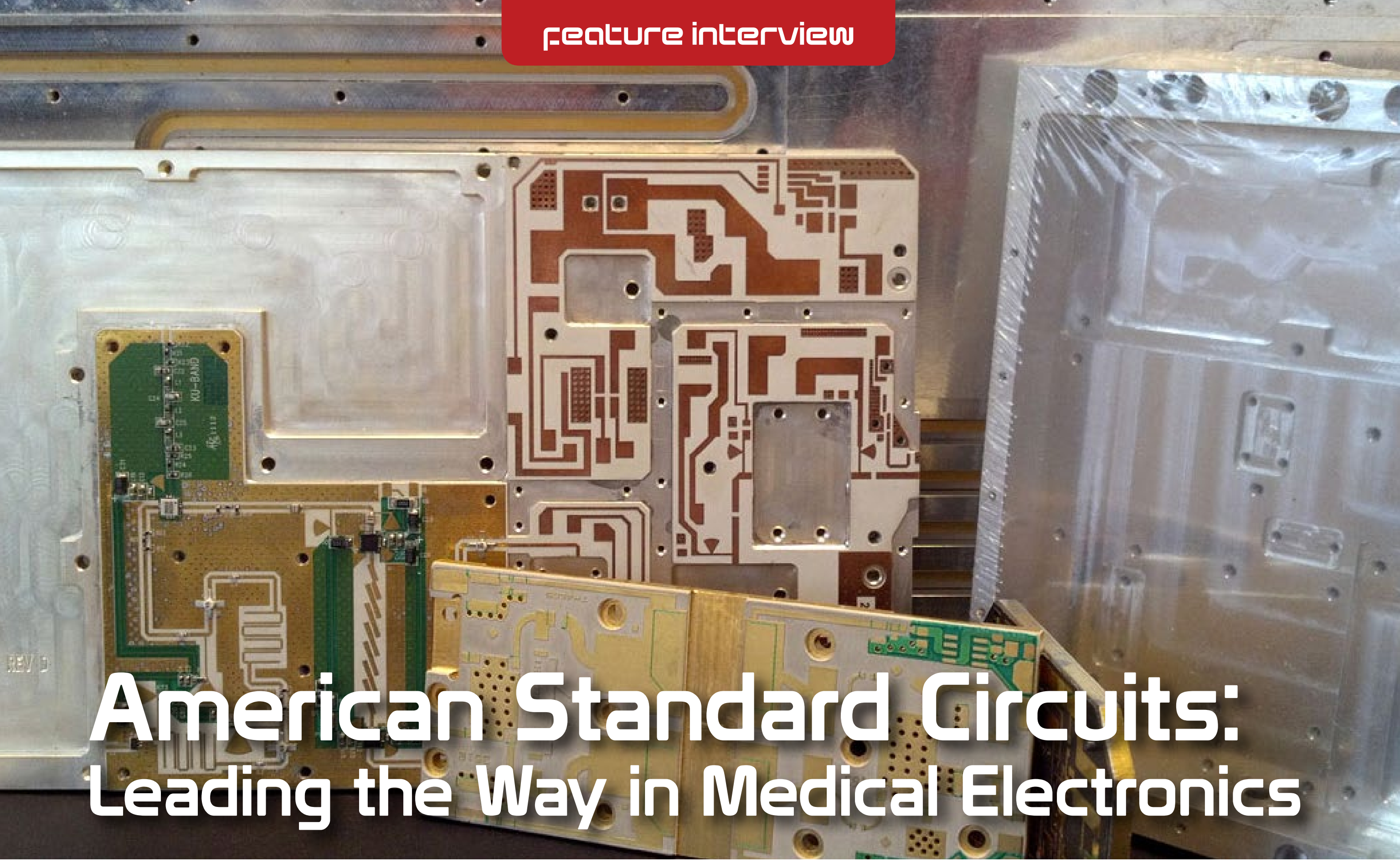
"We have always been leaders in high-power and high-efficiency lasers," said Manijeh Razeghi, Walter P. Murphy Professor of Electrical Engineering and Computer Science, who led the study. "Combining an electrically tunable wavelength with high power output was the next logical extension."



Supported by the Department of Homeland Security Science and Technology Directorate, National Science Foundation, Naval Air Systems Command, and NASA, the research is described in a paper published online on December 21, 2015 in the journal Applied Physics Letters.

With mid-infrared spectroscopy, a chemical can be identified through its unique absorption spectrum. This greatly interests government agencies that aim to detect hazardous chemicals or possible explosive threats. Because Razeghi's new system is highly directional, the high power can be used more efficiently, allowing for the greater ability to detect chemicals. It also allows for standoff application, which keeps personnel physically distant from potentially dangerous environments. The technology could also benefit free-space optical communications and aircraft protection.

"We demonstrated the first continuously tunable, continuous operation, mid-infrared lasers with electrical tuning of the emission wavelength," Razeghi said. "This initial demonstration was very exciting, and continuing developing has led us to a number of new projects."



American Standard Circuits:
Leading the Way in Medical Electronics

by Dan Beaulieu
D.B. MANAGEMENT GROUP

When it comes to innovative fabricators, American Standard Circuits is always at the front of the pack. Naturally, when Editor Andy Shaughnessy asked me to talk to a fabricator about PCBs for the medical market, ASC was the one company that immediately came to mind. I spoke with CEO Anaya Vardya about fabricating medical PCBs, the medical electronics market, and the future of this fast-growing segment.

Dan Beaulieu: Anaya, it's good talking to you again.

Anaya Vardya: Thanks, Dan. It's great to catch up again.

Beaulieu: Please give us a little background on American Standard Circuits.

Vardya: ASC has been in business for more than 27 years. Throughout, we have migrated from a simple double-sided shop to a company that builds a wide variety of products. Today, we build flex, rigid-flex, RF/microwave, metal-backed PCBs and IMPCBs. We are able to build prototypes, quick-turn, high-mix/low-volume and low-mix/high-volume products. We are continuously reinvesting in our business in terms of people and equipment. This year, we have invested over $1.5 million. We are also investing in improving our quality systems.

Beaulieu: When did you get involved with medical PCBs?

Vardya: We first started building parts for medical products in 2009. Often, these products start out as prototypes and take quite a few years to ramp up. We have built flex, rigid-flex, RF/microwave and metal-backed product for the medical industry

Beaulieu: Without getting into specific customers, what sort of medical products do you build PCBs for? What do your boards go into?

Vardya: That's a good question, because we cover a very wide variety of applications including medical. For example, we build flex boards that are used in a digital inflation device for

Anaya Vardya, CEO, American Standard Circuits.

heart stents. We also build boards, both flex and rigid-flex, that are used in blood analyzers. Then we have boards that go into a wide array of markets, such as small boards used as RFID tags in operating rooms. We build metal-backed boards that are used for LED lights for chairs in dentists' offices. One of our most challenging projects was building small rigid-flex boards for a pill camera. These boards are all built from a variety of materials, from Rogers ceramic materials to simple FR-4.

Beaulieu: So you pretty much cover the gamut of medical electronic needs. Are there special or unique technologies that apply to this market?

Vardya: While medical electronics use a wide variety of printed circuit board technologies, there appears to be increasing application of flex and rigid-flex PCBs in this market place.

Beaulieu: Can you tell me roughly what percentage of your business is for medical electronics?

Vardya: Today we estimate about 5% of our business is associated with Medical electronics. We anticipate that this will be a growing market segment for ASC.

Beaulieu: Obviously, when you are dealing with medical applications, it is not over dramatic to talk about being a matter of life and death. Can you talk about what you do in terms of quality assurance and reliability to make sure you are giving your medical customers the very best product when it comes to those features?

Vardya: Dan, one thing that helps us is that we build everything in our facility assuming it needs to be certified to a minimum of IPC Class 3. Reliability is a critical part of what we do especially since we do build a lot of products that are safety related—including boards for active safety automotive electronics. We have invested and trained our quality manager to be an IPC-600-A trainer. We have subsequently certified many of our quality inspectors to IPC-600-A. We are also currently pursuing our AS9100C certification. While this does not directly apply to medical electronics, it is clearly improving our quality system which benefits all of our customers.

Beaulieu: What do you see for the future of medical electronics?

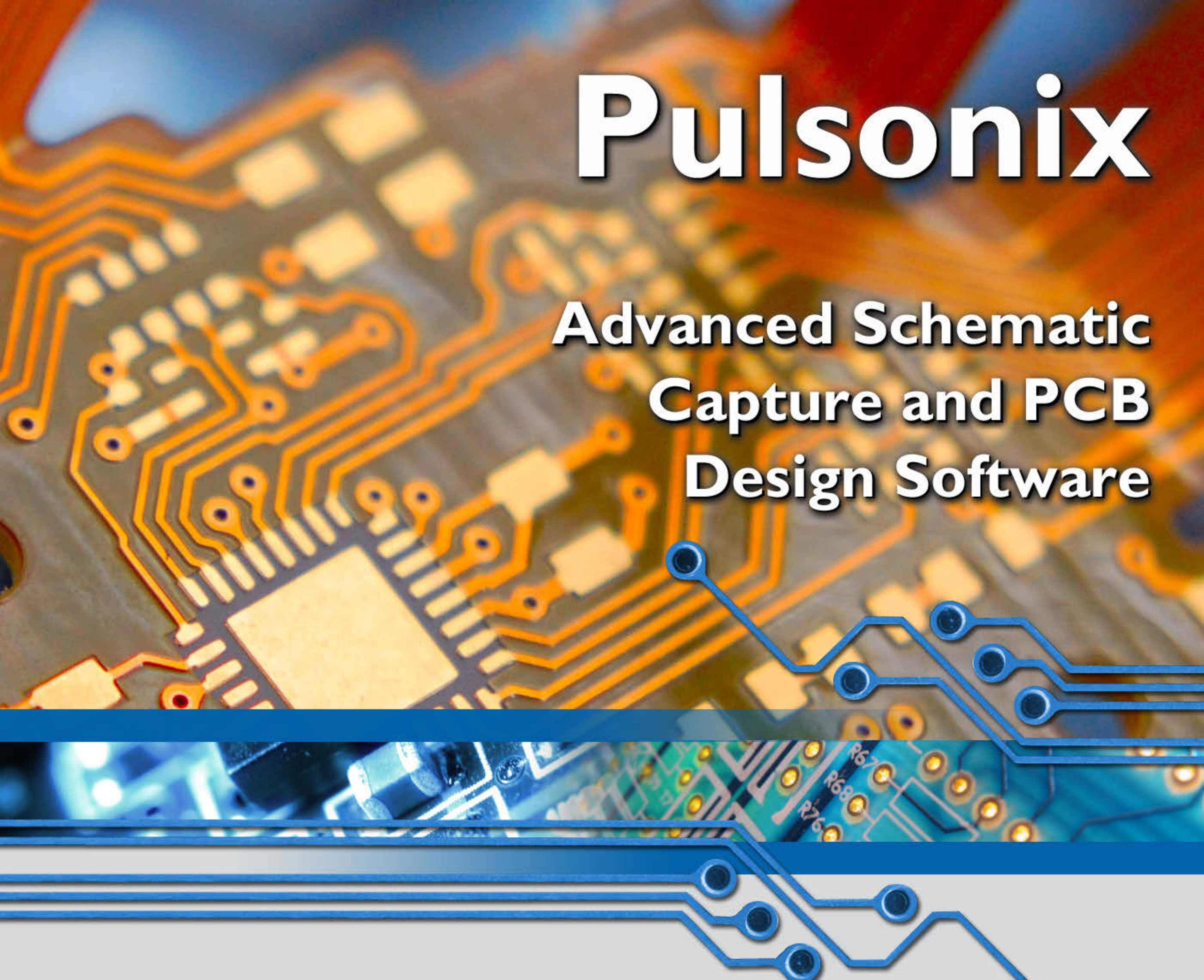
Vardya: I believe that the future for medical electronics is very bright.

Beaulieu: And what are you doing to continue being on the cutting edge when it comes to meeting technology needs?

Vardya: We are investing in people and equipment. We recently appointed Jim Zeman, an industry veteran, to be our director of quality. Jim has many years of experience at Ibiden as a quality manager and is well versed in Japanese techniques. In addition, we hired another industry veteran earlier this year, Rob Coleman, as our VP of operations.

Beaulieu: So you are putting together a real top-rate team. I know those guys, and they're very strong. Have you invested in technology with equipment as well?

Vardya: Yes, we have also invested in both software and equipment to improve our capabilities. We invested in TrueChem software to enable us


Pulsonix
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with SPC, GenFlex to enable us to do a better job of engineering flex and rigid-flex jobs and finally InPlan, which is a rules-based traveler system.

We have also invested in a laser direct imaging tool that helps us with registration, elimination of phototools and improved line/space control; a cupric etcher which also helps improve line/space capability; another X-ray drill machine equipped with state-of-the-art technology improving registration and our controlled depth drilling capability; an inkjet printer for legends and the latest in via filling capability. Some of these are not yet up and running in our facility, but we anticipate most of these will be implemented by the end of Q1 2016.

***Beaulieu:* How much in total dollars have you put into the company by acquiring all of this new software and equipment?**

Vardya: In 2015, we invested more than $1.5 million.

***Beaulieu:* What would you say is the single biggest reason why medical customers should consider using a company like ASC?**

Vardya: Dan, we definitely understand this market. We are focused on high-reliability, leading-edge technologies, and quick-turn capabilities. We are continuously making investments in terms of resources and equipment to this end. Our goal is to make the customer experience as easy as possible. For engineers, we are more than willing to work with them on design for excellence. For flex and rigid-flex designs, we definitely recommend that engineers talk to us during the design phase. A lot of times engineers are looking for quick-turns; however, many times the material lead times can be an impediment. If designers work with us during the design phase, we can work with them on materials. We can even order materials prior to placement of the PO to expedite quick-turns. We are also constantly making investments to enable us to do a better job for our customers.

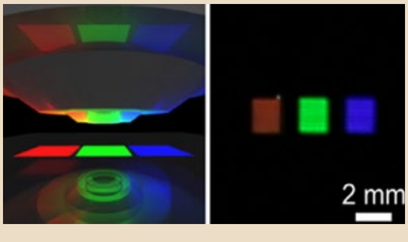
***Beaulieu:* Anaya, once again, thanks for taking the time to talk with me today. I appreciate it.**

Vardya: Thanks, Dan. It was a pleasure spending time with you today. **PCBDESIGN**

Aluminum Nanoparticles Could Improve Electronic Displays

Whether showing off family photos on smartphones or watching TV shows on laptops, many people look at liquid crystal displays (LCDs) every day. LCDs are continually being improved, but almost all currently use color technology that fades over time. Now, a team reports in ACS Nano that using aluminum nanostructures could provide a vivid, low-cost alternative for producing digital color.

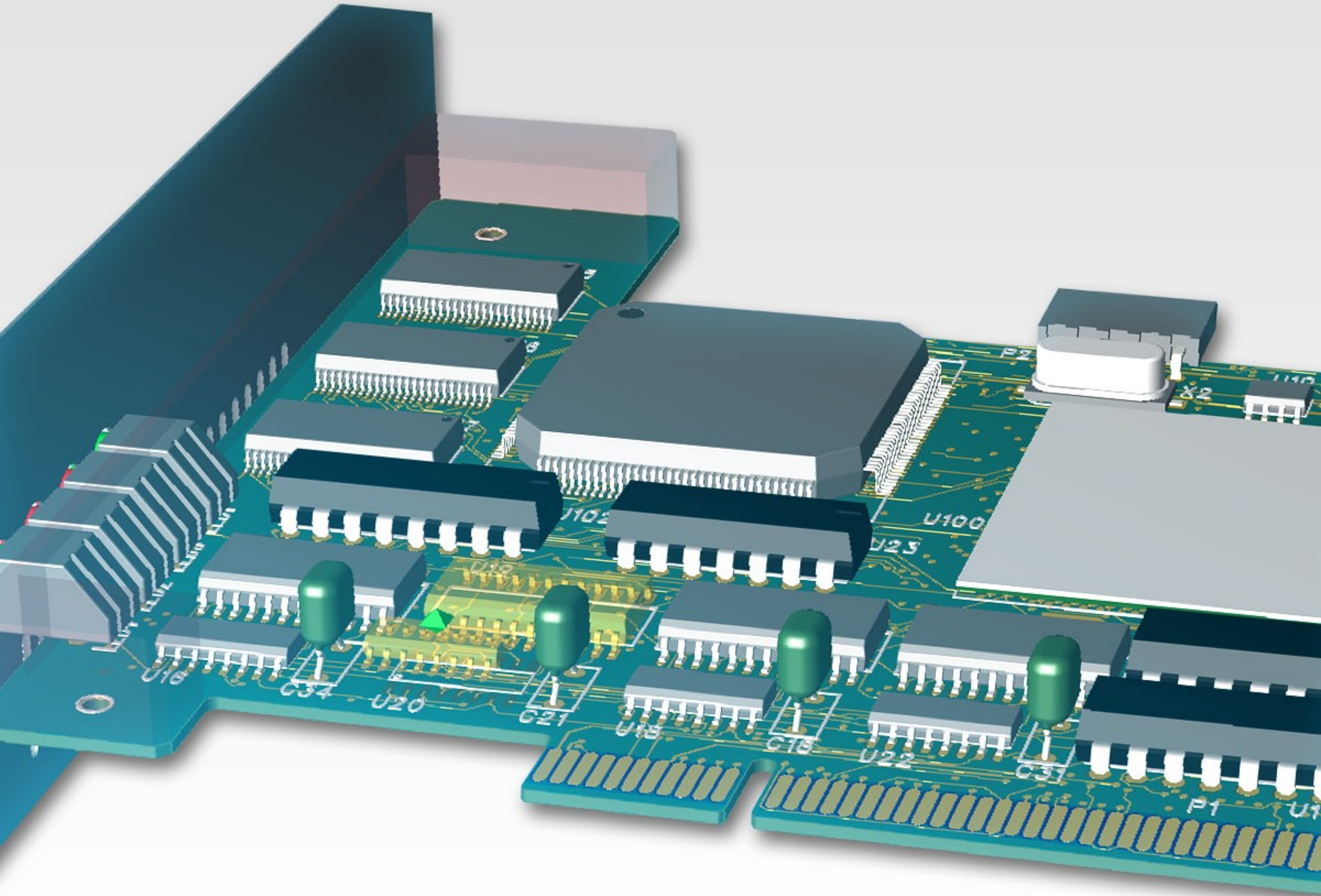
Conventional color technology used in displays is susceptible to photobleaching, or fading. So researchers have looked toward aluminum nanoparticles that can display colors in electronics, thanks to a property called "plasmon resonance." To create plasmonic color devices, researchers group nanostructures into arrays called pixels.

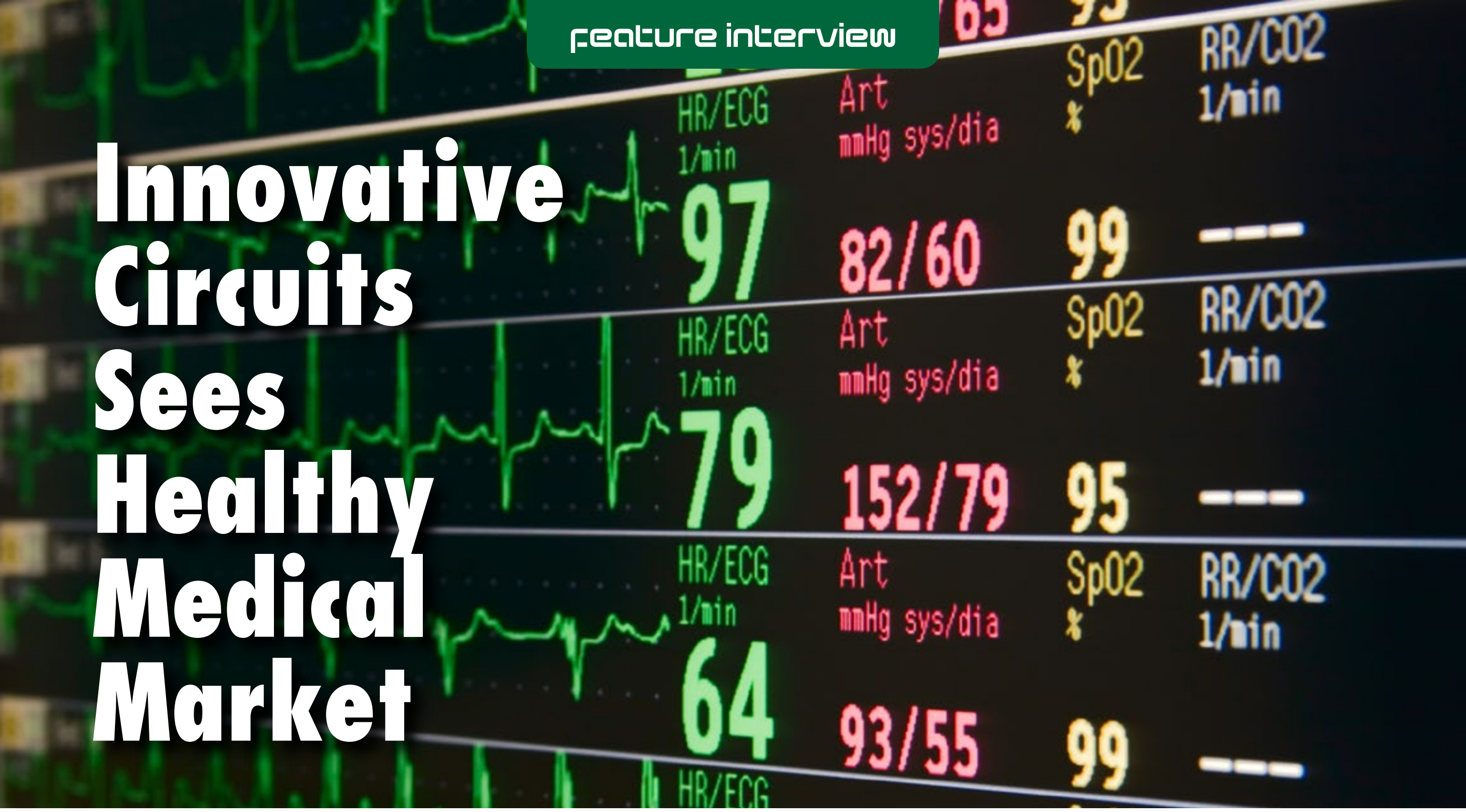


Color is generated by scattering light onto the pixels, with different arrangements creating different colors.

Aluminum plasmonic pixels are advantageous for use in electronic displays because they are inexpensive and can be made in an ultrasmall size, which can increase image resolution. But these pixels create muted and dull colors. In a recent publication, Stephan Link and colleagues developed a method that allows the red end of the color spectrum to be more vibrant.

The researchers used a three-step design approach to create aluminum nanostructure pixels that exploit "Fano interference" — an interaction between the plasmon resonance and the pixel's array structure — to produce vibrant blue-end colors. The researchers then incorporated a set of red, green and blue pixels into a liquid crystal display that could be electrically turned on and off, demonstrating this work's potential use in commercial flat-panel displays.





Innovative Circuits Sees Healthy Medical Market

Medical electronics is one of the fastest growing segments of our industry. Almost weekly, we hear about another cool lifesaving device or piece of medical monitoring equipment. Alpharetta, Georgia-based Innovative Circuits is at the forefront of fabricating medical PCBs, both flex and rigid. I asked Innovative Business Development Manager Amir Davoud to give us a solid diagnosis of the world of medical PCBs.

Andy Shaughnessy: Amir, why don't you start off by giving us a quick background on Innovative Circuits?

Amir Davoud: Innovative Circuits is a fabricator of multilayer rigid PCBs, rigid-flex and flex circuits. Since our inception in 1998, we have remained dedicated to pairing comprehensive engineering support with quickturn and small- to mid-level production solutions. Our clients rely on ICI's extensive knowledge base and highly skilled technicians to assist with their most challenging projects.

Shaughnessy: Innovative Circuits serves a number of medical customers. What sort of devices do these customers create?

Davoud: Our medical clients range from the neurosciences to cardiac care. Most of the projects we work on involve external devices that are either standalone for monitoring or communicate with implants. Our customer's products include the first FDA-approved heart failure monitoring system, modeling tools for complex brain activity, CPAP machines and flexible endoscopes. A specific area of focus for us is in robotics, specifically prosthetics. We have been involved in a number of projects that developed fully functionally partial and complete prosthesis for amputees.

Amir Davoud

Shaughnessy: How is fabricating a medical PCB different than building any other high-reliability board?

Davoud: At Innovative, high reliability is a requisite for the majority of our customers. In addition to the medical industry we service others with challenging high end needs. These include defense and aerospace, and needless to say no one wants a failure at 35,000 feet, let alone on the operating table. In order to meet the demands of our clients, we are required to make a full commitment that ensures repeatability and reliability by maintaining operational excel-

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lence. This begins with laying a solid foundation where every project receives a detailed review that includes recommendations for manufacturability, design integrity and material requirements. From there, we use highly trained technicians that guide each design through a fully traceable fabrication process. Multiple inspection points are also used during this procedure to ensure design adherence at all stages. Once completed, each board undergoes a thorough final inspection and testing process before being shipped.

***Shaughnessy:* I know you all do quite a bit of flex. Are the boards for medical devices primarily flex, rigid, or rigid-flex?**

Davoud: We see an equal amount of each type, though there has been growth in the flex and rigid-flex segments over the past few years. This can be attributed to the increase in robotics and devices that have repetitive movement requirements. In 2016, I anticipate that we will see flexible circuitry requirements surpass rigid needs for medical devices.

***Shaughnessy:* The medical electronics field is so heavily regulated. What sort of "hoops" do you have to jump through, such as certifications and standards, to fabricate medical PCBs?**

Davoud: This industry may present the biggest challenges out of any we work in. FDA regulations place logical limits on materials that can be used in implanted devices as well as requiring strict adherence to approved builds overall. This places great importance for us to work on the design in its infancy as we often see some advanced projects with little wriggle room and repeatability concerns. The standards for devices vary. However, as we regularly build to IPC 6012, 6013 and 6018 Class 2/3, we qualify for most projects we see. There are some additional standards which may assist in qualifying including ISO 13485 certification, which compliments ISO 9001:2008, and is specifically for medical devices. In the end, the most critical requirement is having a fully traceable process that will ensure repeatability while allowing detailed tracking analysis in case of failures. That means we maintain rigorous records for every step starting with material allocation.

***Shaughnessy:* What trends are you seeing in medical PCBs?**

Davoud: In my opinion, the medical world is mirroring the electronics world. Devices are being made smaller, more portable, equipped with multifunctional capabilities and perhaps most importantly interoperability. That requires PCBs to have increased RF/microwave capabilities, fine-line technology, and high-density interconnects. The biggest challenge for board houses is to stay on pace or ahead of the technology requirements of the day. We manage this by reinvesting on average 10-15% of our annual revenue on technology advances. Over the past year, we purchased equipment that allows us to reduce space/trace, enhance our conductive via fill operations and virtually eliminate contamination. These trends also add "hoops" as discussed above; for example, RF capabilities also come with their own FDA guidelines which need to be met.

***Shaughnessy:* People seem to be living longer and longer. Do you think the medical segment will continue to grow?**

Davoud: That's a great question, and I think one is a derivative of the other. Advances in technology and treatment have directly impacted the length and quality of our lives. Over the past 150 years we have doubled life expectancy from 38 years to 76 years. Living beyond 100 years of age will become the norm for children born within the next generation. We will look to technology even more to sustain the health of our aging bodies and manufacturing will be called upon to support the increased heath care needs of a rapidly increasing population.

***Shaughnessy:* Thank you, Amir.**

Davoud: Thanks for the opportunity, Andy. **PCBDESIGN**

PCB007 Highlights

TTM Technologies Unveils Global Operating Model

TTM Technologies Inc. announced changes to its operating model that will create individual business units focused on customer end markets. Effective January 1, 2016, TTM's PCB segment will be comprised of three BUs: Communications and Computing; Automotive, Medical, Industrial and Instrumentation; and Aerospace, Defense, and Specialty. The Electro-Mechanical Solutions Segment will be a single BU.

IPC Standards Committee Reports—Component Traceability, Base Materials, Fabrication Processes, Assembly and Joining

IPC has released its standards committee reports from the 2015 Fall Standards Committee Meetings to help keep the industry up to date on IPC standards committee activities. The 2-19a Critical Components Traceability Task Group held its first face-to-face meeting to continue development of the working draft IPC-1782.

IPC Standards Committee Reports—Packaged Electronic Components, Flex Circuits, High-Speed/High-Frequency, Rigid Printed Boards

These standards committee reports from the 2015 Fall Standards Committee Meetings have been compiled to help keep you up to date on IPC standards committee activities. This is the third in a series of reports.

Flexible PCB: What's in a Name?

Flexible PCB is a common term that is synonymous with flexible circuits. While the term PCB is generally used to describe rigid printed circuitry, "flexible PCB" is a little contradictory because boards aren't really flexible. Some companies, like All Flex, design and manufacture flexible PCBs, but not rigid PCBs.

HKPCA & IPC Show 2015 Kicks Off in Shenzhen China

Barry Matties talks with Daniel Chan, executive director of the HKPCA, about the organization's expanded global outreach. They discuss what attendees can expect from this South China trade show that has become one of the biggest and most important shows in the PCB industry.

Catching up with Winonics' Mark Eazell

I have always thought of Winonics as one of the hidden gems of the North American PCB industry. Their well-equipped and well-laid-out facility in Brea, California is one of the more impressive looking PCB facilities in North America today.

AT&S Joins LEEN Network of Energie Steiermark

AT&S COO Heinz Moitzi is convinced of the purpose of this network and considers it a crucial lever to reduce energy consumption at AT&S even further: "For a globally producing industrial enterprise like AT&S, the reduction of energy consumption is of enormous economic and ecological importance.

Help IPC Persuade U.S. Congress to Extend the R&D Tax Credit

IPC has long urged the U.S. Congress to enact a permanent research and development tax credit—or at least a multi-year extension, not just the usual temporary, one-year deal—and to provide that certainty sooner, not at the last minute.

Data Analytics through Statistical Techniques

Many companies get caught in data traps. They focus so heavily on cost and survival that they end up using data as merely a marketing and sales tool. In doing so, they fail to realize the true power of data: It can transform every aspect of a business.

Conducting Very High Currents through PCB Substrates at High Ambient Temperatures

One of the major challenges of our time is climate change and the associated need to reduce greenhouse gas emissions. The requirement to reduce CO2 emissions has brought about significant changes in the area of power generation, and also in the area of mobility.

Plane Crazy, Part 2

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD AUSTRALIA

In my recent four-part series on stackup planning, I described the best configurations for various stackup requirements. But I did not have the opportunity to delve into the use of planar capacitance to reduce the AC impedance at frequencies above 1GHz, which is the region wherein bypass and decoupling capacitors dramatically lose their impact. In this column, I will flesh out this topic, and consider the effects of plane resonance on the power distribution network (PDN).

Figure 1 illustrates a 12-layer DDR3 board with six routing layers and six plane layers utilizing multiple technologies. This board must accommodate 40/80-ohm single-ended/differential impedance for DDR3, 90-ohm differential USB, and the standard 50/100-ohm digital impedances all on the same substrate. In order to reduce the layer count, it is important that these different technologies share the same layers. Plus, one needs to manage the return current paths and broadside coupling of the stripline configurations—quite a challenge!

The DDR3 matched delay signals are routed on the internal layers 3 & 4 and 9 & 10, which all use ground (GND) as the reference plane. To eliminate broadside coupling, the data lanes (eight in this case), differential strobes, and masks are routed on layers 3 & 4. And the adjacent traces are routed skewed or orthogonally. The address, control and command signals are routed together with the differential clock on layers 9 & 10. This separates the data lanes and address signals. Since DDR technology utilizes synchronous buses, the signals within the data lanes and within the address bus can be routed closely together, but the eight data lanes should be separated to avoid crosstalk.

UNITS: mil — 10/22/2015 — Total Board Thickness: 78.2 mil

Differential Pairs > 40 DDR3 SE | 50 SE | 80 DDR3 DIFF | 90 USB DIFF | 100 DIFF

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		PSR-4000 MH LPI (1GHz)	3.6	0.5							
1	8	Signal	Top Layer	Conductive			2.1	4	6	0.56	52.66	80.64	
		Prepreg		370HR; 106; Rc= 73% (2GHz)	3.74	2							
		Prepreg		370HR; 106; Rc= 73% (2GHz)	3.74	2							
2		Plane	GND Plane 1	Conductive			1.4						
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4							
3		Signal	Signal Layer 1	Conductive			1.4	4	4	0.31	53.08	79.65	95.64
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8							
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8							
4		Signal	Signal Layer 2	Conductive			1.4	4	4	0.31	53.08	79.65	95.64
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4							
5		Plane	GND Plane 2	Conductive			1.4						
		Prepreg		370HR; 1080; Rc= 64% (2GHz)	3.89	2.8							
6		Plane	Internal Plane 3	Conductive			1.4						
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4							
7		Plane	Internal Plane 4	Conductive			1.4						
		Prepreg		370HR; 1080; Rc= 64% (2GHz)	3.89	2.8							
8		Plane	GND Plane 5	Conductive			1.4						
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4							
9		Signal	Signal Layer 3	Conductive			1.4	4	4	0.31	53.08	79.65	95.64
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8							
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8							
10		Signal	Signal Layer 4	Conductive			1.4	4	4	0.31	53.08	79.65	95.64
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4							
11		Plane	GND Plane 6	Conductive			1.4						
		Prepreg		370HR; 106; Rc= 73% (2GHz)	3.74	2							
		Prepreg		370HR; 106; Rc= 73% (2GHz)	3.74	2							
12		Signal	Bottom Layer	Conductive			2.1	4	6	0.56	52.66	80.64	
		Soldermask		PSR-4000 MH LPI (1GHz)	3.6	0.5							

Figure 1: A 12-layer DDR3 stackup using Isola 370HR 2GHz material.

PLANE CRAZY, PART 2

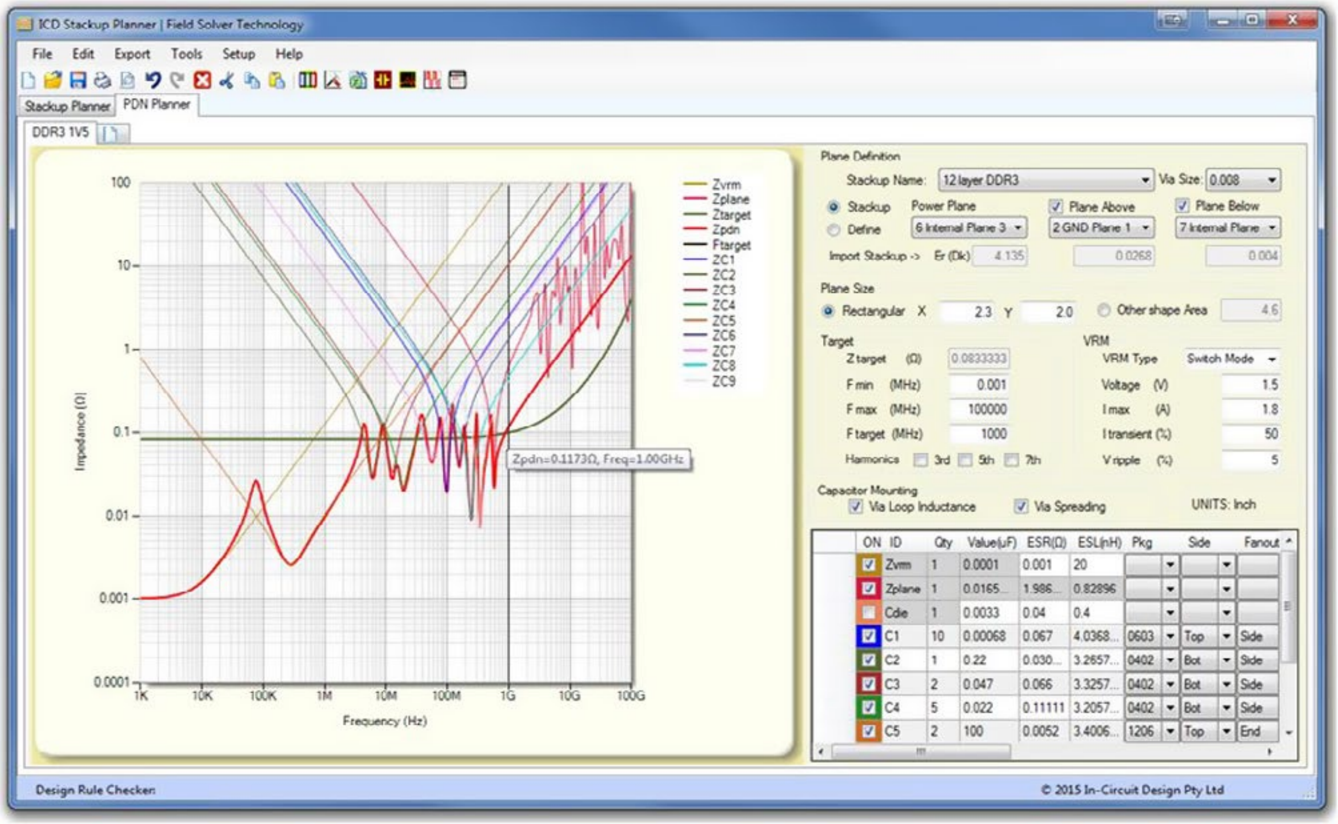


Figure 2: DDR3 PDN with low impedance up to 1GHz.

As you can see, there are four planes in the center of the board, two power and two ground. This is where tight coupling, between adjacent planes, can be utilized to add planar capacitance at low cost and dramatically reduce the AC impedance at the high end. There are thin sheets of Isola 370HR 1080 prepreg (2.8 mils thick) between both planes pairs.

Given the effects of the capacitors equivalent series inductance (ESL) and mounting inductance, the added planar capacitance still reduces the overall impedance to approximately the target impedance up to 1GHz as in Figure 2. Now, this is not easy to do using standard stackups.

With the continuous trend to smaller feature sizes and faster signal rise times, planar capacitor laminate (PCL), also known as embedded capacitor material (ECM), is becoming a cost-effective solution to further improved power integrity. This technology provides an effective approach for decoupling high-performance ICs whilst also reducing electromagnetic interference.

Plane pair cavity resonances contribute to emissions. Smaller plane separation implies less area of equivalent magnetic current at the plane pair edge, or equivalently less local fringing field volume, and therefore lower emissions for a given field strength. However, the smaller the plane separation, the higher the Q of the cavity can be, implying a higher field strength at the plane pair edges.

Embedded capacitance technology allows for a very thin dielectric layer (0.24–2.0 mil) that provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1GHz. Unfortunately, standard decoupling capacitors have little effect over 1GHz and the only way to reduce the AC impedance of the PDN above this frequency is to use ECM or alternatively die capacitance. These ultra-thin laminates replace the conventional power and ground planes and have excellent stability of dielectric constant and dielectric loss up to 15GHz. The thinner layers of ECM, also significantly reduces the capacitor mounting inductance.

The ZBC-2000™ laminate is constructed using a single ply of either 106 or 6060 style prepreg, yielding a dielectric thickness after lamination of 2 mils when measured by cross sectioning. The ZBC-1000 technology results in a 1 mil dielectric distributed capacitance material. FaradFlex™ and Interra™ buried capacitance products utilize a durable resin system for non-reinforced dielectrics for 1mil thickness and below. This also eliminates the skew associated with the fiber weave effect in standard materials. Also, with a product range up to 20nF per square inch in capacitance density, 3M ECM is the highest capacitance density embedded capacitance material on the market.

These ultra-thin laminates allow a significant layer count reduction in PCBs with better signal performance. Having a low dielectric constant, combined with very high withstanding voltage, these glass-free films change the design rules for via diameter and trace width, while still conforming to the manufacturing needs of the Fab shop. Three traces between vias, at a 0.4 mm pitch, are not only possible but very manufacturable according to Integral Technology.

It is a common belief that solid power and ground planes act as a large, perfect, lumped element capacitor. However, they actually encompass a distributed system of surprising complexity. The distinction between a lumped element and a distributed system involves the relationship between the time delay of the system and the rise-time of the signals.

For instance, for a PCB of six square inches, the signals entrapped between the VCC and GND planes create a standing wave, resonating as they reflect from side to side, and have a delay time of about 1ns. If the rise time of the signal is 5ns, the lumped condition is satisfied. However, with a much faster rise time or if the DDR3 plane is very small (typically one inch square), then the driver perceives the VCC and GND structure as a distributed object with significant delay.

This delay causes a couple of issues:

1. During the rising and falling edge, only the portion of the planes and decoupling capacitors located within the close vicinity of the driver can react before the edge has vanished. This frequently results in the noise spike being larger than anticipated.

2. The residual PDN noise from the first event reflects like an unterminated transmission line a couple of ns later, back to the driver. If at that precise moment, the driver switches a second time, both pulses (first and second) are superimposed. If the phases add and the driver has a repetitive pulse (as clocks do), the reflected pulse may build significantly.

One could possibly avoid this potential failure by comparing the round-trip delay across the plane, in question, to the clock period. If it is close, then an adjustment in plane size may be an appropriate solution. This may not eliminate all plane resonances but can serve to shift the resonances to other frequencies. Also, adding stitching vias, in appropriate locations, can reduce the extent that signal energy spreads through the plane cavity, and raises the frequency of structural resonances.

Manufacturer	Material	Description	Thickness (mil)
3M	ECM	Embedded Capacitance Material (ECM)	0.24, 0.47, 0.55
DuPont	Interra HK04	Ultra-thin laminate	0.5, 1.0
Integral Technology	Zeta Bond	High Tg Epoxy-Based adhesive film	1.0, 1.5, 2.0
Integral Technology	Zeta Lam SE	Low CTE C-stage dielectric with a Hi Tg	1.0
Integral Technology	Zeta Cap	Hi performance polymer coated copper	1.0
Oak-Matsui Technology	FaradFlex	Planar capacitor	0.31,0.47,0.63,0.94
Sanmina	ZBC1000	Buried Cap, hi-performance decoupling	1.0
Sanmina	ZBC2000	Buried Cap, hi-performance decoupling	2.0

Table 1: Embedded capacitor materials available in the ICD Dielectric Materials library.

PLANE CRAZY, PART 2

The worst-case noise response of a PDN is formed when a long, slow oscillation is followed by a short, fast oscillation. This phenomenon is referred to as a 'rough wave' and in extreme cases can cause total system failure. The long and slow oscillation is the clock and its odd harmonics, while the short and fast oscillation is due to the high-frequency plane resonance peaks. This is similar to an oceanographic 'rogue wave' phenomenon that is formed when a sudden quick wave hits a long, slow wave.

The ICD PDN Planner displays this plane resonance effect in Figure 2 and the projected EMI in Figure 3 (the red line represents the FCC Class B limit). Although the current EMC limits are only defined to 1GHz, one could assume that these will one day be increased to cover the entire bandwidth. The EMI plot represents the projected maximum radiated noise if a high-speed signal excites the plane resonance at a particular frequency.

If the plane size is increased, then the plane resonance is typically reduced. A combination of modifications to dielectric thickness and dielectric constant of the material in the ICD Stackup Planner, together with an adjustment of plane size, can usually establish the minimum resonance for the configuration. One should also ensure that the resonance peaks do not occur at the odd harmonics (red dotted vertical line), which tend to further radiate.

In conclusion, multiple planes are essential for high-speed design. But, one needs to select the right configuration to manage all of the diverse technologies, return current paths, broadside coupling and multiple power supplies requirements in order to achieve a high-performance, reliable product. Ensuring planes do not resonate, with the clock period, and that slow and fast frequency resonances do not combine will help avoid that dreaded 'rough wave' phenomenon. Power integrity issues generally manifest themselves as intermittent problems, which are otherwise difficult to nail.

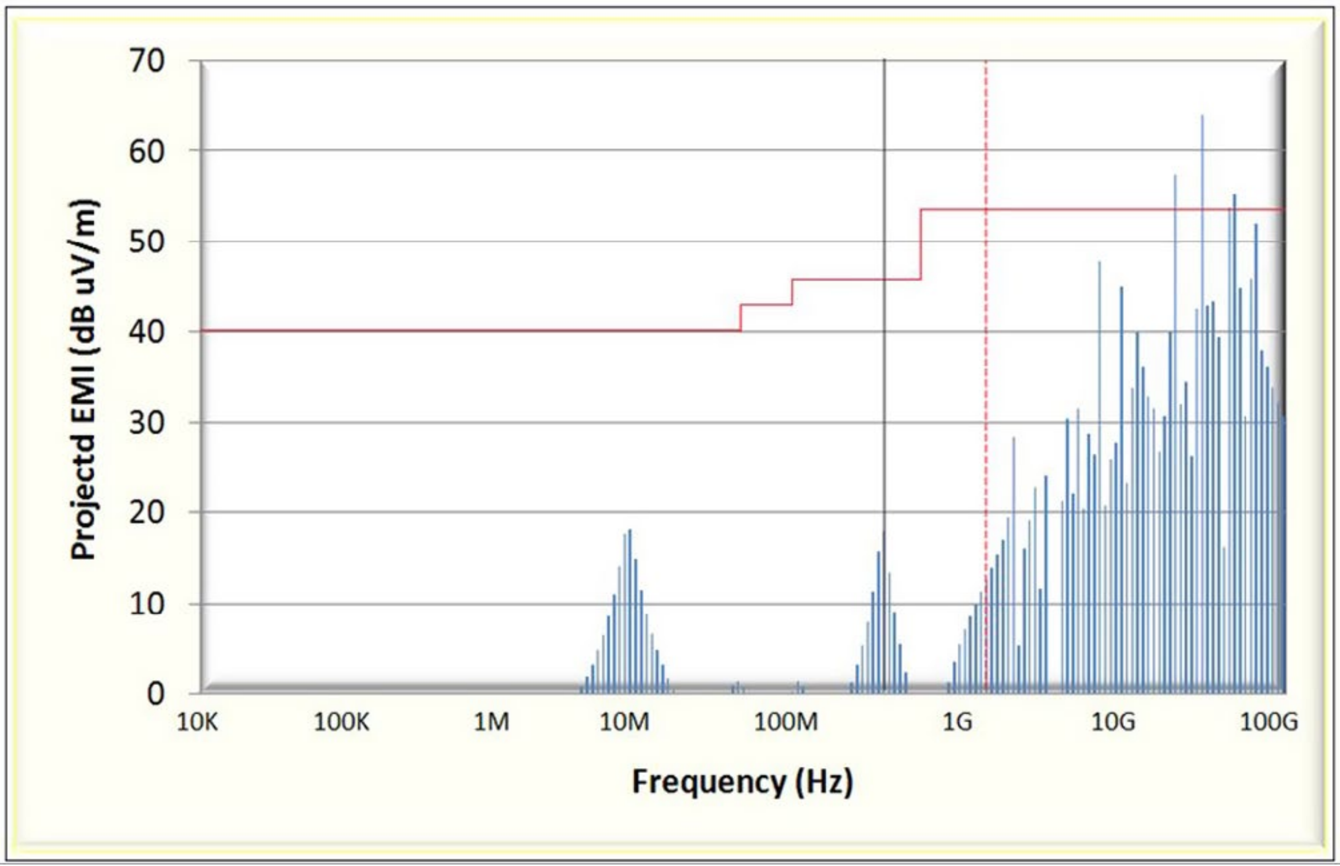


Figure 3: Projected PDN EMI.

Points to Remember:

- Tight coupling between adjacent planes can be utilized to add planar capacitance and dramatically reduce the AC impedance at the high end.
- Planar capacitor laminate, also known as embedded capacitor material, is becoming a cost-effective solution to further improved power integrity.
- Solid power and ground planes encompass a distributed system of surprising complexity.
- A distributed system involves the relationship between the time delay of the system and the rise-time of the signals.
- During the rising and falling edge, the local planes and decaps cannot react before the edge has vanished. This frequently results in a large noise spike.
- Repetitive pulse clocks tend to superimpose and build significant peaks.
- Avoid potential failure by comparing the round-trip delay across the plane, to the clock period.
- A "rough wave" is formed when a long, slow oscillation is followed by a short and fast oscillation.
- A combination of modifications to dielectric thickness and dielectric constant of the material in the ICD Stackup Planner, together with an adjustment of plane size, can usually establish the minimum resonance for the configuration. **PCBDESIGN**

References

1. Barry Olney's Beyond Design columns: No One-Way Trips, The Dumping Ground, Losing a Bit of Memory, Stackup Planning Parts 1-4, Material Selection for SERDES Design.

2. Henry Ott: Electromagnetic Compatibility Engineering

3. Howard Johnson: High-speed Signal Propagation

4. Masanori Hashimoto and Raj Nair: Power Integrity for Nanoscale Integrated Systems

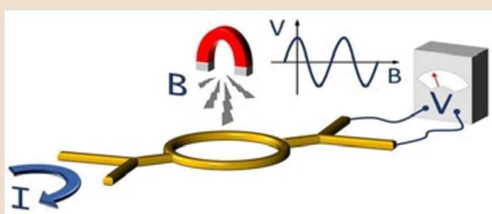
5. The ICD Stackup and PDN Planner: www.icd.com.au

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

Spooky Interference at a Distance

Nanotechnologists at the University of Twente research institute MESA+ have discovered a new fundamental property of electrical currents in very small metal circuits. They show how electrons can spread out over the circuit like waves and cause interference effects at places where no electrical current is driven. The geometry of the circuit plays a key role in this so called nonlocal effect. For designers of quantum computers it is an effect to take account of.

Interference is a common phenomenon in nature and occurs when one or more propagating waves interact coherently. Interference of sound, light or water waves is well known, but also the carriers of electrical current—electrons—can interfere. It shows that electrons need to be considered as waves as well, at least in nanoscale circuits at extremely low temperatures.



The researchers have demonstrated electron interference in a gold ring with a diameter of only 500 nanometers. One side of the ring was connected to a miniature wire through which an electrical current can be driven. On the other side, the ring was connected to a wire with a voltmeter attached to it.

Now the researchers have discovered a new way to affect the dynamical nonlocality. Understanding this fundamental effect is important for future quantum information processing.

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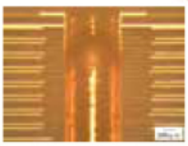

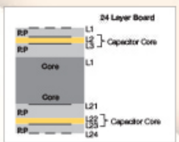

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How to Design a PDN for the Worst-Case Scenario

by Istvan Novak
ORACLE

The target impedance concept implicitly assumes that the largest possible PDN voltage-noise amplitude will be the product of the largest PDN-impedance in the relevant frequency range, and the corresponding maximum current-draw amplitude. Therefore, the maximum noise amplitude presumably could be contained below a target level by assuring that the PDN impedance is below a target value at all frequencies.

However, it turns out that this assumption is true only if the PDN impedance is flat/uniform across all relevant frequencies. If there is variation of the PDN-impedance with frequency, then the largest PDN voltage-noise amplitude can be much larger than the product of the current-draw amplitude and the largest PDN impedance. In my December 2015 column [1], we showed that for linear and time invariant (LTI) systems, the reverse pulse technique is a simple, fast, and guaranteed way to obtain the worst-case transient PDN noise (i.e., the maximum-amplitude "rogue wave").

In this column, we will show how the voltage-noise amplitude can be a function of the number of peaks in the PDN-impedance profile, and of the magnitude of variation in PDN impedance between different frequencies.

As a starting point, we briefly summarize here what we learned in the previous column. We used a circuit from [2], shown in Figure 1, with the impedance profile shown in Figure 2. This circuit has three anti-resonance peaks: 67 kHz, 1 MHz and 51 MHz. The resonance peaks all have approximately 100 mOhm impedance magnitudes. These peaks are clearly visible not

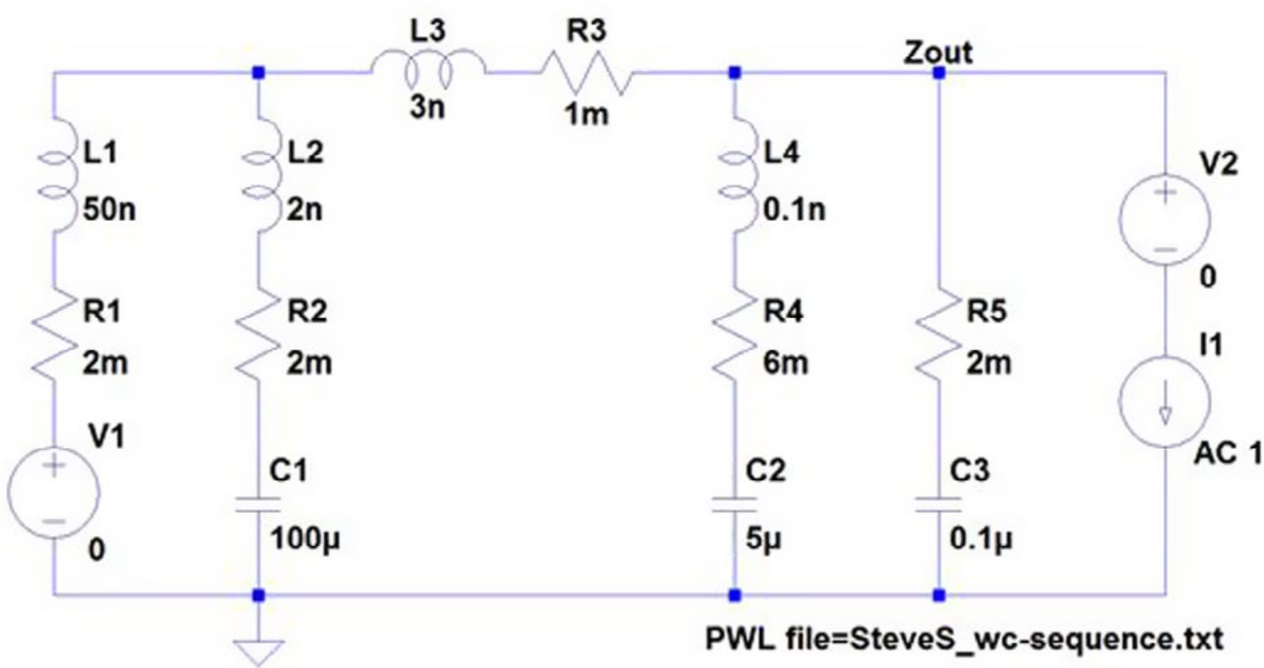

Figure 1: Rogue wave example circuit [2].

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HOW TO DESIGN A PDN FOR THE WORST-CASE SCENARIO

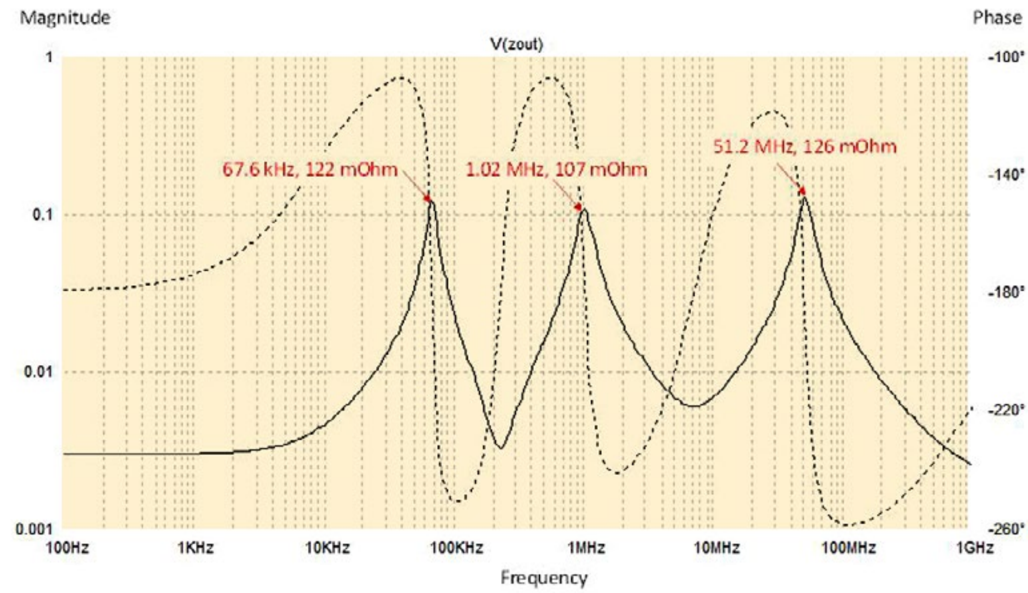

Figure 2: Impedance magnitude and phase from the circuit shown in Figure 1. Note that both axes are logarithmic; in particular, the frequency scale is logarithmic to clearly show the resonance peaks separated by three orders of magnitude.

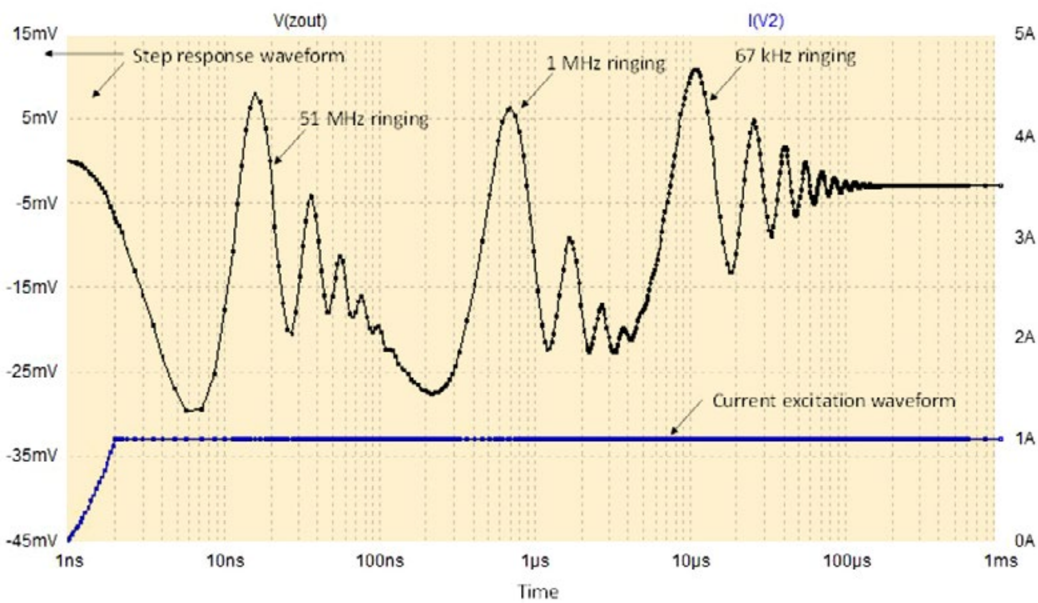

Figure 3: Simulated step response of the circuit shown in Figure 1. Vertical axis is linear, the horizontal axis is logarithmic.

only on the impedance plot, but also on the step response plot in Figure 3, we just need to switch the horizontal scale to logarithmic.

From the step response, we can apply the reverse pulse technique and get the absolute worst-case transient noise, 391 mVpp, which is shown in Figure 4. The step response has a peak deviation of 29.6 mV, which together with the 3mV DC steady state response on the 3 mOhm DC resistance creates a 56.2 mVpp worst-case

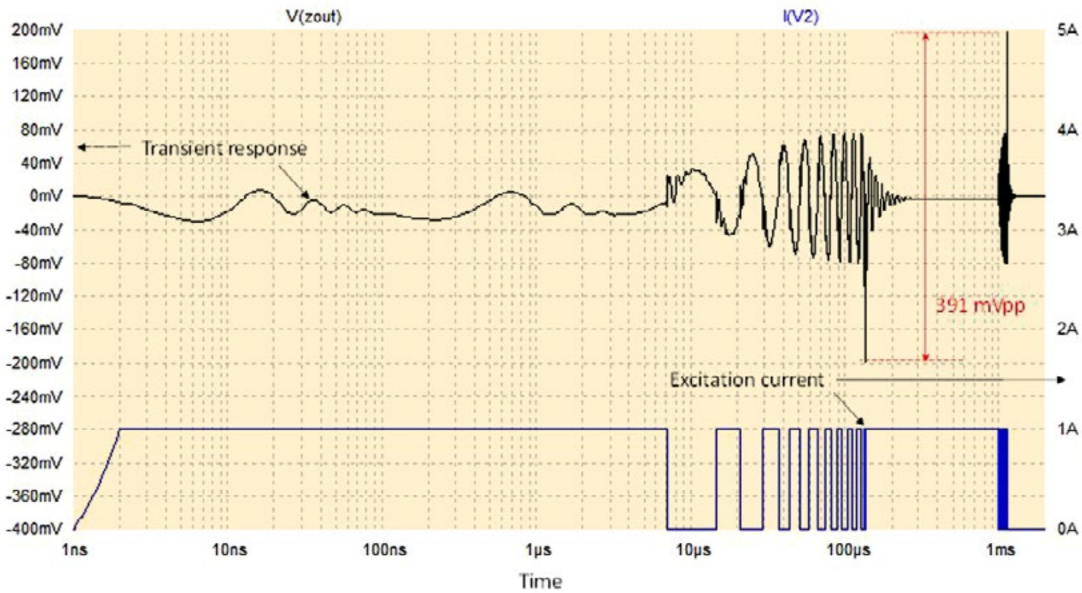

Figure 4: Worst-case response simulated with an excitation sequence calculated from the reverse pulse technique.

noise estimate. We get this amount of noise when a positive-going 1A current step is followed by a 1A negative-going current step with sufficient time between the two current steps so that the response can settle to its steady state before the next step arrives. In contrast, from the straight target-impedance calculations we would expect 100 mV noise.

In the worst case, however, when the positive and negative-going 1A current steps can hit the circuit in any arbitrary sequence, the reverse pulse technique in Figure 4 predicts a 391 mVpp maximum noise, more than six times higher than what we get from the peak deviation of the step response.

In this column we will look at a few further cases illustrating what happens when we have different degrees of "non-flatness."

When we have a linear network, the excitations and the impedance profiles can be scaled, so it does not matter what impedance target we use for the illustrations. For the sake of simplicity and consistency, we will use a 100 mOhm impedance target and for all examples we will make sure that within the bandwidth of the excitation, the impedance does not exceed this limit.

Figure 5 shows the impedance profiles of four cases. We start with a single peak at 0.1

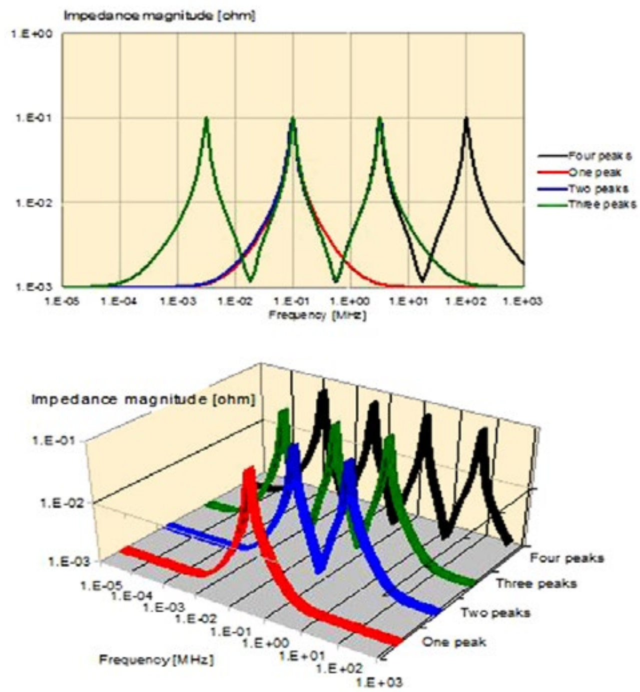

Figure 5: Impedance profiles with one, two, three and four distinct peaks, all reaching exactly 100 mOhm values. The top and bottom plots show the same data: In the top chart, we can better see that all four peaks reach exactly 100 mOhm values. The bottom chart shows better how the peak frequencies in the four cases relate to each other.

MHz. A second peak is added at one and half decade higher, at 3.16 MHz, also with exactly 100 mOhm peak value. The third peak is added one and half decade below the first resonance, at 3.16 kHz. Finally a fourth peak is added at one and half decade above the second peak, at 100 MHz. Note that at very low and very high frequencies the impedance settles at 1 mOhm, 1% of the peak value. The one-and-a-half decade separation between the peaks allows the impedance magnitude to drop substantially in between, close to the 1 mOhm asymptote values.

Figure 6 shows the step response of each of the four cases. Note that the horizontal scale is logarithmic to accommodate the ringing of widely differing frequencies. All four cases have impedance profiles not exceeding a 100-mOhm target value, so by ignoring the non-flatness of

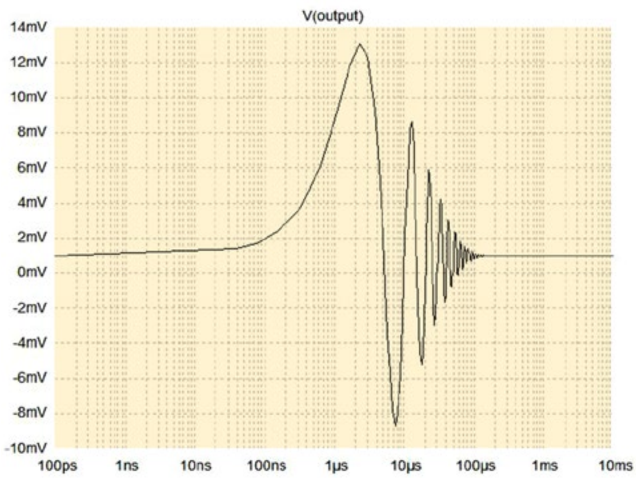

Figure 6a: Step response with one 100 mOhm peak. Worst-case transient noise from the reverse pulse technique is 120 mVpp for each ampere of excitation.

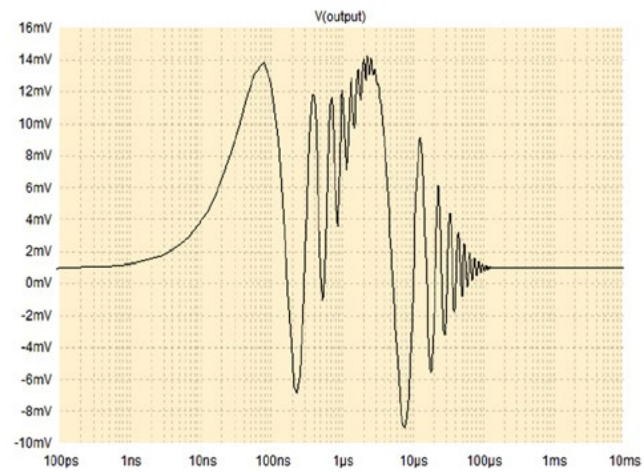

Figure 6b: Step response with two 100 mOhm peaks. Worst-case transient noise from the reverse pulse technique is 234 mVpp for each ampere of excitation.

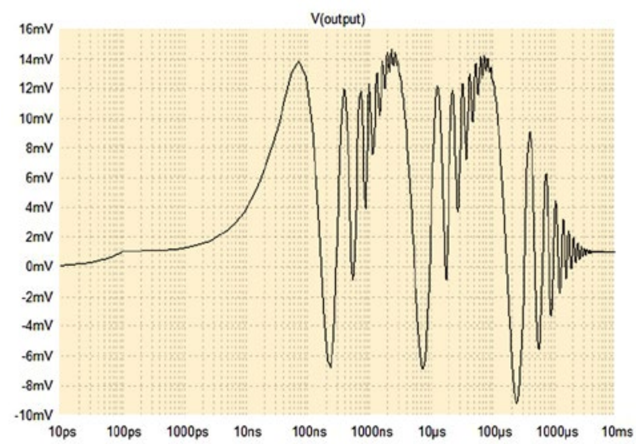

Figure 6c: Step response with three 100 mOhm peaks. Worst-case transient noise from the reverse pulse technique is 346 mVpp for each ampere of excitation.

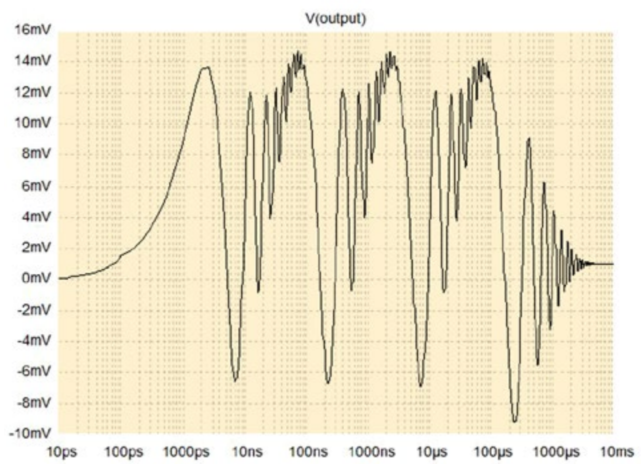

Figure 6d: Step response with four 100 mOhm peaks. Worst-case transient noise from the reverse pulse technique is 453 mVpp for each ampere of excitation.

the impedance, one would expect 100 mVpp worst-case transient noise. Instead, based on the reverse pulse technique, we get 120, 234, 346 and 453 mVpp worst case values. The biggest hit is the initial factor-of-two increase; as we showed [1], this happens because instead of a flat impedance starting at DC with the target impedance value, we start with zero (or very low) impedance and then continue with a flat target impedance at higher frequencies.

When we have just one dominant peak, reaching the target impedance at the peak, but having very low impedance at DC and at high frequencies, we create a the bandpass filter. This produces the worst-case noise when we repetitively hit this peak with a 50% duty cycle square wave. The bandpass filter picks out the fundamental harmonic from the square wave, creating a 4/PI times higher response.

As the number of resonant peaks increases in the impedance profile, the worst-case noise goes up. In the example shown here, the peaks are fairly well separated on the frequency scale, interacting only mildly. The small interaction reduces somewhat the worst-case peak noise from the pathological worst case of 120, 240, 360, 480 mVpp values that we get when the peak responses do not interact.

Next, we look at a single disturbance in a flat impedance profile. We use the same 100 mOhm target impedance as before and drive a deep second-order notch into it with three different Q values: 1, 3 and 10. Figure 7 shows the impedance profiles, Figure 8 shows the step responses. Note that all three responses reach a 1 mOhm minimum impedance at 1 MHz.

Interestingly, for a single disturbance in the impedance profile with the same maximum and minimum values, the worst-case transient noise does not depend on the Q of the notch. When we calculate the worst-case noise with the reverse pulse technique, we get 290 mVpp for all three cases. Figure 9 shows the actual worst-case time-domain response for the Q=10 case.

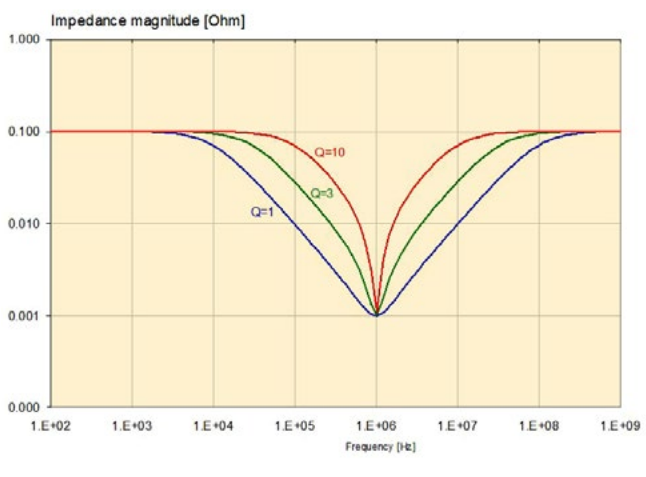

Figure 7: Flat impedance profile with a single second-order notch at 1 MHz frequency.

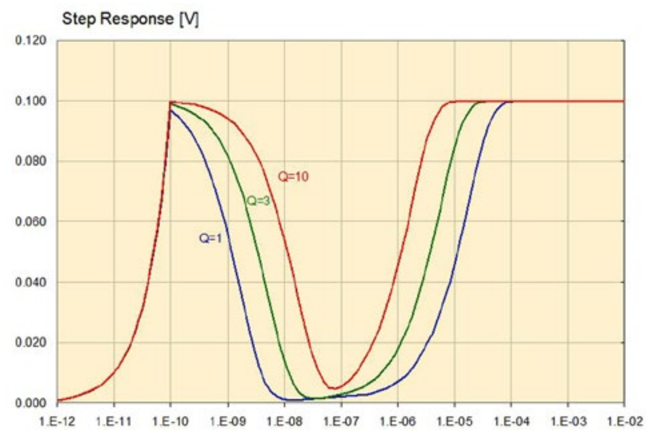

Figure 8: Step responses of circuits from Figure 7.

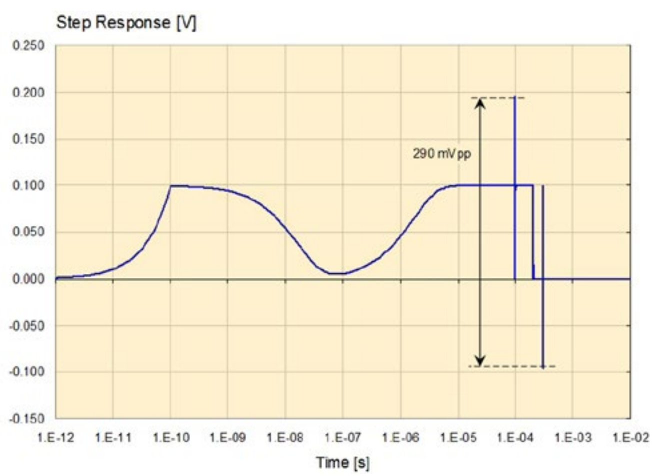

Figure 9: Worst-case transient peak-to-peak noise with 1A 100ps rise time step excitations. Q=10. Note the logarithmic horizontal scale.

Note the enormous increase of noise: From the 100 mVpp value for a perfectly flat impedance, the noise went up almost three-fold, even though we stay within the impedance target!

Lastly, we show the noise penalty as a function of notch depth. We already showed that the Q value is irrelevant, so we use an arbitrary Q=3 value and set the second-order notch to produce an impedance minimum at 1 MHz with a series of values between no notch (100 mOhm) and 1 mOhm. The impedance profiles are shown in Figure 10, the step responses are shown in Figure 11. The worst-case transient noise for 1A step excitations is shown in Figure 12.

Figure 12 clearly shows the penalty of a non-flat impedance profile: for small deviations it varies linearly and proportionally to the max/min impedance ratio.

For a single second-order notch with large deviations, the noise penalty saturates at about 3x. All the above means that very counter-intuitively noise goes up substantially even if we

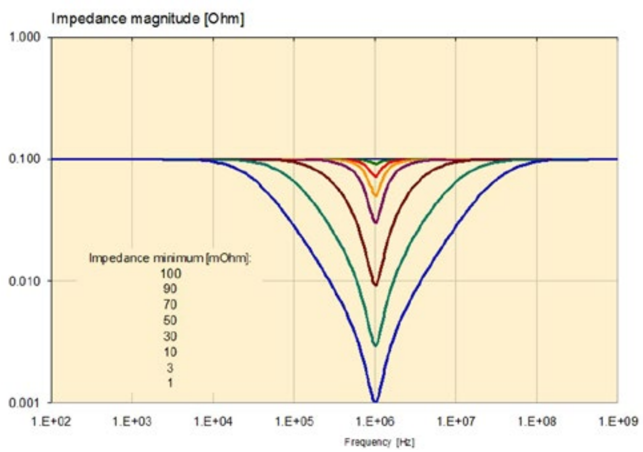

Figure 10: Magnitude of a flat impedance with a single second-order notch with different minimum values at 1 MHz.

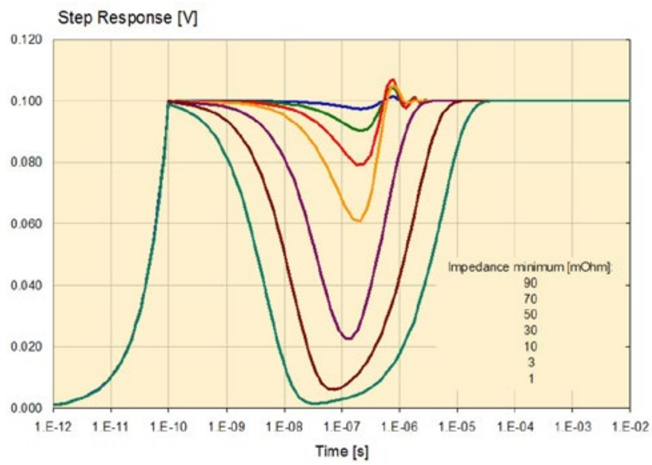

Figure 11: Step responses of the flat impedance profiles with a single second-order notch with various minimum impedance values from Figure 10.

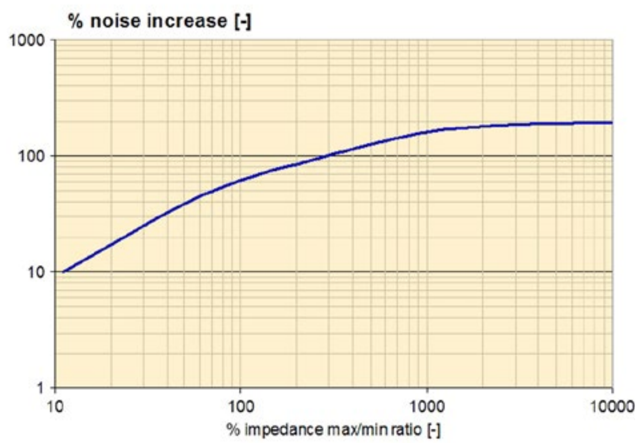

Figure 12: Relative noise increase as a function of relative max/min ratio of impedance profile on a flat impedance with a single second-order notch.

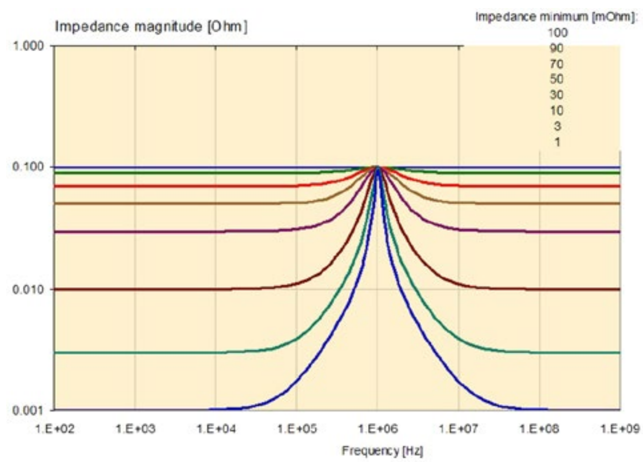

Figure 13: Magnitude of a flat impedance with a single 100 mOhm peak at 1 MHz with different minimum values.

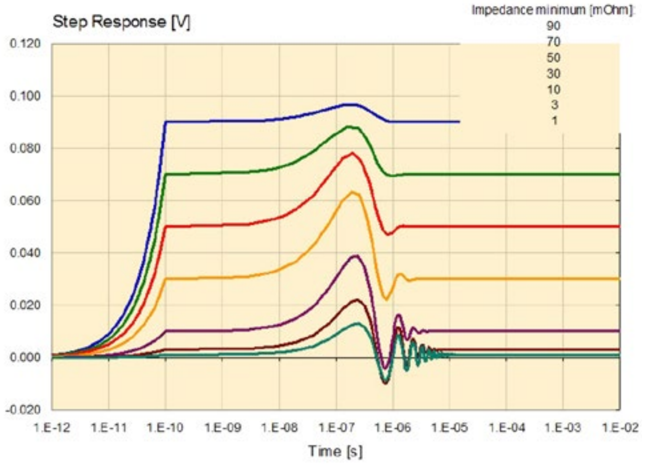

Figure 14: Step responses of the impedance profiles from Figure 13.

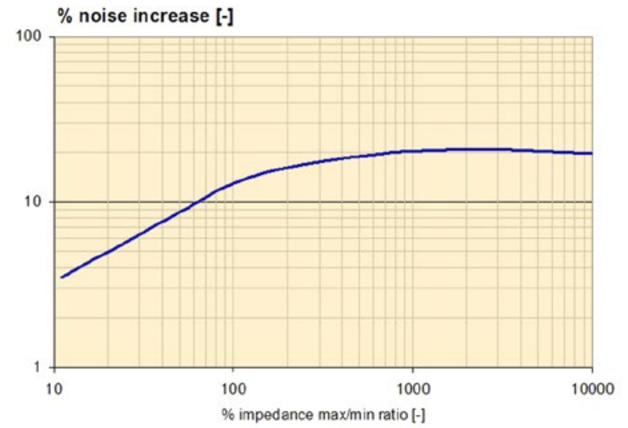

Figure 15: Relative noise increase as a function of relative max/min ratio of impedance profile.

just push the impedance down at certain frequencies, and even if we stay within the predefined maximum.

Lastly, we flip around the impedance profile and use one peak fixed at 100 mOhm maximum value, and we vary the value of low-frequency and high-frequency asymptotes. This essentially creates the inverse of impedance profiles we had in Figure 10; it was a band-reject function there, now we look at pass-band functions. Figure 14 shows the corresponding step responses. Finally, Figure 15 shows the percentage penalty as a function of max/min impedance ratio.

Note these cases do not intend to represent practical scenarios; they merely serve our better understanding. In practice it is very unlikely to have multiple impedance peaks or notches with the same extreme values. Nevertheless these examples serve as a guidance for the design process. If we use the target impedance approach and assume that, due to non-flatness, the worst-case noise is approximately three times higher, we can readjust our impedance target to a lower value and we can then do a straightforward design process. Once the design is known, it is always a good idea to recheck our assumptions with the actual PDN component values and placement and iterate as needed. If we lower the target impedance by a factor of three, very seldom will it be necessary to do iterations.

For more information on the subject, please see the reference section, especially [3] and [4]. **PCBDESIGN**

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3. Target Impedance and Rogue Waves, panel discussion at DesignCon 2016, January 19 – 21, 2016, Santa Clara, CA.

4. Jae Young Choi, Ethan Koether, Istvan Novak, “Electrical and Thermal Consequences of Non-Flat Impedance Profiles,” DesignCon 2016, January 19 – 21, 2016, Santa Clara, California.

Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of “Frequency-Domain Characterization of Power Distribution Networks.” To read past columns, or to contact Novak, click here.

A New Year and a Few Milestones

by Tim Haag
INTERCEPT TECHNOLOGY

I have a collection of circuit boards on the wall of my office (Figure 1). Some were given to me as a reference when I was re-working that design, while others were given to me as samples of what a particular company was doing. And then there are the boards that I personally designed that I was presented with as mementos of my work. But the design that I have the most pride in is a rustic chunk of wood with a handful of primitive components on it. Why is this so important to me? Well, it's because it is the first circuit board that I ever designed.

When I was a boy my parents gave me an electronic hobby board that allowed you to create different circuits by connecting wires to spring posts that were attached to different components. The instruction book taught you basic electronics as you created different projects, from a simple on/off switch for a light bulb to a rudimentary radio. And when you finished one project, you just pulled the wires off the spring posts and started the next one in the book.

After a while, I grew tired of building different projects and decided to make the most difficult design in the book a lot more robust by soldering all the pieces together. So I got busy ripping all the parts off the hobby board and planning out what I was going to do. Mounting the parts on something rigid seemed like a good idea so I took a flat, thin piece of wood and drilled holes for the parts. I then placed the parts and soldered everything together, and when I was done, surprise! It actually worked.

Even though I had never seen or heard of one before, I had without realizing it designed my first circuit board. And since I had used a chunk of wood as my PCB, this truly was a circuit "board." Come to think of it, this would

Figure 1: My collection of circuit boards.

also be my first foray into the world of circuit board fabrication, manufacture, DFM, quality control, and component engineering…but I'm getting ahead of myself here.

We've all seen mile markers alongside the road as we travel, but did you know that other than supplying a needed number or letter for the alphabet game to bored children in cars, that those little green markers actually have a real history to them? They originated in the Roman Empire, where they were originally stone obelisks made from granite, marble or other local stones. Since travel in those days was often no more than a few miles per day, having those milestones along the side of the road became an important method to measure the journey that you were on.

For us today the milestone is still a good way to chart our journey. When I created my circuit "board," I had no idea at the time that decades later I would begin a career as an actual circuit board designer. Laying out and connecting circuits as I had would eventually become a common everyday activity, albeit with a little more complexity involved.

> **"Laying out and connecting circuits as I had would eventually become a common everyday activity, albeit with a little more complexity involved."**

Without realizing it I had erected a milestone in my life. Not a turning point, but a marker that I can look back on to see the road that I have traveled in my career. But as I look in the rear-view mirror of my life, that first layout certainly isn't the only milestone that has marked my journey.

November 22 was my dad's birthday, and although he has been gone now for many years, my dad left a good many milestones in my life. Dad was an electrician's apprentice when he was young, and his stories about those days certainly created in me a great interest in the world of electronics.

But one of the great milestones that I got from my dad was his love of creating something out of nothing. Growing up during the Depression, he learned to scrounge and be creative in order to get the job done. My brother and I would hang on his every word as he told stories of the different projects that he had worked on. Everything from a (non-flying) airplane that was kludged together from parts from the junk yard (and there was a story there, too, about how the engine and propeller shook apart and the resulting shrapnel forced everyone to scatter for cover), to how he engineered a hose setup to go from the exhaust of their Model T down into the ground to smoke the gophers out. That same spirit showed me that if you need something done, you can probably figure out a way to accomplish it with a little imagination and hard work.

Dad also was a ham radio operator before and after WWII, and then went on to work at different radio stations and eventually became a television technician at KOIN TV in Portland, Oregon. The stories that he told about the early days of broadcast were mesmerizing; some I didn't even know about until after he died and his friends spoke at his funeral. Along with his ham radio buddies, Dad would experiment with bouncing radio signals off the moon in those days.

At the same time, he also used his radio skills in helping people to keep in touch with each other during Portland's Vanport flood of 1948. I also found out that he was considered one of the best in the business when it came to fine-tuning those original gigantic color TV studio cameras back in the 1960s.

The amazing thing is that he did all of these things without finishing high school. We would often catch him at home going through books to get up to speed on the latest in electronics and broadcast technology. The fact that he accomplished so much without finishing his formal education set a milestone of perseverance firmly in my mind.

Several times I have gotten jobs that I wasn't the most qualified, educated, or experienced for. And yet those who hired me saw something there and believed enough in me to help me to rise to the next level. This milestone of faith and commitment shown to me has been a tremendous inspiration as I have managed my own groups and mentored my employees.

There are milestones of character and integrity in my life that were set in place by those who refused to give in to the quick thrill of the moment, but instead continued on the right path, even though it may not have been the easiest path to take. I have milestones of charity and compassion in my life left there by people who took time out of their day to help others, often at the expense of their own needs. And the milestones of resilience and hard work have been set in place by those who refuse to back down in the face of adversity, but instead see the job through to the end. True, not all milestones are pleasant and some have real pain associated with them. But those are part of our journey too.

I am very fortunate to have these great milestones as I look back on my life. And now, as I write this, I once again glance over my shoulder at that silly little piece of wood with the simple components on it hanging from my wall, and I am grateful for the milestone that it represents in my life.

Is it possible that it is responsible for my career as a circuit board designer? Did creating that first layout instill within me the desire to one day create larger and more complex designs? I wonder. It is an interesting thing to contemplate. And thanks, Dad. The world has certainly changed from when you were born in 1919. Thanks for helping to prepare me for it.

How about you? When you glance back over your shoulder, what milestones do you see? **PCBDESIGN**

Tim Haag is customer support and training manager for Intercept Technology.

Switching on to Renewables

HSBC aims to source a quarter of the energy used to power its buildings around the world from renewable sources by 2020. It is a challenging goal but the bank has already signed four agreements with renewable energy providers in the UK and India, which together will generate the equivalent of 9 per cent of HSBC's global energy needs.

In the UK, HSBC has signed two agreements with renewable energy providers. The first is a 12-year agreement with a wind farm in the East of England.

HSBC has also signed a similar agreement with a second wind farm in the UK that will provide renewable energy from January 2016. Taken together these UK projects are expected to account for 40 per cent of HSBC's UK electricity requirements, helping the bank reduce its environmental footprint.

In India, a new solar plant in Hyderabad was built after HSBC agreed in 2014 to buy the plant's energy at a fixed price for 10 years. This project will generate enough equivalent clean energy to power four HSBC offices in the region and save up to 10,000 tonnes of carbon dioxide per year.

By signing these long-term agreements, rather than buying renewable energy from existing sources, HSBC is supporting developers to build new and additional wind and solar farms.

As well as using more renewable sources, HSBC is aiming to use less energy in the first place by improving the energy efficiency of its buildings. This is part of the bank's broader goal to manage the impact of its operations on the environment.

MilAero007 Highlights

New OEM Global Account Manager for Avionics & Automotive at Ventec International

Ventec International Group, a world leader in the production of polyimide and high-reliability epoxy laminates and prepregs, is delighted to announce the appointment of Tamara den Daas in the role of OEM global account manager with a focus on opportunities within the avionics and automotive markets.

Eltek Receives Orders worth $1.4M from Customers in India

Eltek Ltd. announced today that since the beginning of the fourth quarter, it has received several orders for military applications from customers in India, amounting to US$ 1.4 million in the aggregate. The majority amount of these orders is expected to be delivered to the customers during 2016.

Dymax White Paper Explains Switching from Conventional Lamp to LED Light-Curing Sources

Dymax Corporation's new white paper, "Ensuring Success When Switching from Conventional Lamp to LED Light Curing Sources," discusses topics such as how LED curing works, the advantages to LED curing, and getting enough information to switch successfully.

Future Batteries Could Charge in 30 Seconds

Future cell phones and other electronics could have batteries that charge in less than a minute. This new capability will be in part thanks to a space experiment using hard, flexible material as a clean power source.

Honeywell Paper Investigates Avionics Vibration Durability

Dr. Joseph Juarez, principal mechanical engineer at Honeywell International, discusses his SMTA paper, which addresses avionics vibration durability between tin-lead and lead-free solder, the years of testing he conducted, the importance of doing a good soldering job, and some of the surprising findings of his research.

i3 Electronics Earns 'Preferred Supplier' Status from Raytheon

i3 Electronics has earned this "Preferred Supplier" status by continuously delivering a high level of performance and value-add to Raytheon. Designation of this prestigious "Preferred Supplier listing" will allow i3 to work even more closely with Raytheon and their world-class team of engineers, scientists and problem solvers.

NASA's SOHO Celebrates 20 Years of Space-based Science

After 20 years in space, ESA and NASA's Solar and Heliospheric Observatory, or SOHO, is still going strong. Originally launched in 1995 to study the sun and its influence out to the very edges of the solar system, SOHO revolutionized this field of science, known as heliophysics, providing the basis for nearly 5,000 scientific papers. SOHO also found an unexpected role as the greatest comet hunter of all time—reaching 3,000 comet discoveries in September 2015.

The Opportunities for Plasma Processing

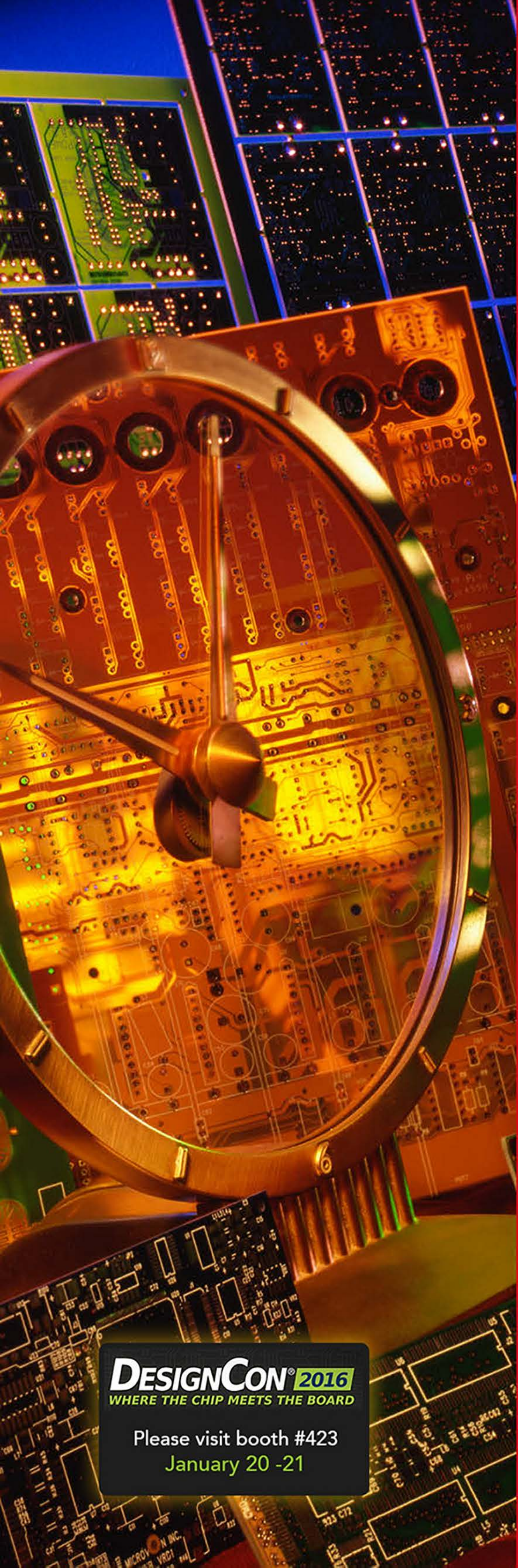
Pete Starkey interviewed Andre Bodegom, managing director of Netherlands-based Adeon Technologies B.V., about their long relationship with Nordson MARCH, typical applications for plasma equipment, and what the most challenging materials are from the point of view of plasma processing in the PCB industry.

Graphic Plc Wins BAE Systems Gold Award

The award recognises continued commitment and support to BAE systems programmes and key business objectives. The award reflects Graphic Plc's achievements in demonstrating sustained excellence in delivery and quality performance.

NASA Selects New Technologies for Parabolic Flights and Suborbital Launches

NASA's Flight Opportunities Program has selected eight space technology payloads for reduced gravity flights on board specialized aircraft and commercial suborbital reusable launch vehicles (sRLVs).



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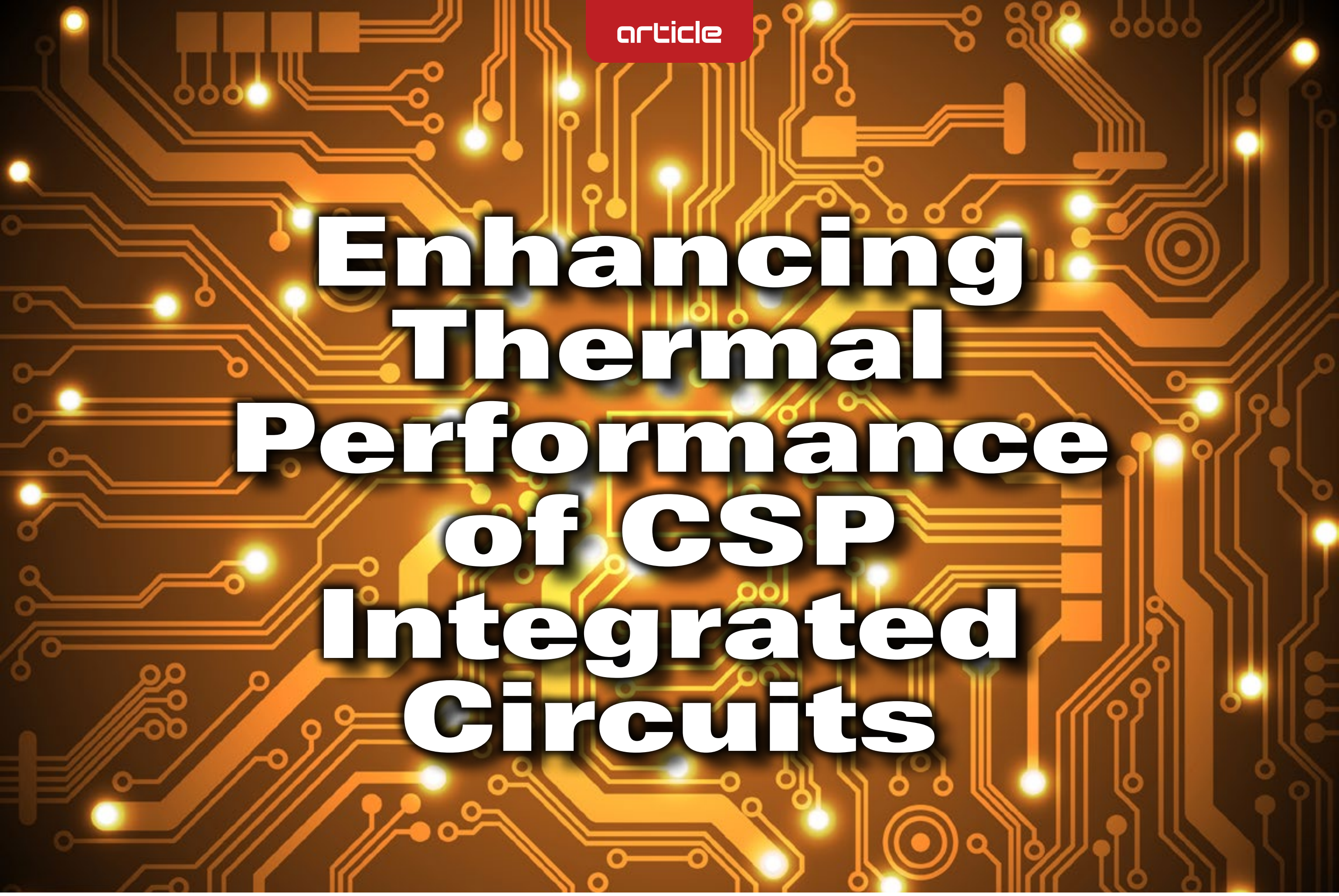

article

Enhancing Thermal Performance of CSP Integrated Circuits

by Nicholaus Smith
INTEGRATED DEVICE TECHNOLOGY

In the portable electronics market, power management integrated circuits (PMICs) are increasingly found being packaged into ball grid array (BGA) and chip scale packages (CSP) for their lower material costs, improved electrical performance (no bond wire impedances), and smaller form factors. These advantages do not come without compromise: The silicon die of CSPs are no longer in direct contact with large heat-spreading thermal paddles (E-PADs) used for electrical and thermal conduction.

This is the primary performance trade-off; because the IC substrate is not in contact with an E-PAD there is no high-conductivity direct thermal connection from the substrate to the heat-spreading copper planes on the PCB. This article will discuss PCB level methods that will lower the operating temperature of CSP devices by examining methods to transfer heat from the source and transport it to the ambient environment by lowering thermal resistance of the CSP IC. There are usually multiple ways to enhance the performance while simultaneously lowering the operating temperature that can be incorporated into new boards or revisions of existing boards.

In order to meet size and weight requirements, constraints of portable electronic designs often force PCB designers to reduce the size of components and PCB real estate area. To meet these demands, the use of CSP packages to shrink the PCB area needed is a common change in designs. As a result of the reduction of total PCB area, the available options to move heat and route high-power PCB traces is also reduced. Furthermore, the thermal performance cannot be matched when a QFN is compared to an equivalent CSP package; therefore, it is imperative that the PCB is designed to optimize heat transfer from the CSP to the PCB, which in turn dissipates it into the atmosphere. The parameter measuring the heat conductivity is the junction-to-ambient thermal resistance specification, Theta-JA (Θ_{JA} (˚C/W)).

Just for reference, to match the area utilized for heat transfer when connecting a typical QFN package E-PAD (3x3 mm square) to a CSP device

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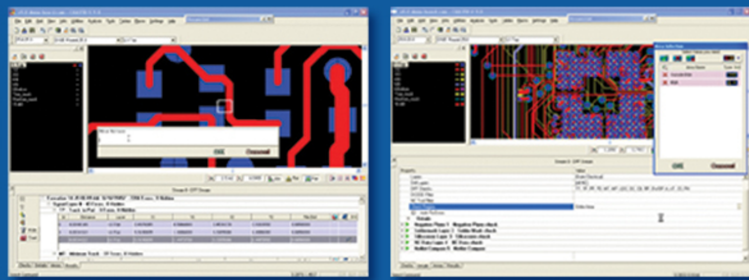

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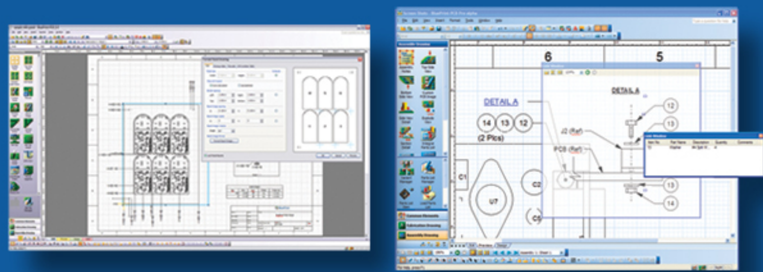

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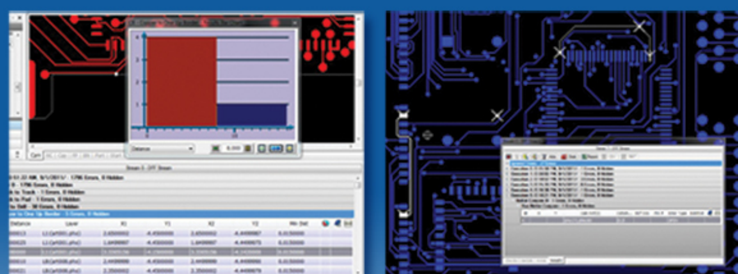

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with 0.4 mm pitch one would need to connect nearly 30 CSP pins to maintain an equivalent heat sinking capability based on the area of the E-PAD. Comparative Θ_{JA} datasheet values for the same silicon soldered to similar PCBs under identical electrical loading conditions can vary from 45˚C/W in CSP packages to 25˚C/W for equivalent QFN packages (reference data from the IDTP9023 Wireless Power Receiver) for well-designed PCBs. Such a difference means the CSP will operate at higher temperatures than QFN counterparts. As a consequence, thermal performance is typically only half as good when an IC is packaged in a CSP package compared to the QFN when both have identical power consumption. Thus CSP thermal performance can easily be more than twice as bad as an equivalent QFN if not properly compensated for with a well-planned PCB design.

The operating temperature of a packaged IC is determined by three factors: convection, conduction, and power burned by the IC to perform the electrical demands. When thermal analysis calculations are solved for CSP ICs using the thermal resistance parameters, it should be noted they are made using an estimate of the number of thermal vias connecting the IC to the PCB. Each connection creates a thermal path that can be used to direct heat away from the IC's semiconducting junctions. These estimates assume that the IC is mounted to a 3" x 4.5" solid copper four-layer PCB as defined by JEDEC standard 51. When a real application PCB is being designed, the area is usually much smaller, has cutouts and irregular form factors, many components, multiple vias, and electrical connections that will decrease the thermal performance relative to the JEDEC standard.

A common dilemma faced by the designer is the challenge of getting the heat developed in the IC to transfer from the device to the atmosphere through the PCB, with a minimum temperature drop in the thermal pathways.

In Figure 1, each pad connected to a component side trace and each thermal via-in-pad transfers heat from the silicon into the PCB copper planes. Design of the via-in-pad and the number of vias influence–the effectiveness of the heat path, as well as the surface area of copper that the vias are in direct contact with. The pitch of the IC under development will influence the size of the hole and proportionally the volume of copper available to conduct the heat (think of the via as a hollow heat-carrying copper cylinder) to the copper surfaces connected to the via (i.e., copper planes or traces). Additionally, after the vias-in-pad are built by electroplating, they will need to be filled with a material (non-conductive or conductive) prior to being resurfaced evenly for the installation of the actual CSP device.

The via fill material is "poured" into the hole and the packing ratio is usually optimized by the fabricator based on hole diameter. The conductive fill material used to back-fill the vias usually has higher electrical and thermal resistance than copper, so the fill material only has a small impact on thermal performance due to

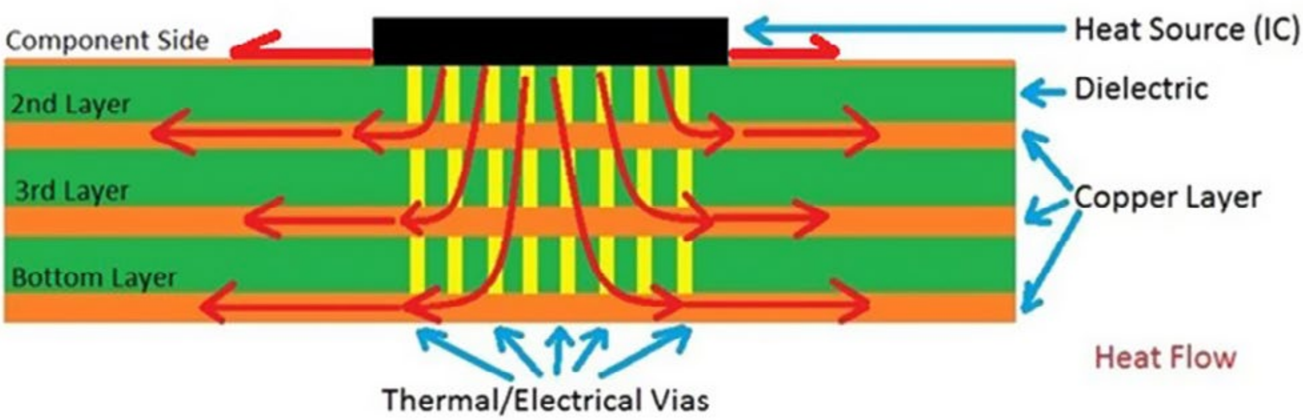


Figure 1: Cross-section of a PCB-mounted CSP package showing conduction thermal transfer.

the lower thermal and electrical resistance of the via-in-pad copper. Additionally, most conductive materials have higher thermal expansion coefficients than copper, which can cause via walls to rupture. For these reasons non-conductive fill is typically used in high-volume production, but as the state of the industry continues to evolve, conductive materials may begin to dramatically outperform non-conductive fill materials without the risk of yield losses.

According to first-order heat flow and thermal conduction, the primary influencing factors of heat flow from a source to a volume are the distance between source, the cross-section (copper in connection) and the temperature difference between the source and the volume [1].

$$H = kA \times \frac{\Delta T}{\Delta L}$$

Equation 1

In which H (Heat) = Q (heat flow)/Δt (seconds),
k (Watts/(meter*Kelvin)) = thermal conductivity of the material,
A (Area (m^2) = area of the cross-section perpendicular to the heat path,
ΔT (˚K) = difference in temperature from the IC to the adjoining copper surface, and
L(m) = length of the heat flow path

While this simple approximation may not appear to solve the current problem, it indicates that in order to transfer more heat, area should be maximized and the length of the path the heat flows through should be minimized. The important relationship for maximizing heat flow is the ratio of cross-section to length of the connecting copper to a surface, such as a copper plane.

In Figure 2, the vertical heat transfer is impacted by three parallel thermal resistances. Q_1 is the copper that is the wall of the via and it is the most effective at thermal transfer. Q_2 is

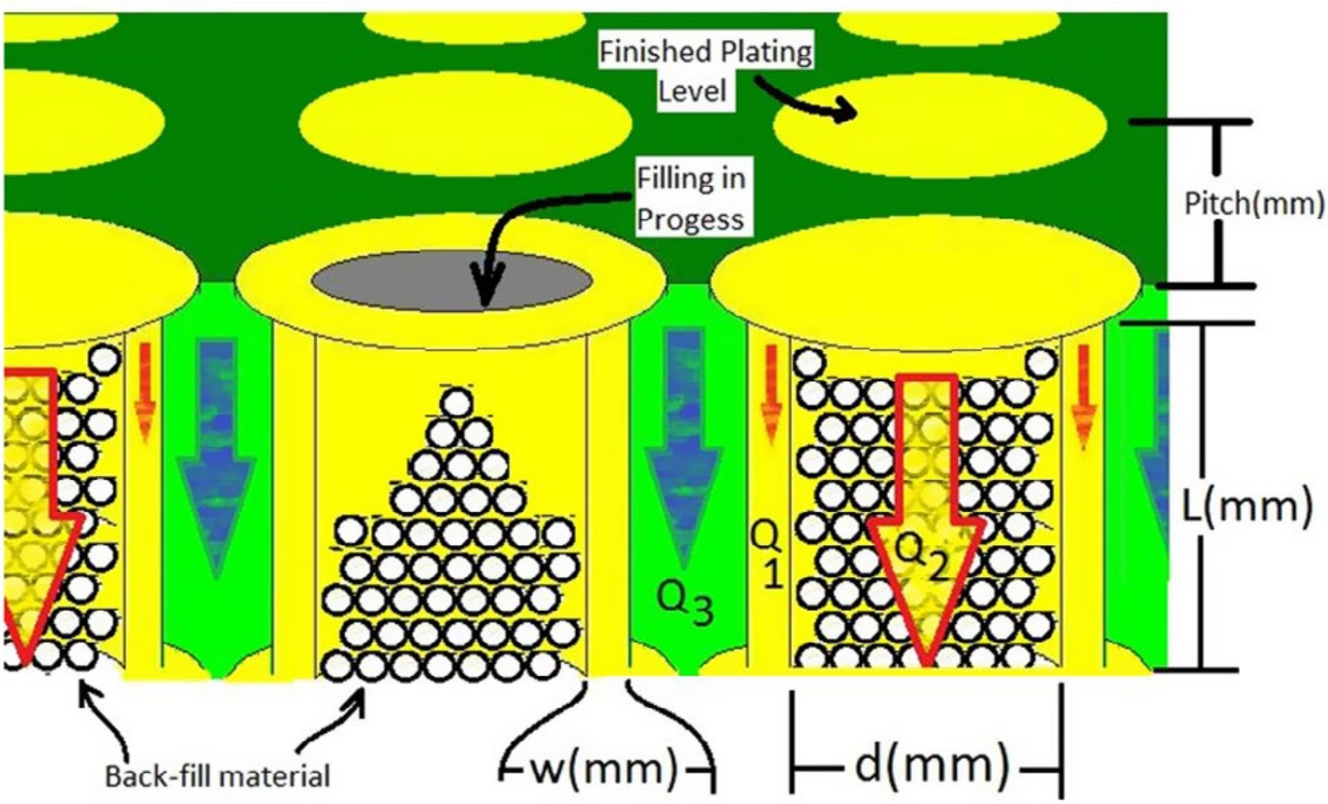


Figure 2: Heat flow paths from CSP device pins to PCB & via-in-pad fill materials.

the via-in-pad fill material, and Q_3 is the heat flow through the FR-4 material. Several methods to employ to optimize the flow of heat include making the via hole diameter (d) as large as possible to maximize the volume of copper that composes the via wall (solve for the volume of a cylinder). Attach as much copper as possible to as many vias-in-pad as possible on the inner layers and connect these vias to parallel layers to increase the connected volume of copper (each additional internal layer contacting the vias will increase the volume available to dissipate the heat into).

"Attach as much copper as possible to as many vias-in-pad as possible on the inner layers and connect these vias to parallel layers to increase the connected volume of copper (each additional internal layer contacting the vias will increase the volume available to dissipate the heat into)."

Once the via-in-pad reaches the layer that will be used to complete the electrical connection, widen the copper of the trace on the terminating layer as much as possible so that the developing heat will have copper to flow into and disperse. In a CSP package, the thermal resistance of the silicon substrate should be considered much lower than the thermal resistance of a via-in-pad that conducts from the component side of the PCB to any alternate layer; as a result, the CSP package will be approximately isothermal (give or take a few degrees) throughout its volume. Therefore, each CSP pin should be considered equivalently connected to the heat source and capable of transferring the same amount of heat from the IC even if the signal of the pin conducts little current or is not physically located near a heat-generating source inside the IC.

With this concept in mind—that each CSP pin is capable of transferring an equal amount of heat if connected to similarly sized copper shapes—every connection to every CSP should be completed using the maximum area of copper plane or trace that is as thick as possible (i.e., 2 oz. Cu weight vs. 1 oz.) to improve the heat-sinking ability of the board.

Figure 3 shows the third layer of the PCB from the component side of the board, and each via-in-pad has the surface area of the copper connected and maximized regardless of the electrical current the trace conducts. The only traces that are left "thin" are those that are not in contact with a via-in-pad directly connected to the IC. These can be identified by the larger-diameter holes (grey circles) verse the much smaller diameter of the via-in-pad located under the CSP footprint (small diameter forced due to the 0.4 mm IC pin-to-pin pitch) which only allows for 0.254 mm (10 mil) pad and a 0.127 mm (5 mil) diameter (d, from Figure 2) via-in-pad. In this example layout, the signals for /ENABLE, TS, FOD2 will carry, at most, less than a micro-amp of current each, but the traces are purposely widened in order to take advantage of the heat-carrying capacity of the connection to the via-in-pad connected to the CSP package.

Reconsidering Equation 1, the heat flow is influenced by the distance (L) from the heat source to a heat-spreading plane or layer. Simple examination of thermal conductivity values for copper and FR-4 will prove that copper (thermal conductivity) is superior at transferring heat compared to FR-4 (thermal conductivity); however, when the distance (L or thickness of the dielectric) is much smaller compared to the area (L<<A), heat flow across the dielectric (such as from 1 copper layer to the next) is reasonable from a heat dissipation point of view even though the FR-4 is considered a thermal insulator.

For example, imagine a heated cookie sheet with 20 sheets of paper (thermal insulator) placed on top. If you pressed your hand on the top of the papers, after several moments, chances are that you will barely feel any heat, even if the cookie sheet was still in contact with a hot stovetop burner; however, if you tried this with a single sheet of paper, your hand would

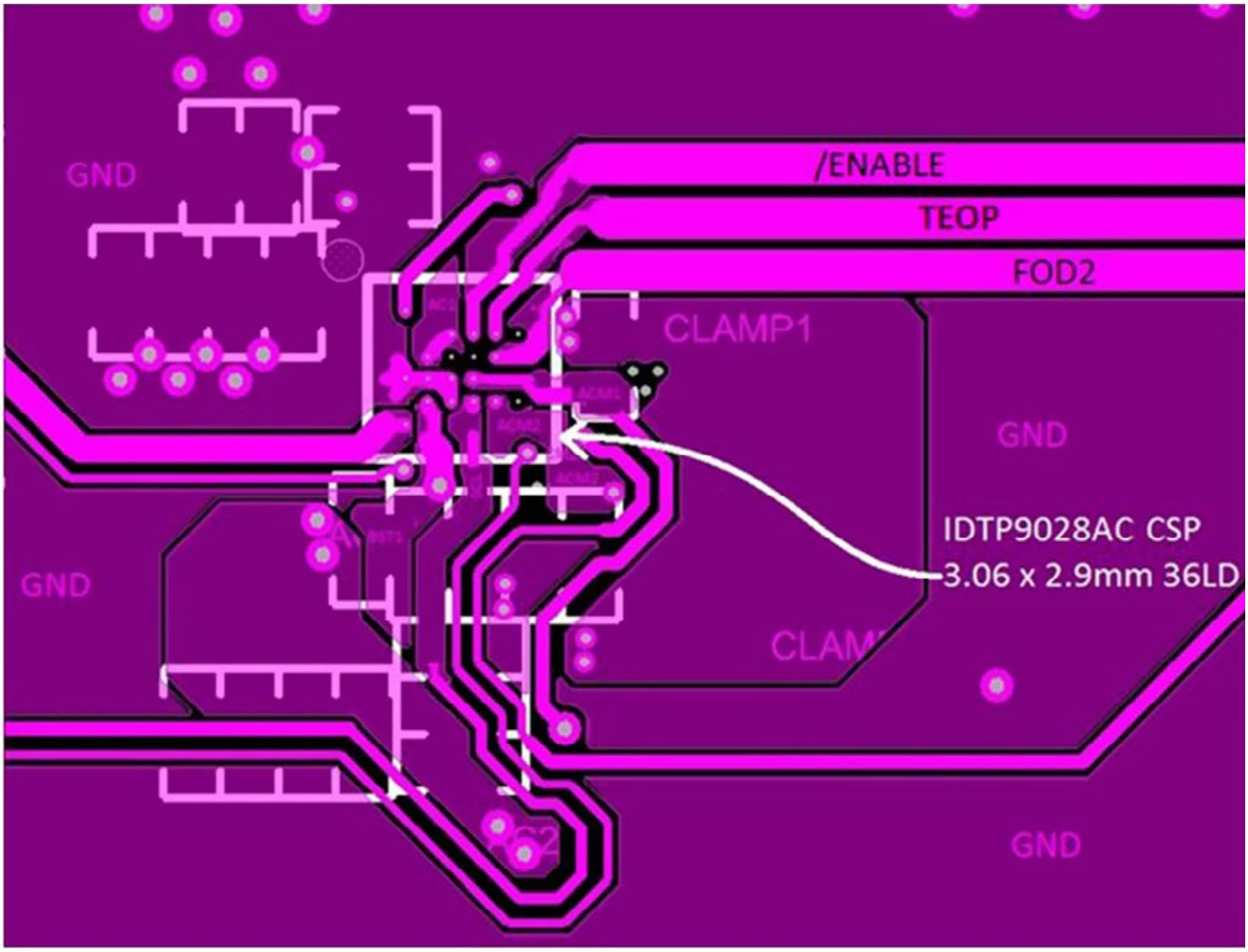


Figure 3: CSP device mounted on a four-layer PCB, third PCB layer shown (mid-layer 2).

surely be burned, because the amount of heat per unit times that the paper allows to flow now is 20x larger. This evidence proves that when a dielectric thickness is thin relative to the surface area that the heat will readily flow through the material and, in fact, the thinner the dielectric, the more effective the heat will transfer through the PCB thickness and spread across ground planes.

An optimal PCB design will have the top layer at nearly a uniform temperature across its entire surface and the bottom layer will be as close as possible to the top temperature. This is the point at which the transfer of heat from the circuitry on the PCB to the atmosphere (or other media in which the PCB would be immersed) is optimal (minimum temperature drop), with both sides of the PCB operating as heat-transferring surfaces.

Furthermore, when wide thick copper planes are used, the heat will travel horizontally and heat copper planes evenly since the copper plane has high thermal conductivity (raising the temperature of the entire area), and this will facilitate evenly distributed heat across each plane. Once heat is evenly spread, reductions in dielectric thickness will allow the surface temperatures to be closer to each other by improving the layer-to-layer transfer of heat. Therefore, PCBs with thinner dielectric thickness will outperform a PCB with thicker dielectrics regarding overall operating temperatures of the CSP ICs, all other variables held constant.

The final and most effective means to lowering the operating temperature of a CSP device is to maximize the volume of copper in contact with the IC on the component side of the PCB. The component side of the board is the layer that can transfer heat the most effectively away from the PCB due to the proximity to the ambient environment. Any inner layer heat must traverse to the PCB surface before it can be dissipated; therefore the surface temperature must be elevated for heat to flow away from the PCB. Another way to analyze the way surface copper will transfer heat most effectively is to compare the ratio of area to length of the heat paths close to the source. The key to identifying the most substantial paths is to determine the paths with the largest ratio and the number of these paths should be counted and summed since they are cumulative. This is a way to calculate a simple comparable value of potential thermal resistance of individual and cumulative heat transfer capabilities.

Considering a 36-pin CSP device that is a 6x6 array, let's assume the IC has 8 GND pins and each is connected directly to GND planes; with the thin via walls and the relatively long distance to the next layer, the ratio of area to length (A/L (m2/m)) is higher when considering the via compared to a 0.254 mm trace connected to a copper shape on the component side of the PCB. For example, a via that is 0.152 mm diameter via that has a length of 0.47 mm is a cylinder with the area of each infinitely thin annulus of the cylinder would be ~13.9 nm (assuming a via wall thickness plated up to of 25 µm thick) results in a heat transfer ratio of 29 µ (A/L).

Now, calculating the heat transfer ratio of a short component side trace to a heat-spreading plane with a length of 0.254 mm comprised of 1-oz copper and is 0.254 mm wide results in a heat transfer ratio of 35 µ (A/L). The short copper trace has a higher ratio and thus will conduct more heat than the via. Now consider that there are 8 GND vias, the total via-in-pad heat ratio would be 280 µ verse 350 µ if the CSP perimeter pins have 10 out of 21 perimeter pins are able to be connected to a wide surface of copper. So component side connections have a larger heat path ratio and typically have more direct connections to heat-spreading surfaces available than the number of vias-in-pad that are available for direct connections to copper planes.

Operating temperature is the result of the ambient temperature plus the increase in temperature needed to displace and dissipate all heat generated. Optimal thermal performance is achieved by designing a PCB that has the generated heat from the CSP spread as evenly as possible to as wide of an area as possible by conduction, so that convection is maximized by forcing the smallest possible delta from IC package temperature to the PCB surface temperature to ambient environment temperature. Since the CSP power devices do not have a direct substrate to PCB connection (such as the E-PAD of QFN packages), the flow of heat must be considered on a pin-by-pin basis.

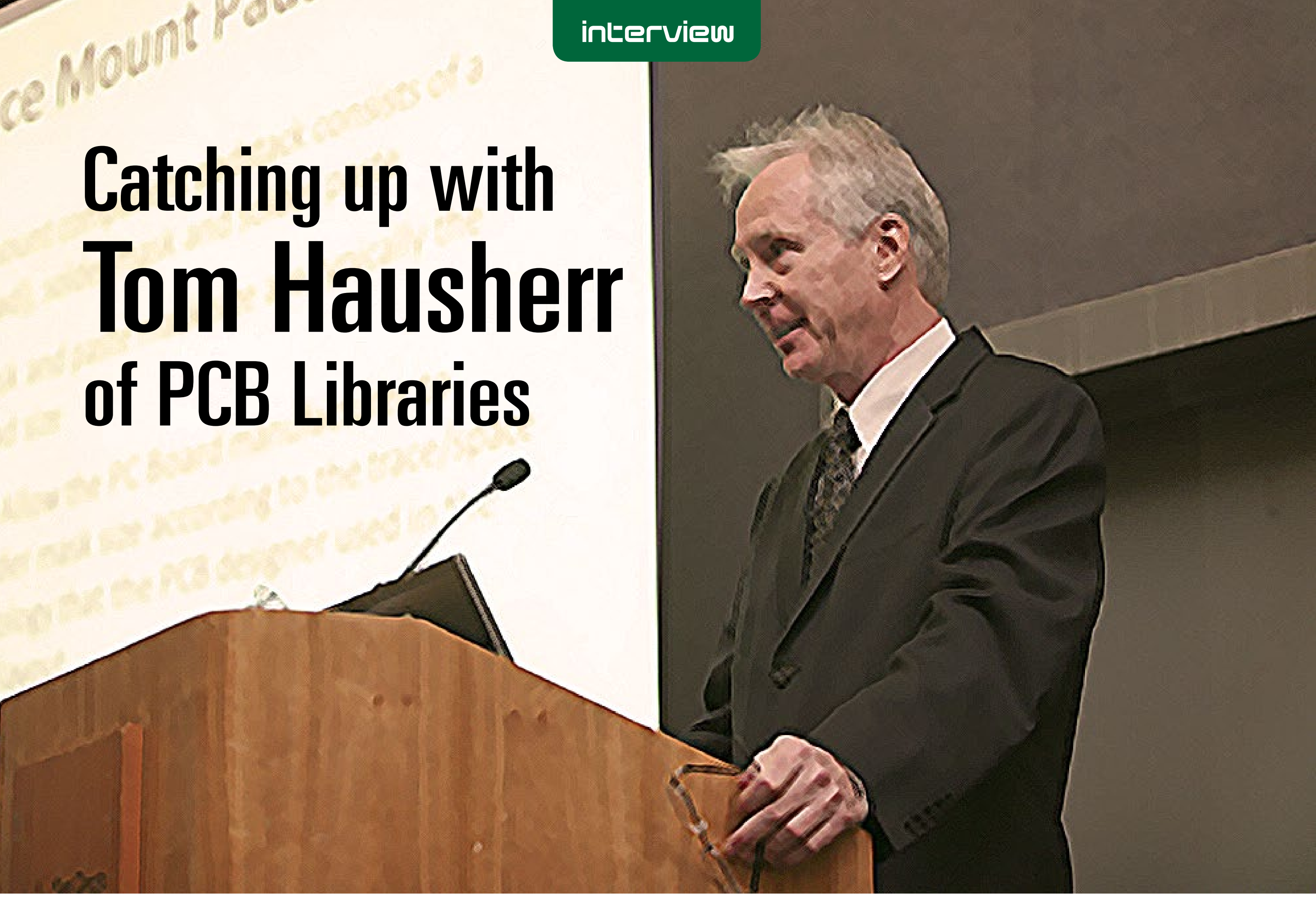
For the CSP, the heat path from each pin to the substrate is nearly identical since the die will be nearly the same temperature (within 1–2°C); therefore, each pin connection should be carefully inspected to increase copper connectivity in order to optimize the heat transfer from the integrated circuit to the PCB under development or revision. Since the component side of the PCB is the most effective means of heat transfer due to the outer pins having no thin vias, and there is a large number of outer perimeter pins all outer perimeter pins should have wide copper shapes connected to them as space permits regardless of current flow on the node without neglecting current carrying requirements. Finally, vias-in-pad should be utilized to connect each inner pin to wide copper shapes or traces as space permits, multiple layers decreases operating temperature as well as thinner PCBs. **PCBDESIGN**

References

1. Resnick, Robert. "Physics, 5th Edition, Vol. 1," Wiley, 2002.

Nicholaus Smith is an applications engineer at Integrated Device Technology.

Catching up with Tom Hausherr of PCB Libraries



by Judy Warner
ZENTECH MANUFACTURING

In the past year, I stopped procrastinating about attending my local chapter meetings of the IPC Designers Council in Southern California. My friend Scott McCurdy of Freedom CAD had been gently nudging me for months before I finally made it to my first meeting back in March. Scott has been running the Orange County DC Chapter for 12 years and has turned it into the largest chapter in the country. Knowing this, I was still shocked when I walked into a room packed with 77 people. Furthermore, I was captivated by the speaker for that day, Tom Hausherr of PCB Libraries.

I know little about the dynamics that go into component libraries, since my tenure has been in the fabrication and assembly side of the business. Yet, Tom's information was clear and accessible—even to me. On that day, I made a new friend and became a fan of Tom's. So, when fate placed us both at PCB West, we made sure to carve out some time together. Tom agreed to have a long breakfast with me so I could learn more about the challenges related to component libraries and how his company addresses these issues. So, pull up a chair and join us for a chat.

Tom Hausherr

***Judy Warner:** Tom, there are CAD libraries everywhere. Manufacturers offer free libraries on their websites. How is PCB Libraries different?*

Tom Hausherr: Unlike canned libraries that are everywhere (we've offered them before) but found that most of our users do not really use them. All of our parts are dynamically customized with unique user preferences. Users get parts with their desired rotation, tolerance, pad shapes, linewidths, and desired colors for 3D STEP models, and dozens of other customizable features. The part data from PCB Libraries

gets processed by the Library Expert (where user preferences are applied), and output to the various CAD formats. This feature allows users to adjust dozens of preferences and rebuild entire libraries based on future needs. Professional designers and engineers want boards designed in a consistent manner, not patched up with no consistency between free parts obtained from dozens of places. Among other powerful features, the Library Expert also allows users to search an entire bill of materials (BOM) against their parts to automatically identify the parts they have and the ones they need, which greatly simplifies the part search process.

Warner: That's an interesting concept. What led you to develop a library tool like this?

Hausherr: I started my first library of symbols and footprints at Beckman Instruments in 1982. My manager educated me that the CAD Library was the foundation of the PCB Layout. I'll never forget his words, "Garbage in, garbage out." Based on our need and the limited computer technology then, it took me nine months of working long hours before I could start my first CAD tool PCB layout. I thought to myself, "There has to be a better way." Ready-to-use, high-quality library parts where a must-have for us to increase productivity. Then, in the 1990s, I owned CADPRO, the largest PCB design service bureau in San Diego at that time. Besides PCB designs, we offered the CADPRO library that helped hundreds of companies.

Warner: What happened to the CADPRO Libraries?

Hausherr: In 1998, I took the IPC CID certification class with Dieter Bergman. I learned from Dieter that the electronics industry is in a metric conversion process and that the Inch-based CADPRO libraries will be obsolete in 10 years because most component manufactures will provide package dimensional data in metric units. Dieter also asked me to join IPC's effort to support IPC-SM-782 and that IPC would help me with the creation of the first standalone PCB library calculator software program. After a couple weeks of research, I sold CADPRO and went to work for Wind River.

Warner: Why did you select Wind River as your next employer?

Hausherr: Wind River was CADPRO's largest customer and when they heard I was selling CADPRO, they asked me to manage their CAD department. That is where I met and started working with Jeff Mellquist. Jeff and I started collaboration on inventing Excel spreadsheets that contained the mathematical model for IPC-SM-782. It took us three years to create a unique calculator for every standard component package. Then we opened pcbstandards.com to upload test libraries created from the Excel Spreadsheets. However, in 2001 Dieter Bergman introduced Jeff and me to a new three-tier library concept which became IPC-7351. Jeff and I took another two years to fully develop IPC-7351 calculators and in 2003 Jeff left Wind River as a senior PCB designer to learn software programming.

Warner: Is that how PCB Libraries got started?

Hausherr: Yes, Jeff created his first software program in 2003-2004, and it was released as the Library Navigator. I left Wind River in 2004 to join PCB libraries. The original Library Navigator was a clunky tool but people purchased it because it shaved time off library creation. Jeff soon rewrote the program and we renamed it LP Wizard. We renamed the company PCB Matrix because we started to develop other software tools for PCB design layout and the name PCB Libraries no longer suited us. However, our flagship product was the LP Wizard, which was rapidly spreading throughout the industry. In December 2008 we sold PCB Matrix's LP Wizard to Valor Computerized Systems.

Warner: What motivated you to sell a successful product?

Hausherr: Because Valor offered an expanded reseller chain, upgraded customer support, ad-

ditional programmers, a larger marketing budget, and they promised to keep and improve the CAD tool interfaces in LP Wizard. We looked at the Valor deal as a big win for us, and for our customers. Our customers were very happy at the news.

***Warner:** How did the Valor acquisition turn out?*

Hausherr: Valor lived up to all of their promises and commitments. More programming help was added, marketing was expanded globally and the LP Wizard's future was bright, but this only lasted for a little over a year. Mentor Graphics acquired Valor, and eventually chose to discontinue support for any CAD tool except theirs. This was the single biggest blow to LP Wizard as the product revenue was reduced drastically. About one year later, the remainder of the PCB Matrix team was laid off. So the original team went back to IPC and met with Dieter Bergman to apologize for all the commotion and upsetting the global library industry. We discussed the creation of a brand-new tool that, unlike the LP Wizard, would be based on component dimensions going through user preferences to fully automate the creation of custom library parts, come with much more content, and even support non-standard parts.

***Warner:** How did you restart PCB Libraries?*

Hausherr: Nick, Jeff and I worked tirelessly for over a year to design a new website and create a new tool called PCB Footprint Expert from scratch. We eventually had to change the product name to PCB Library Expert once we offered the first 3D STEP automation tool in the industry, and we're planning on supporting schematic symbols in the near future. As common with startups and new products, while the new product gained a footing, we all worked for no pay or benefits for two years until we finally had enough sales to generate a small payroll.

***Warner:** So what's next for PCB Libraries Inc.?*

Hausherr: We're currently rewriting Library Expert from scratch again for 2016. We plan to add new features that we did not consider or could not implement originally. Technology keeps changing. We want to take advantage of the latest Windows 10 OS and advancements in software programming tools for the new features, and help take the Library Expert into the future. The new Parts on Demand website[1] has just started to take off and we now have one million part numbers that are free to all our Library Expert users. Some day we plan to have many millions of parts to offer our customers. I can see the day when maintaining large CAD libraries will be a thing of the past. The library parts for every design will be stored with the PCB design file and new library parts will be auto-generated with new rules that are specific to every new PCB layout. The days of manually creating and maintaining PCB library parts will come to an end in the near future.

***Warner:** The future is looking good for the electronics industry. Shaving days off every PCB layout would be another major industry innovation. Thank you, Tom, for this informative interview and history lesson.*

Hausherr: Thank you for the interview. It was fun going back in time.

References

1. www.PCBLibraries.com/POD

Judy Warner is director of business development for the Western Region and RF/microwave markets for Zentech Manufacturing and a frequent contributor to I-Connect007 publications.

Recent Highlights from PCBDesign007

1 IPC Designers Council Viewpoint: Rick Hartley

Rick Hartley has been in involved in PCB design and design education for decades, so it's no surprise that he started working with the IPC Designers Council early on. Now retired from his day job at L-3, Rick still teaches PCB design and shows no sign of slowing down. I asked him to discuss his work with the Designers Council, and what the group means to the design community.

2 DownStream Takes on Data Documentation Management

Most PCB designers love their jobs. But designers will also tell you that as much as they enjoy laying out the board, they dislike the final data documentation step, which often involves various formats, including handwritten notes. Enter DownStream Technologies, a company founded 14 years ago to address the challenges related to post-processing the design. Senior Product Marketing Manager Mark Gallant recently discussed the company's efforts to take the pain out of data documentation, even as data becomes more complex.

3 Most-Read PCB Design News Stories of 2015

Each December, we like to look back at the year in PCB design news. January seems like yesterday, doesn't it? Since then, we've seen plenty of innovative new tools and a variety of partnerships, and we've said goodbye to a couple of longtime friends. As we approach 2016, enjoy this list of the 10 most-read news items on PCBDesign007 in 2015.

4 EMA: Helping Technologists Manage Disparate Data

Today's EDA tools are better than ever, but managing design data, from schematics through Gerbers, can be an unwieldly task. I recently interviewed Manny Marcano, president and CEO of EMA Design Automation. He discusses EMA's approach to managing a variety of types of complex data, the need for seamless data processes, and the future of compliance-aware design.

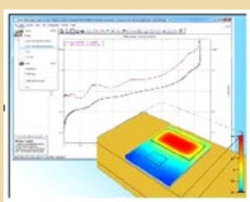
5 Rogers Scales up Production and Integrates Arlon Range

Editor Pete Starkey interviews Rogers European Sales Manager John Hendricks at productronica 2015. Hendricks updates us on Rogers' acquisition of Arlon, and explains how the Arlon products are complementary to Rogers' existing materials.

6 Beyond Design: Plane Crazy, Part 1

A high-speed digital power distribution network (PDN) must provide a low inductance, low impedance path between all ICs on the PCB that need to communicate. In order to reduce the inductance, we must also minimize the loop area enclosed by the current flow. Obviously, the most practical way to achieve this is to use power and ground planes in a multilayer stackup. In this two-part column, I will look at the alternatives to planes, why planes are used for high-speed design, and the best combination for your application.

7 Mentor Webinar: Maximizing the Accuracy of FloTHERM Models



This January 20 webinar will introduce the new capability in FloTHERM v11.1 to automatically calibrate FloTHERM models to match T3Ster measurements. T3Ster measurements capture the full transient thermal characteristics of a device, and converts this into industry standard Structure Function curves.

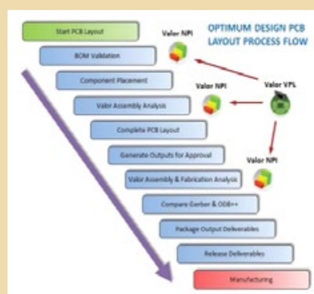
8 Zuken USA Expands Operations with CAETEK Acquisition

Zuken USA Inc., a leader in electrical and electronic design software, has acquired CAETEK Inc. CAETEK is a software developer and sales partner for electrical design and manufacturing solutions. The addition of CAETEK will strengthen Zuken USA's product portfolio and coverage in the electrical design space. CAETEK employees and intellectual property will transition to Zuken USA as part of the acquisition.

9 Pulsonix Poised to Take More EDA Market Share

Publisher Barry Matties met with Bob Williams, managing director and co-owner of Pulsonix, and Sales and Marketing Manager Tyrone Stephens to discuss the challenges facing the EDA tool market, and how they're establishing this UK-based company in the global design tool marketplace.

10 Mentor White Paper: Optimum Design Associates on Implementing Lean NPI



Pleasanton, California-based Optimum Design Associates has implemented Lean NPI into its PCB design and layout processes, and seen exceptional results. In this series of white papers, ODA explains how Valor NPI and ODB++ were instrumental in helping this company achieve best practice Lean NPI, and how Lean NPI can help your company too.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out ***The PCB Design Magazine's*** event calendar.

DesignCon 2016
January 19–21
Santa Clara, California, USA

Pan Pacific Microelectronics Symposium 2016
January 25–28
Big Island, Hawaii, USA

Rocky Mountain Expo & Tech Forum
January 26, 2016
Denver, Colorado, USA

The Changing Landscape of REACH
February 10, 2016: Brea, California, USA
February 17, 2016: Herndon, Virginia, USA

Houston Expo & Tech Forum
March 1, 2016
Stafford, Texas, USA

Dallas Expo & Tech Forum
March 3, 2016
Plano, Texas, USA

IPC APEX EXPO Conference & Exhibition 2016
March 15–17, 2016
Las Vegas, Nevada, USA

CPCA Show (China International PCB & Assembly Show)
March 15–17, 2016
Shanghai, China

South East Asia Technical Training Conference on Electronics Assembly Technologies 2016
April 12–14, 2016
Penang, Malaysia

NEPCON China
April 26–28, 2016
Shanghai, China

SMT Hybrid Packaging
April 26–28, 2016
Nuremberg, Germany

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Strategies for Increased Profits

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