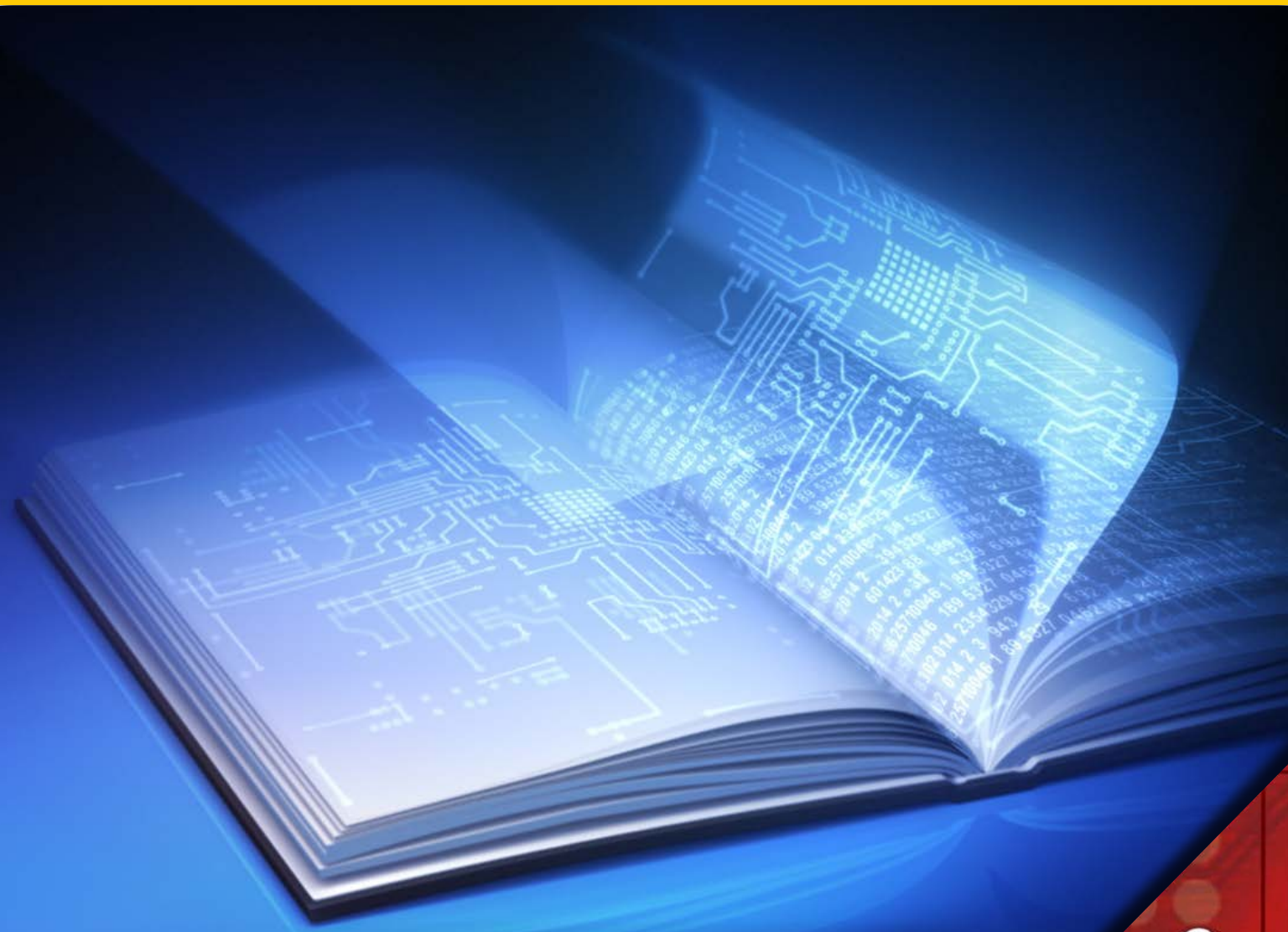
THE pcb design MAGAZINE

March 2014

AN I-CONNECT007 PUBLICATION

DOCUMENTATION



Mitigating the High Cost of PCB Documentation

by Mark Gallant, Page 12

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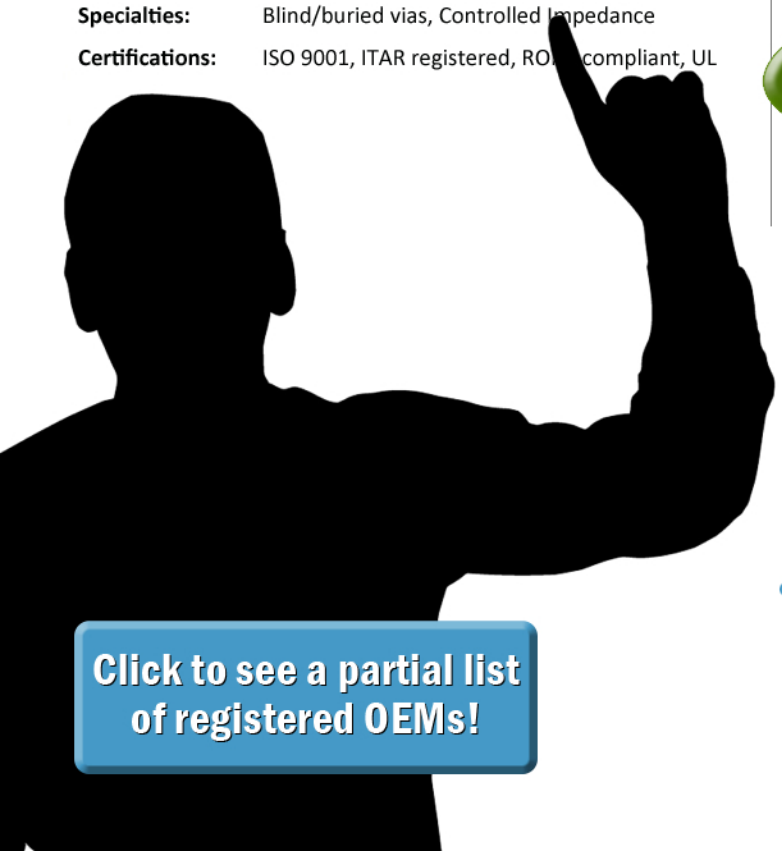

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THE pcb design MAGAZINE™
March 2014
This Issue: DOCUMENTATION

FEATURED CONTENT

The layout is finished, but now it has to be documented for manufacture. What's the best approach to ensuring your fabricator builds the board exactly the way you intend? Find out in this issue of *The PCB Design Magazine,* when veteran contributors Mark Gallant, Martyn Gaudion, and Amit Bahl focus on what happens after layout.

FEATURE COLUMN

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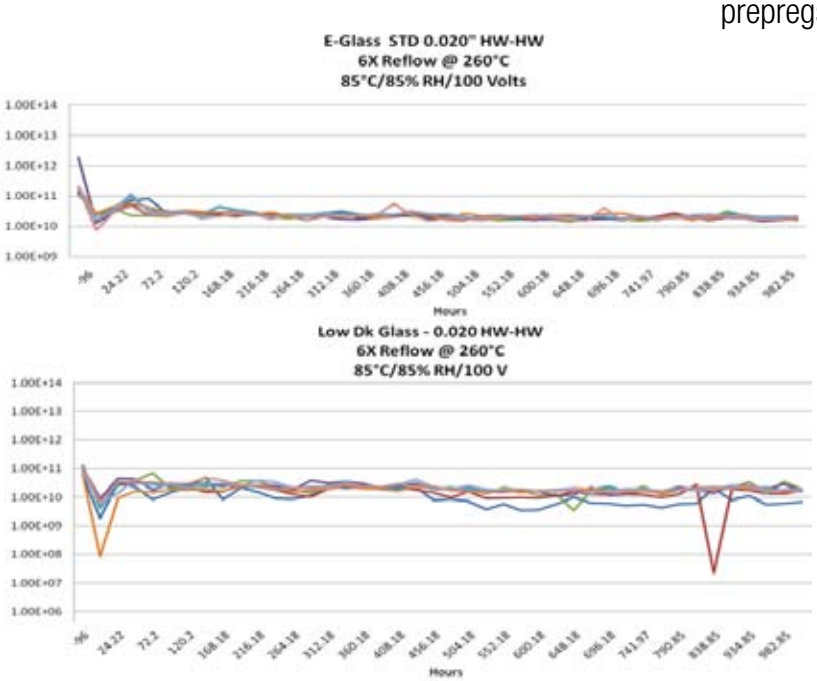

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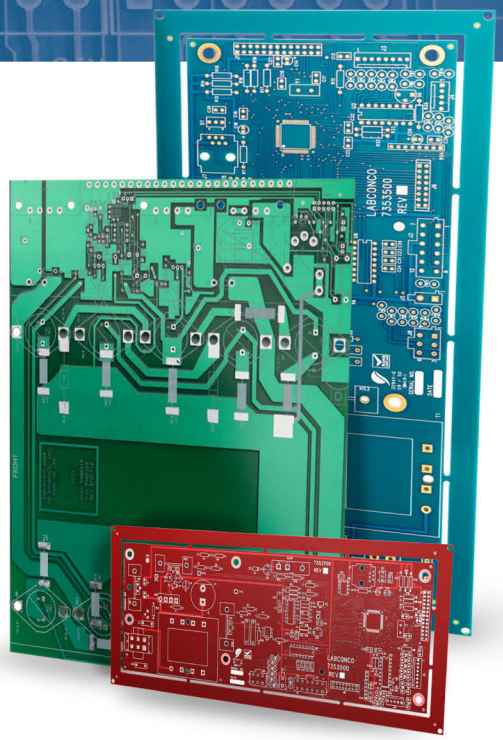

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THE SHAUGHNESSY REPORT

Back to Vegas

by Andy Shaughnessy
I-CONNECT007

Yes, we're heading back to Las Vegas for IPC APEX EXPO 2014. I, for one, will be glad to get back to Sin City.

I admit I was a little burned out on Vegas the last time APEX and the Designers Forum were held there, back in 2011. (That was BD, or before divorce.) We had been there for four years in a row covering the show, so I cheered when IPC announced that the event would be moving to San Diego for 2012 and 2013, and alternating every two years after that.

Now, don't get me wrong: San Diego is a great location. It's hard not to like a place that's always at the top of the annual "Top Cities in the Country" lists. And we did some sailing, which the desert pretty much precludes.

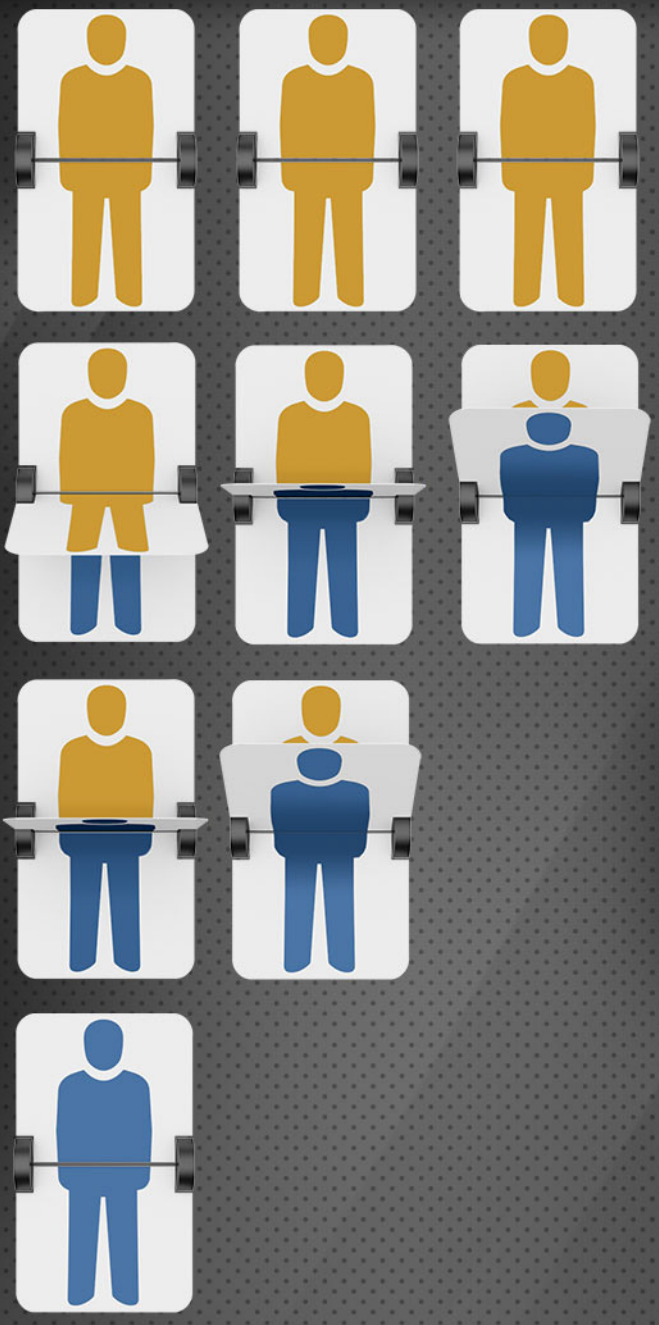
But after three years, it'll be nice to get back to Vegas. It's a microcosm of America, a symbol of all that is positive and negative in the land of red, white, and blue. This town is a true dichotomy: gamblers can win big, or lose big. There are a lot of really happy people on the way up, and a lot of not-so-happy people on way down. Plenty of shiny casinos, and too many foreclosed houses.

Of course, Vegas presents its own unique challenges. My co-workers and I spend most of the week bathed in artificial light. We get up early, and by the time we finish work, it's nighttime. Years ago, Editor Marcy LaRont dubbed us "The Mole People," because we went for days at a time without ever seeing the sun. I was afraid we might develop the bad eyesight that moles are famous for.

And you'd better wear your walking shoes for trade shows in Vegas. Mandalay Bay is a great venue, but it's so big that you just about need a GPS. Everything you need is a quarter mile away from your current location. One Mandalay Bay staffer told me that the show floor is almost half a mile from the front door.

Still, I'm glad to be heading back to Vegas. This year, APEX kicks off with the Designers Forum on Monday, March 24. Speakers include Greg Munie of IPC, Karen McConnell of Northrop Grumman, Gary Carter of Fujitsu

More and More PADS Users are Switching to Altium Designer



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BACK TO VEGAS *continues*

Network Communications, Dieter Bergman of IPC, Mark Laing of Mentor Graphics, Humair Mandavia of Zuken, and Ben Jordan of Altium.

Guest Editor Kelly Dack and I will be shooting video interviews for our *Real Time with… Designers Forum* program, and we'd love to interview you on camera. I've noticed that more and more PCB designers and design engineers are video-savvy; many of you handle yourselves well in front of the camera, and you don't freak out when the red light comes on.

It's really not much different from speaking to the other members of your department. But even if you're reluctant about being interviewed on camera, we can work with you. And if you're a PCB designer, I guarantee that you have a story worth telling. It does get easier over time. My first interview was a disaster, but we gave Charlie Capers and the rest of the staff at Trilogy Circuits something to chuckle about!

The Survey Says…

This month, don't miss "The Town Crier." The inaugural column by our newest columnist, Dan Smith. Dan is a principal technologist at Raytheon, and a 33-year veteran of software design firms and military contractors. He has worn a lot of hats: PCB designer, programmer, product architect, and professional piano player.

Dan, "The New Mr. HDI," was handed the HDI torch by Happy Holden, and he leads the PCB HDI—Next Generation group on LinkedIn. He has a passion for PCB design, especially design education. He's taught the PCB design process internationally, and he's led IPC's HDI certification efforts.

In this month's column, Dan delves into the state of PCB design instruction, and he wants your feedback. Take a few minutes to complete Dan's short survey on PCB design and design education. I know you're busy, but this won't take long. Then, Dan will discuss the survey results in his column over the next few months. This issue is too important to cover with just one column.

Dan welcomes your e-mails, but don't be surprised if your name shows up in an upcoming edition of "The Town Crier."

See you in Vegas! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking here.

MIT Develops Herding Robots

Writing a program to control a single autonomous robot navigating an uncertain environment with an erratic communication link is hard enough; write one for multiple robots that may or may not have to work in tandem, depending on the task, is even harder.

This May, at the International Conference on Autonomous Agents and Multiagent Systems, researchers from MIT's Computer Science and Artificial Intelligence Laboratory (CSAIL) will present a new system that stitches existing control programs together to allow multiagent systems to collaborate in much more complex ways.

Researchers are currently testing their system in a simulation of a warehousing application, where teams of robots would be required to retrieve arbitrary objects from indeterminate locations, collaborating as needed to transport heavy loads.

"In [multiagent] systems, in general, in the real world, it's very hard for them to communicate effectively," says Christopher Amato, a postdoc in CSAIL and first author on the new paper.

"What typically happens is, the programmer decides that red light means go to this room and help somebody, green light means go to that room and help somebody," Amato says. "In our case, we can just say that there are three lights, and the algorithm spits out whether or not to use them and what each color means."

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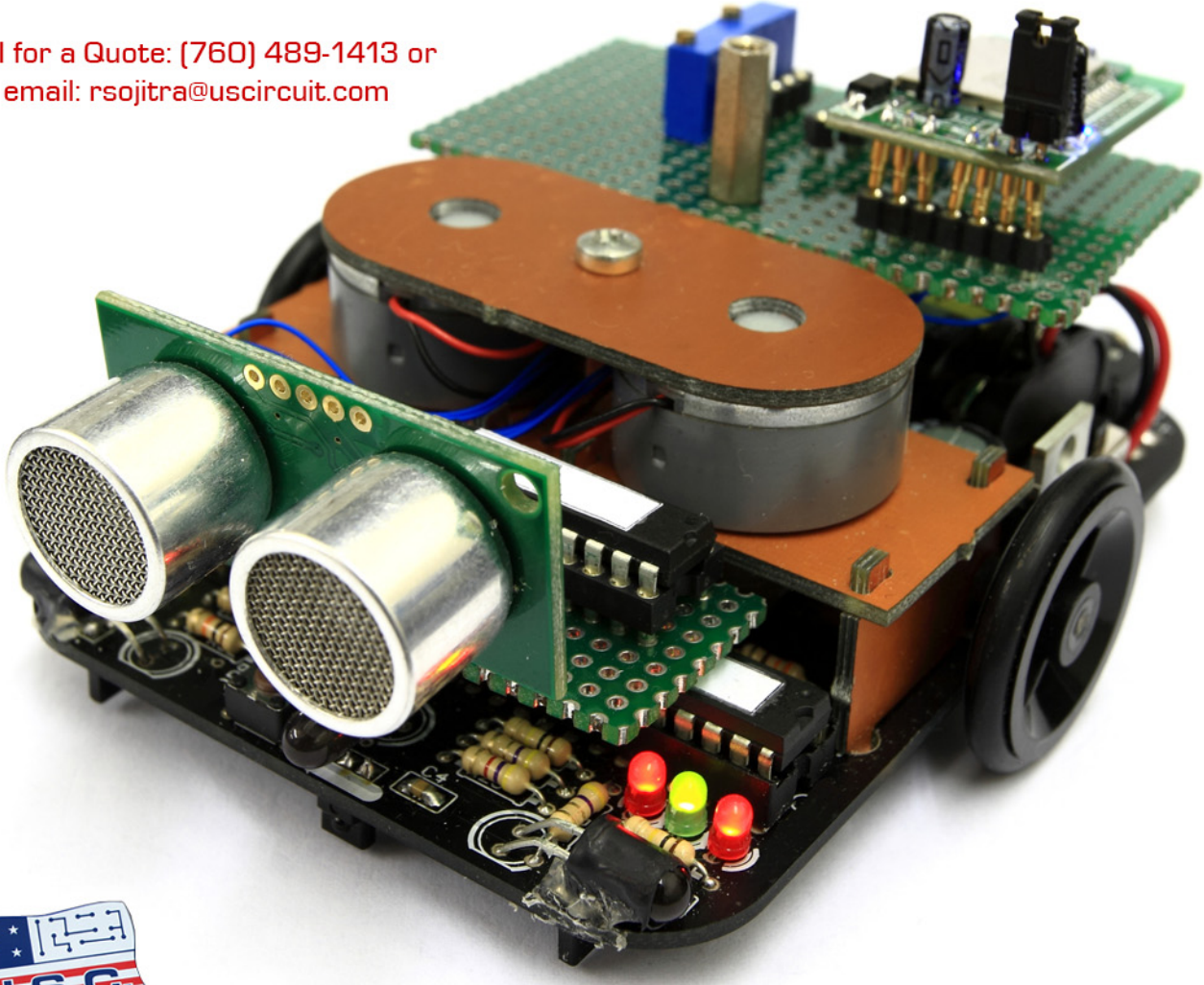

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Mitigating the High Cost of PCB Documentation

by Mark Gallant
DOWNSTREAM TECHNOLOGIES

The goal of minimizing the time and cost for engineering a new product and getting it to market before the competition is a constant struggle for developers of leading-edge electronic products. The complexities of the electronic component supply chain, reductions in qualified staff, and managing globally distributed engineering teams are just a few of the challenges. Eliminating bottlenecks can dramatically reduce concept-to-production time in a product life cycle. This is the Holy Grail in the quest for corporate efficiency.

To reduce or eliminate these bottlenecks in new product development, many electronic engineering teams are looking inward and reassessing the efficiency of their product engineering process. From concept to design, fabrication, and assembly, there are process inefficiencies that result in delays. The usual excuse for not reassessing, "This is the way we have always done it," may be a sign of complacency in an inefficient engineering process.

Quite often the assessment involves an evaluation of the current EDA tool set proficiency. Frequently, these tool evaluations evolve into an assessment of how their current tools perform against competitive tools. Loyalty to the incumbent EDA provider is a lesser consideration than the efficiency of the tool. As a result, entrenched EDA suppliers are forced to perform benchmarks for current users or risk a decline in their customer base.

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The Evolution of EDA Tools

In the CAD revolution of the 1980s, software-based EDA tools facilitated the migration from light tables and drafting boards to rooms full of hardware and software from best in class EDA tool providers. When one component of the EDA tool set was deemed inefficient, it was replaced with a more efficient tool from a litany of niche EDA tool providers. However, there was an inherent inefficiency in the interoperability of tools from different EDA tool providers. Integration was rudimentary at best, and often managed by the end-user. Poor tool integration was a key factor during the EDA provider consolidation in the 1990s as mergers and acquisitions forever changed the EDA landscape. The number of tool providers shrank dramatically, and the multi-provider EDA tool set slowly morphed into a sole-vendor EDA tool set.

With the rapid adoption of a sole-vendor EDA tool methodology, new challenges arose. Being the largest EDA tool provider did not necessarily equate to being the best provider. Technological advancements and engineering process improvement goals often required tools not available from the core EDA vendor. In some cases, vendor offerings were just not suitable for the users' needs. Replacing inefficient or unsuitable components of a single-vendor EDA tool set imposed a significant challenge. Any new component must integrate seamlessly

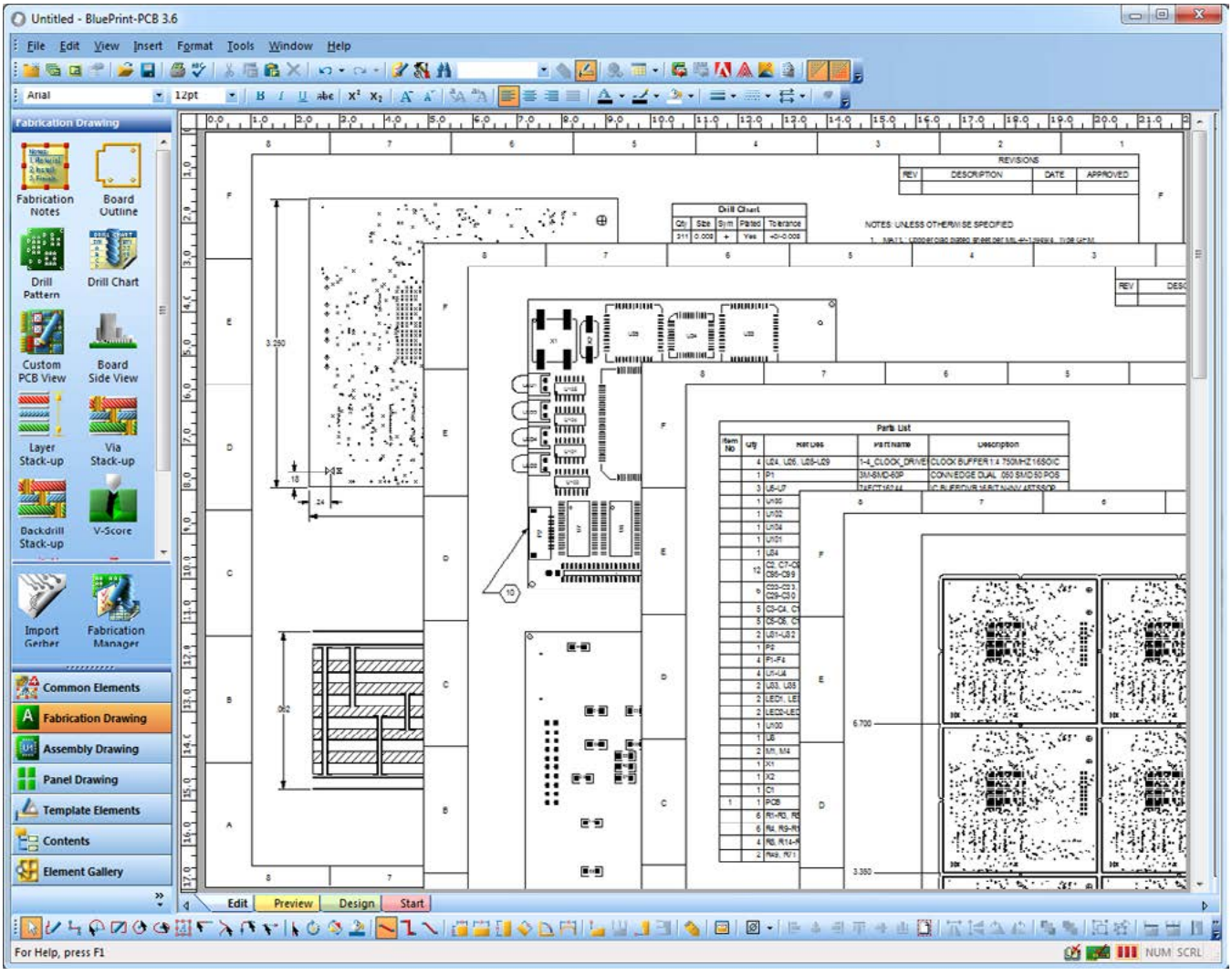


Figure 1.

into the current process and not disrupt the engineering process.

To facilitate this plug and play, engineering teams relied on user-developed custom applications. These applications served as the glue or patch cords between core EDA tools and niche third-party tools to create a manageable work flow. The pain of this methodology became obvious whenever an EDA tool provider required users to migrate away from their tried and true legacy tools to newer, more efficient tools. Typically, userware applications are written in a version specific scripting language. Legacy userware was incompatible and required herculean effort by specialized development resources from a small talent pool to achieve compatibility with the new tool.

These resources were vital to maintaining a smooth engineering process, but they are not without their impact on new product introduction costs. The cost of implementing and maintaining integration of disparate tools was the impetus for industry standard file format specifications for data transfer, such as IPC-2581 and ODB++. Having a neutral file format endorsed and supported by all members of the EDA ecosystem facilitated data transfer among disparate tools.

EDA tools like schematic capture, digital and analog simulation, PCB design and layout,

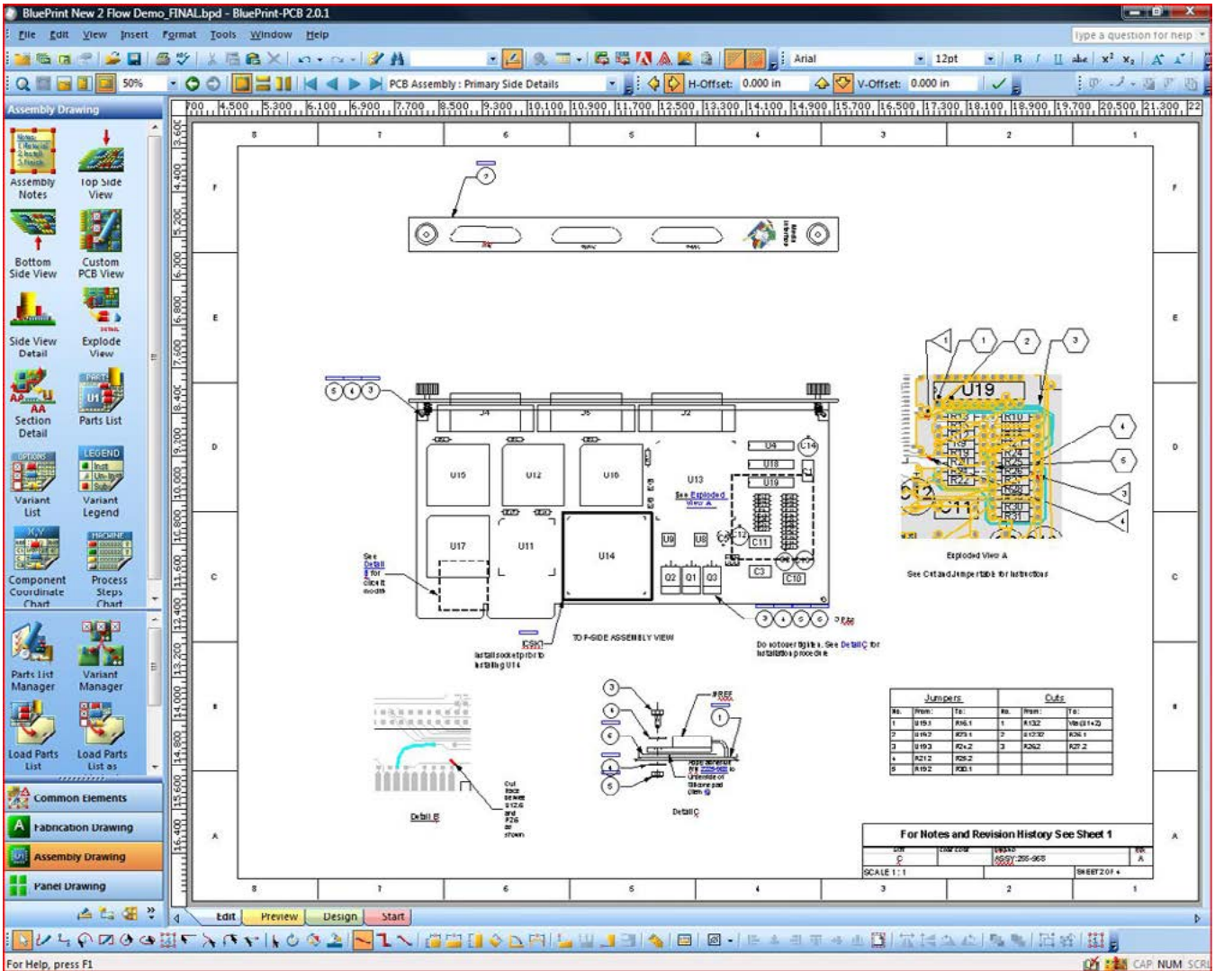


Figure 2.

autorouters, and others have matured, dramatically reducing time to market. But, even though most EDA tool providers have enhanced their tools through integration of new functionality or acquisition, some areas of inherent inefficiency in PCB CAD tools remain.

Post-Design Documentation: Late to the Party?

One glaring example of this: The documentation required for fabrication and assembly of the PCB. Comprehensive PCB documentation is a requirement today, and if the end-product is destined for a military or aerospace user, the documentation requirements ratchet up considerably.

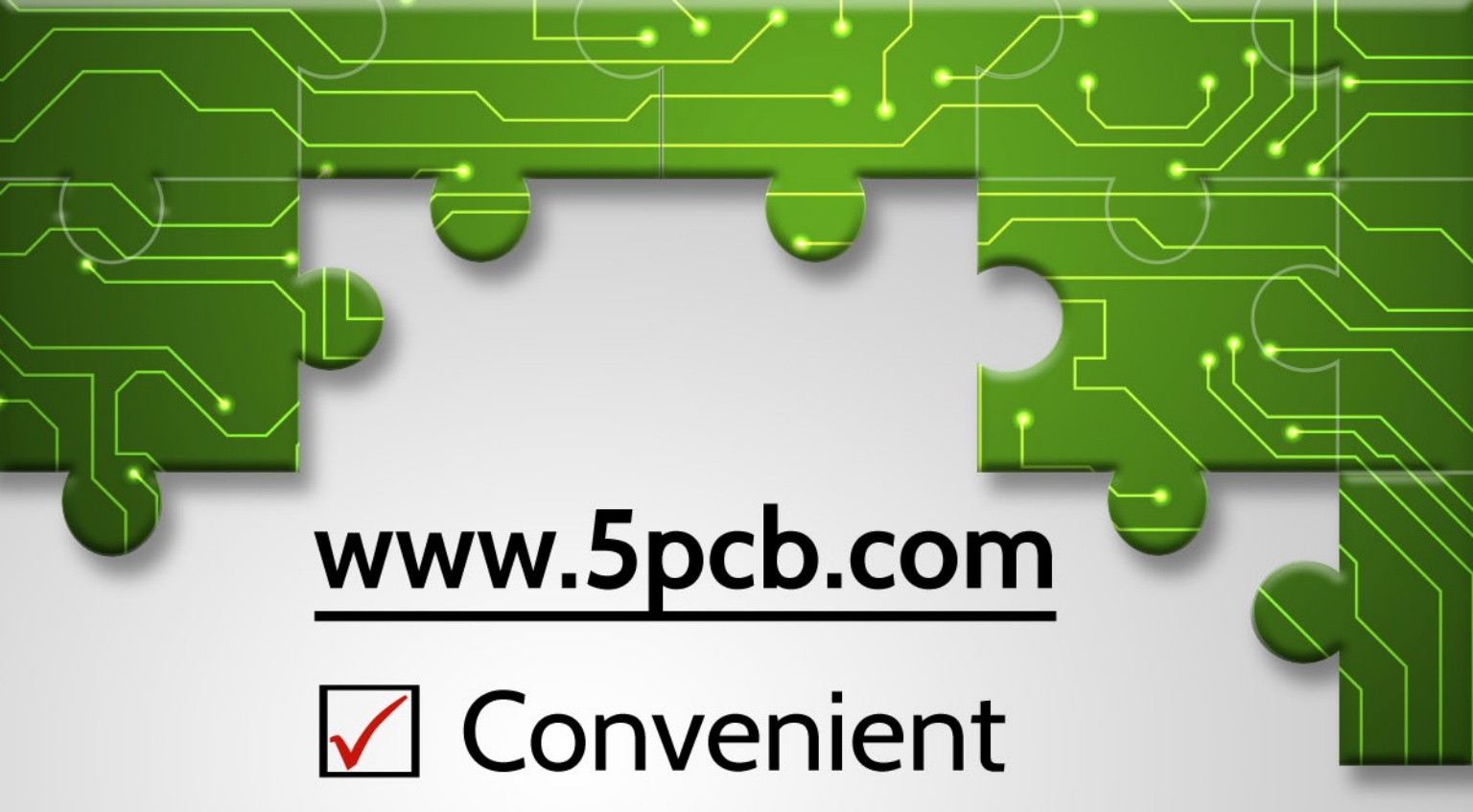
Yet the majority of PCB documentation is created using PCB CAD drafting features that have not improved since the CAD revolution of the 1980s. CAD tools are superlative at reducing the PCB design cycle, but they fall short on some of the most basic documentation tasks. For example, PCB design tools that sell for tens of thousands of dollars per seat lack the spell-checking found in $99 word processor software. Most CAD tools lack support for a paragraph requiring the user to create multiline text strings as basic fabrication notes. Countless hours are spent using rudimentary drafting tools to create PCB detail views and drill charts, one segment or one line at a time.

These antiquated methods show their real colors during a design re-spin. Drill quantities out of sync in a manually drawn drill chart? Select the text string and edit the value. PCB detail view need updating because a component moved on the PCB? Either recapture the entire view or start editing the graphics one vertex or one segment at a time. Some engineering organizations have resolved to use popular MCAD tools to complete the PCB documentation. MCAD tools are superior to PCB CAD tools with respect to creating documentation.

However, converting the design to MCAD file formats results in disassembling the intelligent PCB CAD data. Parts are converted to shapes, traces to lines, copper shapes to polygons, and so on. Creating tables, notes, complex dimensions is certainly quicker, but cultivating intelligent data for a parts list is no longer possible with MCAD tools. Should a design re-spin be required, the MCAD drawings must often be recreated or manually updated with new design content. It also introduces an MCAD design database to an already crowded PCB documentation file collection. Maintaining synchronicity between PCB and MCAD design databases becomes the responsibility of the user.

> ***Every PCB design has its share of tasks related to documentation. Stringent documentation standards for military, aerospace, automotive and other segments require highly detailed, time-consuming documentation sets. Documentation requirements are not limited to one department across an entire organization. Many downstream processes in product manufacturing have unique documentation requirements.***

The bottom line: Creating PCB documentation is not free or well automated in PCB CAD tools. Every PCB design has its share of tasks related to documentation. Some documentation sets can be dozens of drawing sheets. Stringent documentation standards for military, aerospace, automotive and other segments require highly detailed, time-consuming documentation sets. Documentation requirements are not limited to one department across an entire organization. Many downstream processes in product manufacturing have unique documentation requirements. This includes PCB rework instructions, assembly process steps, PCB panel fabrication drawing, assembly inspection, and more. There is more to a PCB documentation set than a simple one-sheet assembly and fabrication drawing. All of these



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documentation requirements should be part of any documentation efficiency calculation.

When considering the efficiency of your PCB documentation process, you must measure both creation and maintenance of a complete documentation set for the full life cycle of the product. A new product's documentation cycle typically begins at the prototype stage. From there, the number of documentation iterations can easily reach double digits. Consider that each iteration of a documentation set has both tangible and intangible costs, the greatest tangible cost likely being the salary of the individual creating the documents. Assuming an average PCB designer salary of $75,000, and 20% of his time devoted to originating documentation, annual documentation costs will average $15,000 per designer. That amount does not include time spent revising original documentation or documenting rework instructions to update in-house product inventory.

If we assume that revising a document takes 50% of the time it took to originate, add another 10% or $7,500, and your annual documentation costs rise to $22,500, a hefty sum if you are creating a basic two-sheet documentation set. Developing military standard PCB documentation can usurp more than 40% of a PCB designer's time. For those products, the cost of creating and maintaining documentation can easily escalate. Some engineering organizations operate without dedicated PCB designers and require electrical engineers to complete the PCB design process. Because the average salary of an electrical engineer is higher than that of a PCB designer, this could factor into the high cost of creating documentation.

Developing military standard PCB documentation can usurp more than 40% of a PCB designer's time. For those products, the cost of creating and maintaining documentation can easily escalate. Some engineering organizations operate without dedicated PCB designers and require electrical engineers to complete the PCB design process. Because the average salary of an electrical engineer is higher than that of a PCB designer, this could factor into the high cost of creating documentation.

There are also intangible costs that are difficult to quantify. An inefficient documentation process that results in delays or a lengthy new product introduction process bears lost opportunity costs. Errors in the documentation set can result in multiple unplanned documentation revisions, re-spins of the PCBs, and errors in the assembly or part procurement process. Having a PCB designer focus 20% or more of his time on documentation rather than PCB design will delay the start of the next PCB design project. Sharing a networked PCB design product license to create documentation and design PCBs may require users to postpone critical tasks until product licenses are made available.

To mitigate the cost of documentation, begin by evaluating your PCB documentation tools and considering how well they meet your documentation requirements. Using a PCB CAD tool with minimal support for basic documentation tasks may require additional effort for working around its shortcomings. For example, what does it take to draw a complex layer stackup detail or multi-row drill chart? How easily can these details be updated when the layer count is increased, drill counts are changed or new drill sizes added? Secondly, you should examine the documentation process and documentation requirements across all members of your organization. Follow the documentation trail to learn how each member of the entire enterprise uses the documentation set.

Are they creating documentation to augment their process that is currently not part of your standard documentation set?

Over the course of the CAD tool evolution, the suite of tools required for PCB design has somewhat stabilized. Schematic capture tools are used for drawing schematics, simulation tools for analog and digital simulation, PCB design tools for circuit design, and so on. All are automated tools designed and maximized for a specific part of the electronic product design process. Automated PCB documentation tools are not new, but their use is not widespread. Many are still reliant on the outdated method of creating PCB documentation within the PCB CAD tool to meet their requirements.

You can't design a PCB with a schematic capture tool, so why are so many designers using a PCB CAD tool to create documentation? This is akin to manually routing each trace of a 16-layer 8,000 net PCB design rather than using automated routing. The results will be similar, but the effort far greater.

The old adage "Use the right tool for the job" rings true for PCB design and documentation. If you are creating PCB documentation today, you should consider dedicated PCB documentation tools, such as Mentor Graphics' Fablink or DownStream Technologies' BluePrint-PCB.

The benefits of using a dedicated, automated tool specifically designed for PCB documentation are many. As automation has reduced the tedious task of routing traces individually, so too have documentation tools reduced the tedium of creating and maintaining PCB documentation. An automated documentation tool can reduce documentation tasks, reduce errors, and offer greater efficiency. **PCBDESIGN**

Mark Gallant is senior product marketing manager at DownStream Technologies.

Documenting Intent With IPC-2581

by Amit Bahl
SIERRA CIRCUITS

Would a book be convenient if the chapters weren't bound, were scattered among different locations, required translation, and handwritten? That's akin to what PCB manufacturers face every day when piecing together Gerber files, drill files, board drawings, notations, netlists, BOMs, and pick-and-place coordinate files, to interpret what designers expect them to build.

That collection of files, none of which (except the Gerbers) share the same format, is almost always the way PCB designs are submitted for fabrication and assembly, except for a relatively few designs that are output in the ODB++ unified format. But salvation from the hodgepodge of design documentation is at hand, however, thanks to Revision B of the IPC-2581 standard for formatting PCB CAD data, which was released in late 2013.

In my November 2013 column, I wrote about how this standard consolidates all the data for a design into a single file that manufacturers can easily read, check to verify that the design is ready to build, and then use to drive CAM tools. The implementation of RevB by the CAD tool companies, DFM software vendors, and the CAM sector is underway. But there is far more in store for IPC-2581 to document designs as the standard evolves, as I learned from a recent conversation with Gary Carter. He is the senior manager of CAD engineering at Fujitsu Network Communications, and a founding member of the IPC-2581 Consortium.

Carter first pointed to what the revised standard already enables. "With the PCB stackup section that's been incorporated in RevB, we've eliminated the need for a profile drawing entirely," Carter began. I won't steal his thunder about that provision, other than to say it will facilitate interplay between a PCB designer and manufacturing resources at the outset of a project to nail down the

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DOCUMENTING INTENT WITH IPC-2581 *continues*

optimum stackup. He'll reveal the details on March 24 in a presentation at IPC APEX EXPO in Las Vegas. In fact, RevB eliminates the need for any drawings among the design data to convey build intent.

Carter explains, "We can render directly from an IPC-2581 file what otherwise takes several sets of drawings." He then referred to a network line card that has cutouts for optical modules, which was fabricated three-up per palette by several manufacturers as a demonstration project.

"There were the V-scores and the mills and drills, which along with the stackup structure used to involve a couple of different drawing sets," Carter continued. "Now, no drawings are required at all. You've got the specific tools spelled out in the file that are required for the V-cut, where those V-cuts are located, all described in a spec tied to that V-groove. The details on the milling outline can be described by '2581 so you know how that cutout is achieved. And by the way, back-drill information is also conveyed by '2581, so there's no requirement to specify that in a separate file set."

> ***The upshot is that the revised standard now in place reduces the number of files for export to just one, but provides much more thorough and coherent documentation to clarify build intent than the legacy method of conveying a design to manufacture.***

The upshot is that the revised standard now in place reduces the number of files for export to just one, but provides much more thorough and coherent documentation to clarify build intent than the legacy method of conveying a design to manufacture. This will include assembly operations. But wait, there's more on the horizon.

Carter envisions a bridge to product lifecycle management (PLM) environments, which integrate all data about a product from a systems perspective from cradle to grave, including but far from limited to parts and production processes. As he explained, PLM is intended to be a part-centered view of any object, which encompasses all the attributes that define each part of the object and whether those part descriptions apply to the preliminary stages of product development, whether a part is actively being sourced for the product, or whether it is obsolete.

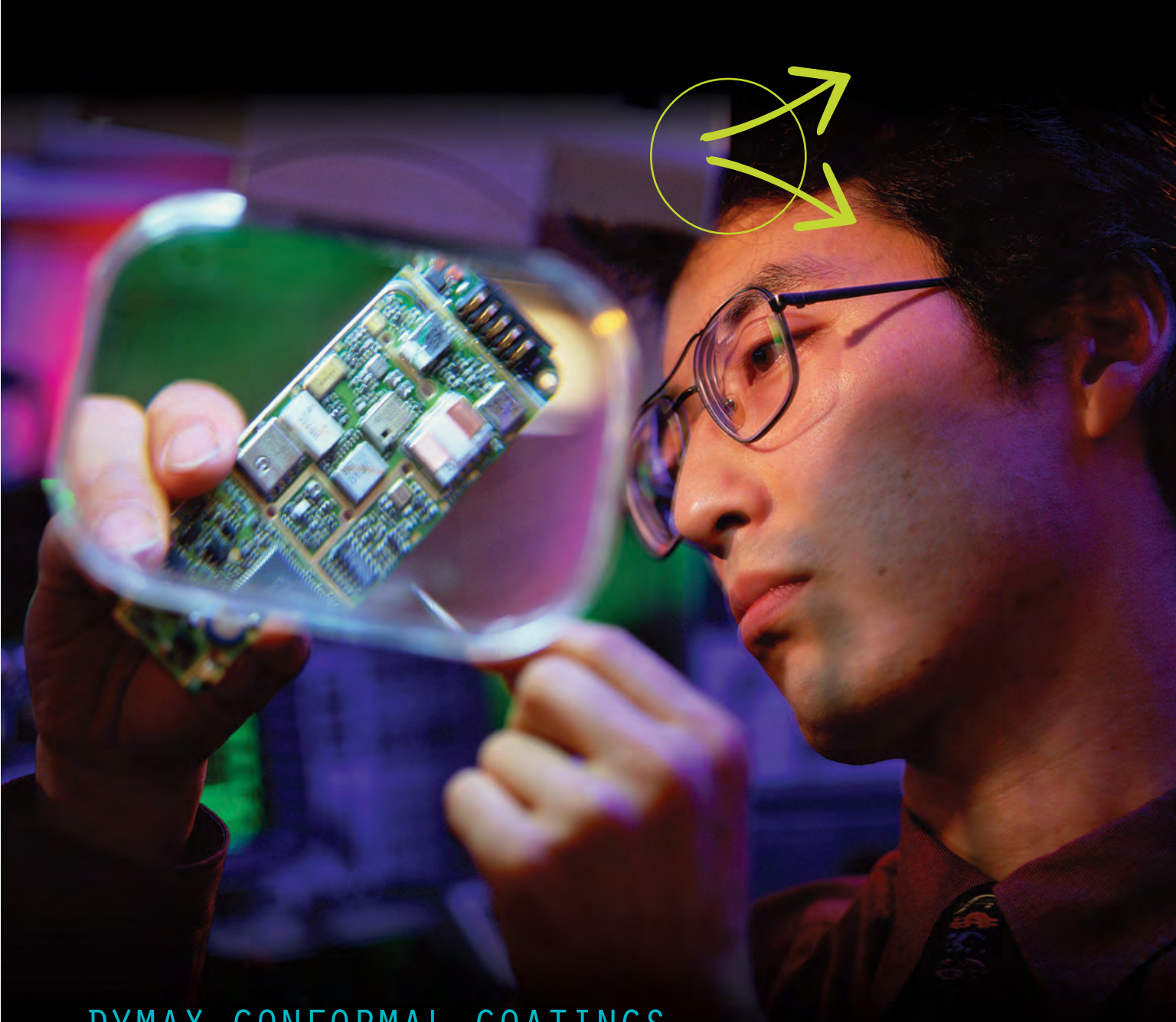
But Carter described a hook within the standard that could tie to more than hardware descriptions. "Contained in IPC-2581 is the ability to include external references to firmware configuration," he said, "so this is another aspect of the PLM story. I could export design data from my CAD tool into the PLM environment and thereby bring up a product configuration function that will be identified through the attributes I've assigned parts: 'Hey, I'm programmable. I need my reference guide to be related to a binary file that contains the program information that manufacturing needs to inject during the assembly process."'

Most likely, the IPC-2581 file will merely point to an external file that could have a part number, which would be the program file.

Carter added, "I believe there's even the ability to inject that into a dictionary inside IPC-2581, but I don't think I would ever do that. It would add too much burden to the size of the design file."

He speculated about sometime merging such mechanical elements as 3D rotatable parts views with the IPC-2581 domain. That's a story for future iterations of the standard. Meanwhile, at the moment, RevB is the most flexible, comprehensive way to document a design so that a PCB manufacturer will understand exactly what you intend to be built. **PCBDESIGN**

Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, CA. He can be reached by clicking here.



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PCB007 News Highlights

American Standard Circuits Earns "Manufacturer of the Year"

U.S.-based circuit board manufacturer American Standard Circuits (ASC) has been awarded "2013 Manufacturer of the Year" by the Alliance for Illinois Manufacturing. The award is intended to showcase a company that serves as a testimonial to the Alliance's integrated business delivery model.

Viasystems Reports 10.9% On-year Sales Growth

"We finished the year with some positive momentum that sets us up to continue to make progress on our cost structure in 2014, but in many ways I am glad that 2013 is behind us," said David M. Sindelar, CEO. "During the past year, we have worked through a number of challenges, including factory relocations, recovery from a fire in one of our largest factories, and new project launches, not to mention the economic pressures from reduced government spending."

Invotec Wins Formal ESA Approval

The company is delighted to announce it has been formally awarded ESA approva—the first PCB supplier to achieve such approval in many years. Invotec already has a rich space heritage, manufacturing HDI and HDI flex-rigid boards for a variety of ESA and non-ESA space programmes to OEM specifications which, in many cases, go beyond current ESA approvals.

IPC: North American PCB Sales Continue Slow Recovery

"North American PCB sales in December continued their slow recovery, while orders have been volatile," said Sharon Starr, IPC's director of market research. "In the current cycle, the book-to-bill ratio appears to have hit its low point in November and is now beginning to climb again."

Chinese PCB Firm DPMC Refutes Bankruptcy Rumors

China-based printed circuit board manufacturer Dalian Pacific Multilayer PCB Co. Ltd (DPMC) has denied rumors that the company is going bankrupt.

IPC APEX EXPO 2014 Proves Leadership; Space Sold Out

To visitors, the sold-out status means that the show floor will be busy and informative, with more than 425 exhibitors introducing new product technologies, innovations and demonstrations of the industry's newest advancements, many of which will also be highlighted in the dedicated New Product Corridor on the show floor.

MFLEX Doubles Sales to New Customers

Reza Meshgin, CEO, commented, "Net sales to our newer customers more than doubled sequentially, and are expected to represent approximately 23% of total net sales. Looking ahead to the fiscal second quarter, we expect a significant sequential decline in net sales that we anticipate could approach 40%."

Dragon Circuits Intros Pure Gold LPC for Medical Circuits

Texas-based circuit board manufacturer, Dragon Circuits (DCI) has announced immediate availability of their Pure Gold LCP, 100% pure gold traces plated on liquid crystal polymer (LCP) without the use of copper-base metals.

TTM Reports Strong Q4 and FY 2013 Results

"We delivered strong results for the fourth quarter as seasonal revenue growth combined with solid execution resulted in increases in gross margins and operating profit," said Tom Edman, CEO. "Strong demand for our advanced HDI and rigid-flex PCBs drove our product mix shift toward advanced technology PCBs and brought our Asia Pacific factory utilization rates above 90%."

Global Flexible PCB Market to Reach $12.686B in 2015

The FPCB market was valued at $11.321 billion in 2013, up by 9.4% year-on-year. In 2013, the most significant change in the industry was in the slumping profit margins of veterans and the soaring profit margins of new entrants. Market veterans lagged behind new entrants in equipment and technical R&D strength, according to market analyst Research in China.

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Tolerant of Tolerance?

by Martyn Gaudion
POLAR INSTRUMENTS

Wouldn't life be great if everything fit together perfectly? There would be no need for tolerance. However, for that to be the case, everything would need to be ideal and without variation. Therefore, unfortunately (or, maybe, fortunately), we all deal with measurements and materials and situations that are not ideal and are compromised in one way or another.

Often the challenge with tolerance comes down to misunderstanding, and the fact that we all now design with CAD tools which have levels of precision far in excess of the realisable parameters of the mechanical or electrical materials and measurement systems we deal with on a day-to-day basis. Poor understanding of tolerance or being intolerant of tolerance can lead to disappointment (see Figure 1).

Or, as attributed to Aristotle, "It is the mark of an educated mind to rest satisfied with the degree of precision which the nature of the subject admits and not to seek exactness where only an approximation is possible." That translation itself is, of course, only an approximation and requires an appropriate degree of tolerance, but you get the idea.

Looking back a few decades, it is clear that the challenge in terms of tolerance and dimensioning shifted with the move from analog to digital measurements, and electrically there is the beginning of a second shift where high-speed digital systems blur back into the analog realm.

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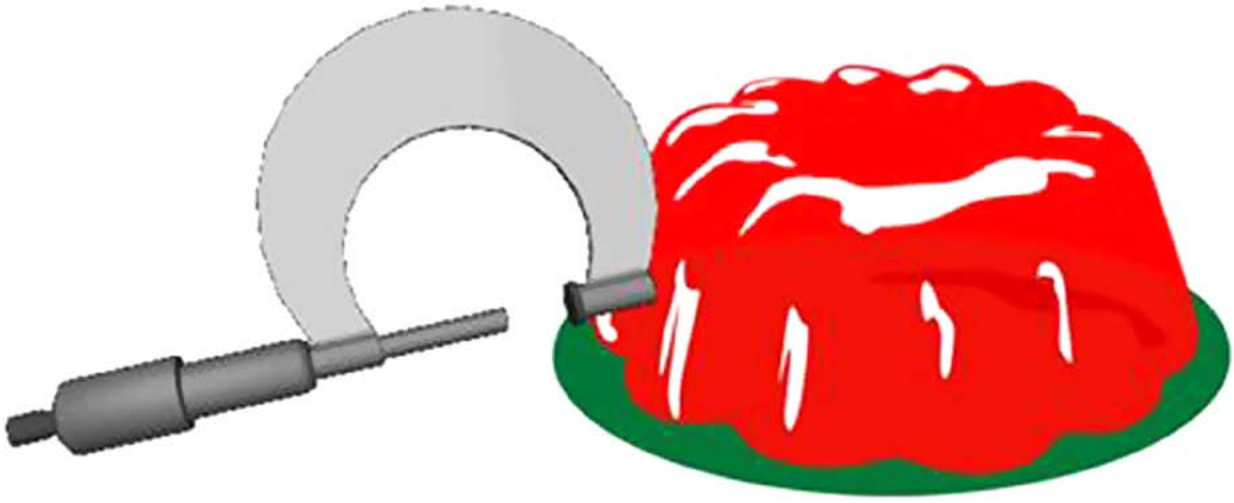

Figure 1: Misunderstanding tolerance can lead to disappointment.

Those of us in the industry for long enough can recall the move from analog voltmeters to digital and from vernier scale to digitally encoded micrometers and calipers. Digressing slightly, I recall a very analog moment when, as a naïve 11-year-old, I and a school friend decided to measure the current available from mains electricity—with an analog AVO meter (safety note: not a wise move!).

The result was a large blue flash, melted meter cables and a visit from the local electricity authority as we had vaporised the main fuse in the supply box. Fortunately, we are both still here, and I still use a trusty old analog AVO meter for electrical jobs around the house. Perhaps that's why I ended up with a career in the electronics industry, but I have to say it's not as exciting as that first experience, and maybe that's not a bad thing.

Back to tolerance. In a supply chain, problems set in when tolerances are set incorrectly or when the tolerance specified is unachievable. The story in the PCB industry dates back to the introduction of CAM and the ability to set hole tolerances far tighter than those achievable with the available drills or drilling machines. It is important that everyone in the supply chain understands what is achievable and what is not. The same is true for electrical measurement. It also comes as no surprise that a long, complex supply chain also has a lot to take on board as each particular measurement can present individual challenges.

Take electrical measurements: I have described how the nature of electrical measurement changes as frequency increases. The same is true for tolerance. When measuring at low frequencies, current, voltage and resistance are all capable of being measured with a high degree of precision with many decimal places of accuracy and tolerance on measurements can be tight indeed. But as the frequency starts to creep up it becomes harder to hold to such tight tolerances. At DC, tenths or hundreds of an ohm present little problem; but at mid frequencies, say, from 100MHz to 2GHz, then measurement of impedance presents more of a challenge. Perhaps a tolerance of 0.2 or 0.5 ohm is the best you can expect, and that depends on the impedance measured. Even the precision impedance air lines made traceable via NIST or NPL can present the user with a surprising amount of impedance uncertainty, limiting the achievable tolerance and absolute accuracy of measurement systems.

At even higher frequencies, resistance, voltage and current become even more tricky to measure, and RF engineers resort to power measurement, where the heating effect of the RF power is really the only way of measuring the gain or attenuation of a system, the voltages and currents being too elusive to measure.

This is why you will see, as designers push high speed digital to ever loftier transmission speeds, that insertion loss S21 or differential insertion loss Sdd21 is measured as a ratio of power into the line under test vs power out. The difference between the power in and out will be the insertion loss. Putting a tolerance on this type of measurement is tricky as the measurement of the loss will depend as much on the design of the test pieces as on the metrology instrument.

It is interesting to look at this from a distance as, to a casual observer, accurate low-frequency measurements need a good meter, but the probes can be quite simple and low in cost. As the frequency ramps up, shielding is often required, along with coaxial or transmission line probes. Additionally, the interconnect between the probe and the measurement system becomes a critical part of ensuring accuracy and repeatable measurements. At the highest frequencies, where ultimately a user may resort to a probe station, the probing system cost can be of a similar order to that of the measuring instrument. In fact, at high frequencies, all the parts of the measurement system need to be carefully crafted to ensure you can make accurate measurements within the desired tolerance; typically, the higher the frequency, the more the achievable tolerance widens out.

It is interesting to look at some VNA specifications regarding tolerance and accuracy: you will find that the measurement precision depends on a blend of factors, including the design of the test piece. For example, if a coupon is designed with a very high loss (almost complete signal attenuation) or very low loss (almost 100% transmission), it is hard to make an accurate measurement of loss per unit length. Samples therefore need to be designed with an appropriate loss depending on the base material used. Therefore, for low loss materials the coupons may need to be longer (loss is proportional to line length) than for a standard loss FR4 material.

> ***Some systems are very repeatable and sit well within their factory specifications, but the specifications are there for a reason; do not assume because your measurements are very repeatable that they are more accurate than the published tolerance of the measurement system.***

What increases your production tolerance?

First—and, seemingly, one that people miss—you need to allow for the tolerance of your measurement system. Some systems are very repeatable and sit well within their factory specifications, but the specifications are there for a reason; do not assume because your measurements are very repeatable that they are more accurate than the published tolerance of the measurement system. Given that you have accepted this and you are working within the limits of your measurement system, let's take a look at controlled impedance traces and the possible offenders which may cause some of your products to fall outside, or close to, their permitted tolerance. Cross-sections are important here. The primary drivers of impedance are dielectric separation and trace width. Trace thickness and dielectric constant are second-order effects. It follows then that variations in line width may cause traces to vary in their measured impedance. Taking several cross-sections can confirm if this is the case. As line width reduces, it becomes more difficult to achieve a given level of tolerance.

Surprisingly (to some designers, at least), the same is true for dielectric separation. The board thickness does vary in different parts of the PCB—copper density is a key driver of this—and it is essential to ensure the density of Cu is well balanced to ensure there are not excessive variations of height and therefore dielectric separation. Local variation of dielectric constant can also have an effect—witness the many papers on fiber weave mitigation—though, interestingly, low-twist fibres and mechanically spread glass can help this and perhaps in future the advances in glass design will reduce the need to deal with fiber weave variations in E_r.

It is interesting that spread glass is one of those rare win-win coincidences as it was originally developed to ease controlled-depth laser drilling, the resin being far easier to ablate than the glass. A side effect of the improved cloth is reduced regional variation in E_r. There is a third win here which no one saw coming: At very high (GHz) frequencies, the periodic variation in E_r caused by weave mitigation can cause high-frequency variation in the insertion loss characteristics, but that's for another article.

Summary

So, when specifying any measurement, you should ensure that the design authority (or supply chain procurement management) specifies realistically: that means both measuring within the limits of the capability of your measurement systems and recognising that in some cases an appropriate sample measurement test vehicle (coupon or sample material) is an important part of the measurement system.

Finally, the key to keeping tolerance as tight as economically possible is an understanding of the materials and processes that are the key drivers of the property you are measuring. And if you are still wondering if the AVO survived its traumatic measurement experience, well, yes, it did. **PCBDESIGN**

References

1. A Designer's Guide to PCB Tolerancing, Polar Instruments Application note AP521.

Martyn Gaudion, CEO of Polar Instruments Ltd., began his career at Tektronix in the early 1980s. He joined Polar Instruments Ltd. in 1990 and was appointed CEO in 2010. Gaudion also writes occasional articles for a number of PCB industry publications and regularly contributes to IPC high-speed, high-frequency standards development activities. To contact Gaudion click here.

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Welcome to the 2014 IPC APEX EXPO Show Guide

APEX EXPO IPC

CONFERENCE & EXHIBITION March 25-27, 2014
MEETINGS & EDUCATION March 23-27, 2014
Mandalay Bay Resort & Convention Center
Las Vegas, Nevada

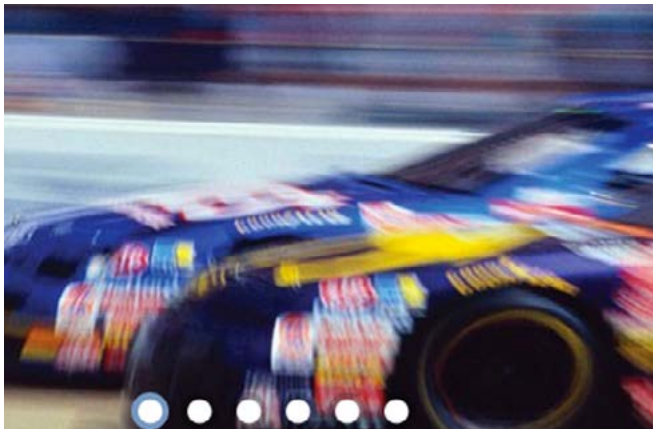
This year, the Mandalay Bay Hotel and Convention Center is the site for the industry's premier event, featuring 430 exhibitors from more than 50 countries. Featuring advanced and emerging technologies in printed board design and manufacturing, electronics assembly, test and printed electronics, APEX is a great place to find new suppliers with new solutions and connect with colleagues from around the world. Plenty of free offerings are on hand—follow these links for a complete online show brochure or event schedule.

Here are a few highlights of what attendees may expect include:

- 430 exhibitors showing equipment, materials and services for printed boards and electronics manufacturing—plus printed electronics! There›s no better place to see and compare.
- The largest technical conference for our industry in the world. Highly selective, the conference presents new research and innovations from experts in the fields of electronics assembly, test and board fabrication and design.
- FREE! Industry poster sessions—Catch up on the latest research and meet the authors.
- Professional development courses provide comprehensive updates on pressing industry concerns.
- Standards development meetings that help shape the future of our industry.
- IPC International Hand Soldering Grand Championship—Compete in or watch the excitement on the show floor.
- Other happenings on the show floor include the Show Floor Welcome Reception on Tuesday and a display of cutting-edge products and services in the New Product Corridor. There are also plenty of informational resources at the IPC Bookstore.
- Networking opportunities including an International Reception, First-Timers' Welcome, IPC Tech Talk, Women in Electronics Networking Meeting, and IPC Government Relations Committee Open Forum allow attendees to meet colleagues, get updates on key issues and share ideas.

To register to attend IPC APEX EXPO 2014, click here.

For an inside look at the show and in-depth interviews with industry insiders directly from the show floor, be sure to visit I-Connect007's Real Time With… site during the show. We're the only publication posting interviews and events in real time!



Free Keynote Addresses All Three Days!

APEX EXPO IPC

Opening Keynote Address:
Tuesday, March 25, 2014
8:30–9:30 a.m.

Peter Diamandis, M.D.
Creating a World of Abundance

Peter Diamandis, M.D., is a dynamic inspirational speaker and tech entrepreneur who will share his insights about how breakthroughs in exponentially growing technologies like artificial intelligence, nanomaterials, 3D printing, robotics and digital medicine will re-engineer products, companies, industries—and even society—over the next 20 years. Diamandis will explain how human society has evolved from "local and linear" to "global and exponential," and how this change has not only spawned the creation of new billion dollar start-ups out of nowhere, but also led to the demise of 50-year-old billion-dollar companies overnight.

Through his work as chairman and co-founder of Singularity University and chairman/CEO of X PRIZE, Diamandis has proven the transformational power that exponentially growing technology has on companies, governments and humanity—and on "do-it-yourself" technologists and small companies who can now achieve what only governments or large corporations could do before.

Day Two Keynote Address:
Wednesday, March 26, 2014
9–10:00 a.m.

James McLurkin
Swarm Robotics and the Toys, Movies and Insects that Made it all Possible

They will flock. They will swarm. And they will tackle the dangerous, dirty and dull jobs for which humans are inherently ill-suited. They're multirobot systems—and one day they will become the norm, according to roboticist, inventor, researcher and teacher, James McLurkin. Inspired by the complex group behaviors found in ants, bees, wasps and termites, McLurkin's work focuses on developing software and programming techniques for groups of autonomous robots with populations ranging from 10 to 10,000.

As a child, McLurkin was constantly playing with Star Wars® toys and building with LEGO® bricks, cardboard boxes and any other materials he could access. Today, armed with degrees in electrical engineering and computer science from M.I.T. and University of California, Berkeley, McLurkin continues to harness his inventiveness to develop the robot swarms that will one day perform jobs ranging from warehouse operations to search-and-rescue missions to Mars exploration. Don't miss this fascinating look at the future of robotics and the technology that is making it happen.

Day Three Keynote Address:
Thursday, March 27, 2014
9–10:00 a.m.

Diandra Leslie-Pelecky, Ph.D.
The Physics of NASCAR

How do you design and manufacture a car that will move at speeds in the neighborhood of 200 mph (321 km/h), yet handle with precision and, most important, keep the driver alive? What technology makes a NASCAR car different from the vehicles you see on the highway?

In a presentation based on her book, "The Physics of NASCAR," physicist and researcher Diandra Leslie-Pelecky, Ph.D., will take you behind the scenes of America's most popular spectator sport—and explain the feats of engineering that make NASCAR work. Drawing on her extensive access to NASCAR race shops, drivers, crew chiefs, engine builders and pit crews, Dr. Leslie-Pelecky will trace the lifecycle of a racecar, from its creation at leading race shops to competing in the action of the NASCAR series.

IPC APEX EXPO 2014

Free IPC APEX EXPO BUZZ sessions

Eight free BUZZ sessions will be offered at IPC APEX EXPO this year. The industry's top technical experts on subjects ranging from automotive and new technologies to conflict minerals, export controls and technology roadmaps will provide insights into timely issues. Admission to the BUZZ sessions and the exhibit hall is free to pre-registrants, a savings of $25 on-site. Click the link above for BUZZ session times and a complete schedule.

This year's BUZZ session topics:

- Underwriters Laboratories: Updates
- Advanced Fabrication Instruction Exchange Between Design and Manufacturing: The IPC-2581B Model
- Promoting Excellence: New IPC Standards for Reliability and Quality, and IPC Validation Services Program
- Forbidden by the Government: Electronics' Materials Restrictions
- INEMI Sustainability Forum
- Counterfeit Components
- What's Coming in 2015 in Electronic Technology Roadmaps

IPC PCB Supply Chain Leadership Meeting

Monday, March 24
8:00 a.m.–5:00 p.m. (includes networking breakfast, lunch and dinner)

A learning and networking forum exclusively for senior-level executives of PCB fabricators and their suppliers, this meeting focuses on issues related to executive decision making in the industry, such as market trends, customer requirements and the economy. Hear from noted industry experts and find out how your peers are addressing common challenges. To view the full agenda, click here.

IPC APEX EXPO 2014 Technical Conference

The IPC APEX EXPO technical conference is known worldwide as one of the finest and most selective in the world. Learn about new research and innovations from key industry players in the areas of board fabrication and design and electronics assembly.

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IPC APEX EXPO 2014

Professional Development Courses

Sunday and Monday, March 23–24
Thursday, March 27

This year, 29 professional development courses are being offered, with each three-hour course focusing on a critical issue within nine specialized areas, including: assembly processes for lead free and tin-lead soldering; cleaning, coating and contamination; design; emerging technologies; environmental issues and compliance; PCB fabrication and materials; printed electronics; quality, reliability and test; and supply chain/business issues. Course attendees will receive an instructional handbook to reinforce key information and use as a reference when they return to work.

Among the instructors leading the courses are Rainer Thueringer, Ph.D., Technische Hochschule Mittelhessen; S. Manian Ramkumar, Ph.D., Rochester Institute of Technology; Phil Zarrow, ITM Consulting Inc.; Jennie Hwang, Ph.D., Sc.D., H-Technologies Group; Ray Prasad, Ray Prasad Consultancy Group; Gerjan Diepstraten, Vitronics Soltec; and Mike Bixenman, DBA, Kyzen.

Click here for a complete list of professional development courses and instructors.

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Drop by the I-Connect007 booth to see for yourself how easy it is to find a fabricator, or create a Showcase listing!

Real Time with... Interviews and Panel Discussions

This year, I-Connect007 and the Real Time with... program returns to Las Vegas, Nevada to bring you complete video coverage of IPC APEX EXPO 2014. Last year, we brought you more than 150 interviews—and this year promises to be just as prolific.

The Real Time with… team of editors, guest editors, and videographers will be working throughout this seminal event to capture the keynotes and bring you one-on-one interviews and panel discussions with the industry's top technologists, engineers, and business leaders as it happens!

Visit Real Time with... for updated information about IPC APEX EXPO 2014.

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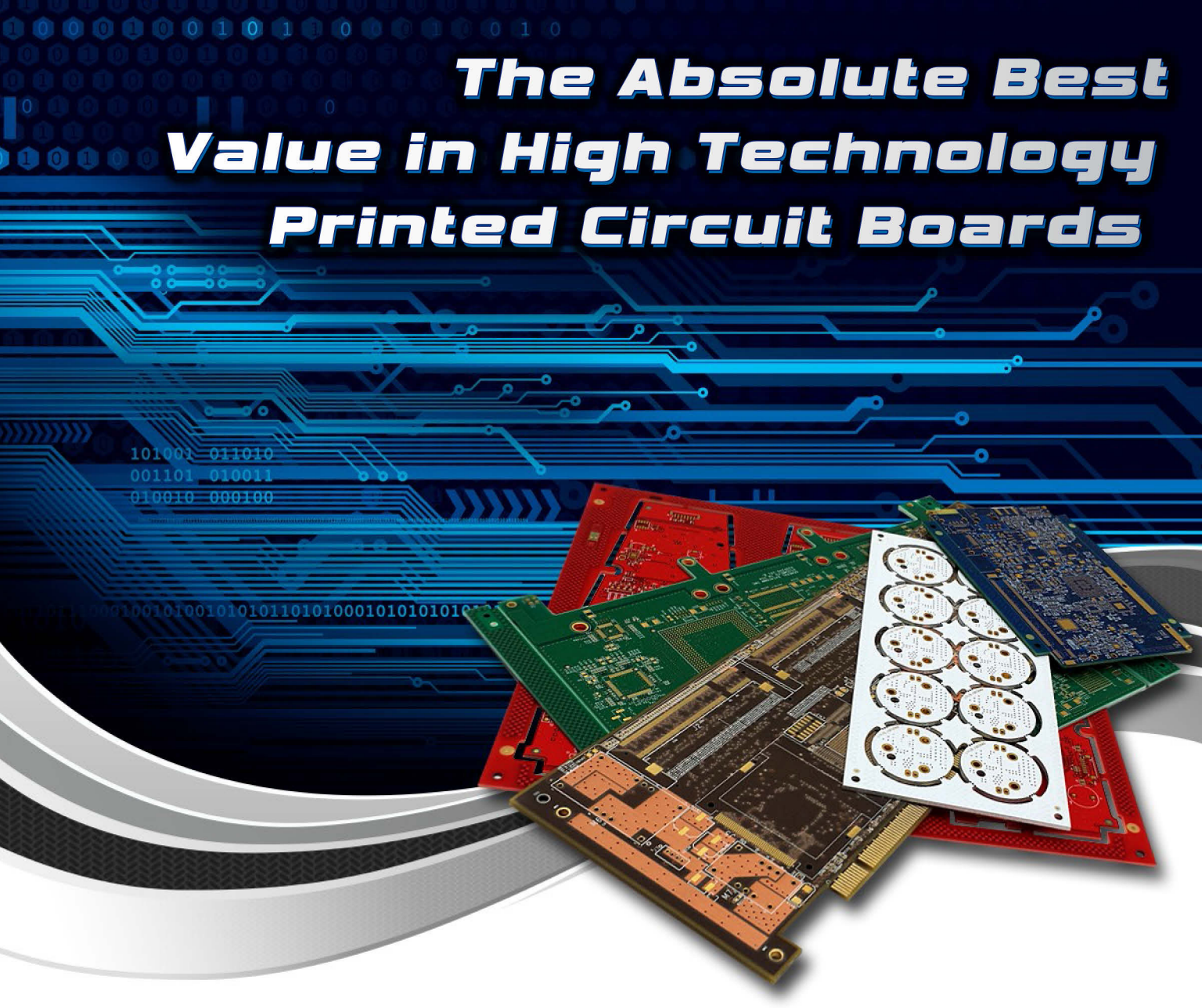

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Differential Education 101 for PCB Designers

by Dan Smith
RAYTHEON MISSILE SYSTEMS

What is the state of PCB designer education in 2014 and where is it going? Where should it be going? My new column will focus on PCB design, design processes, education and a host of topics that are important to PCB designers.

As such, I would like to hear from PCB designers and their managers about where their minds and dollars are headed regarding staying at the head of our industry.

Let's get started! Solve this equation:

$$\frac{\partial u}{\partial t} = 6u\frac{\partial u}{\partial x} - \frac{\partial^3 u}{\partial x^3} \quad \text{Eq. 1}$$

The average time to solve this is three minutes. For those of you who remember differential equations, have fun. For the rest of you who are resolved not to attempt this problem and are now feeling your blood pressure going down, I would like to explore the state of formal and informal PCB designer education.

Before I attack the problem in this new column, I am dividing my thanks (historically) to four distinct groups of formal and informal educators in the PCB educator community.

First, I'd like to thank all of the PCB design educators who have tirelessly taught around the globe and written articles and books to offer their insights. For those who are unfamiliar with the educator's rule of "class preparation time," as a minimum, one minute of class lecture or lab requires a minimum of five hours of research and preparation. If the assembled students ever cared to realize why many teachers look tired but feel enthusiastic during these formal courses, it is because these same educators live for the "Aha!" moment of joy they see on their students' faces. There is no dollar amount that can equal this moment that educators live to see.

Second, a big thank you goes to those who have participated in industry and company-specific design standards and practices. These participants collectively put in the range of in-

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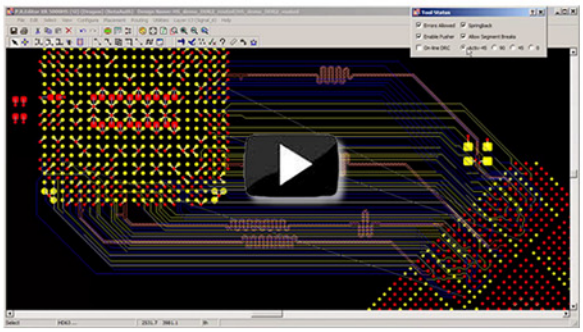

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DIFFERENTIAL EDUCATION 101 FOR PCB DESIGNERS *continues*

finite man-hours, just to get their thoughts on paper so that others can grow their skill sets exponentially. This same participating group gets inversely proportional amounts recognition, usually little or none.

Third, to all of the EDA tool vendors, thank you for showing us how to use these tools so that we can become more productive. They have taken a wide variety of ideas, equations, and other theories, and synthesized them to formulate tools that have subtracted hours, weeks and months from design schedules. All the while, these companies have helped us understand and master the additions of newer design concepts, such as high-speed signals and HDI via stackups.

Lastly, we need to recognize that the majority of growth and education is actually indebted to the PCB design community itself, who have remained a positive force at seminars, webinars, and vendor fairs.

If all four of these groups were put into the denominator, from any starting point in the past few decades, the numerators of the participation for each of these groups would slowly approach the absolute zero of Lord Kelvin.

Businesses (and society in general) prefer to align themselves with formal education (degrees, awards, and certificates) rather than informal education (i.e., the school of hard knocks), because it affirms that a person has participated in a structured environment and attended a minimum set of science-based foundational courses.

Yet it is the formal educational model that has never materialized for our industry.

Formal education provides the best foundation for growth as a subject matter expert, but education is also now a business. Yes, there are rankings of the top schools for each vocation, but it is also about the economics of providing a curriculum that will attract the most money from students, alumni, industry, and special interest groups.

“Informal education flourished when major companies’ engineering teams actively participated with the manufacturing community. Side “special projects” of experimentation allowed for discoveries and inventions that created advancements in the PCB design process. But as interest and money was diverted away from these projects, informal education opportunities dried up.”

Informal education flourished when major companies’ engineering teams actively participated with the manufacturing community. Side “special projects” of experimentation allowed for discoveries and inventions that created advancements in the PCB design process. But as interest and money was diverted away from these projects, informal education opportunities dried up.

The PCB design process has been stable for more than 20 years. The only significant PCB educational push in the past 10 years has focused on better understanding the physics of the newer devices and their interaction with the substrate interconnections.

When new PCB design articles are written, the most effective way to distribute this content is through the Internet. The weekly/monthly distribution of these articles has caused me to take a step back and notice a significant education void that boils down to three high-level questions:

1. Why aren’t these PCB design process articles being channeled into formal courses, lab experiments and textbooks?
2. Why hasn’t there been an industry push to create a complete and consistent curriculum that could be taught by every technical college in the world?
3. Is the PCB user community content with the current education situation, or do they want more than what is being offered?

Instead of just reading more personal observations, it is far more productive for me to offer you, the PCB designers and managers, a chance to supply some of your thoughts by participating in an e-mail survey. Editor Andy Shaughnessy and I want to hear your collective voices, and we will publish the results for all to see.

Thank you for reading this column, and more importantly, thank you in advance for your feedback.

To take this short survey on PCB design and design education, click here. Next month, we'll go over the results. See you next month!

PCBDESIGN

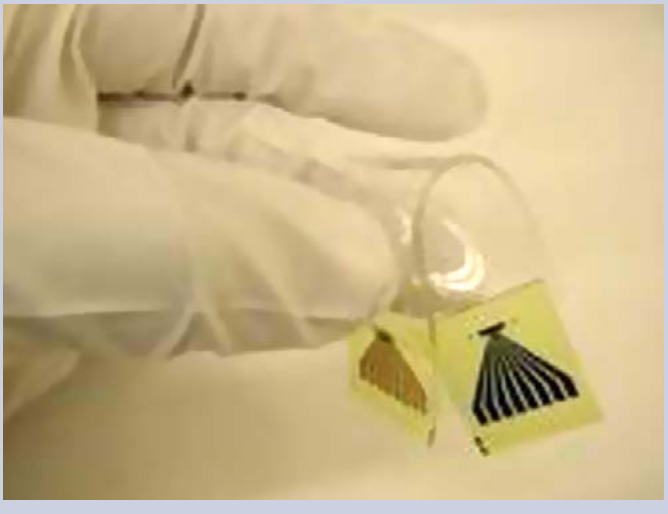
Ed: This series on design education will continue for the next few months. Dan wants your feedback, so don't be shy. You may even see your name in an upcoming edition of "The Town Crier."

Daniel J. Smith is a principal technologist for Raytheon Missile Systems. He has taught multiple aspects of the PCB design process internationally, and he has authored several PCB-related patents, articles, and standards over the past 30+ years. To contact him, click here.

Optical Circuits Flexing Their Way to the Forefront

For futuristic applications like wearable body sensors and robotic skin, researchers need to ferry information along flexible routes. Electronics that bend and stretch have become possible in recent years, but similar work in the field of optics--communicating with light instead of electrons--has lagged behind.

Now a team of Belgian researchers reports progress on this front with what may be the first optical circuit that uses interconnections that are not only bendable, but also stretchable. These new interconnections, made of a rubbery transparent material called PDMS (poly-dimethylsiloxane), guide light along their path even when stretched up to 30% and when bent around an object the diameter of a human finger.



Until now, the researchers say, no one had discovered a way to enable these materials to carry light while stretched. Past efforts also included embedding waveguides made of semi-rigid glass fibers into a stretchable substance. In the new method, the stretchable substance itself is the waveguide.

The new connector consists of two materials, both made of PDMS: a transparent core through which the light travels, surrounded by another transparent layer of PDMS with a lower refractive index, a characteristic of the material that describes how light moves through it.

Bending a waveguide beyond a certain point causes some of the light trapped in the core to escape, a process called optical loss. The Belgian team tested how far they could bend and stretch their new optical connector before too much light escaped.

"We were surprised that stretching had so little influence on the waveguides and also that their mechanical performance was so good," Missinne said. The guide's reliability was also "remarkable," he said.

This work has been performed at the Centre for Microsystems Technology (CMST), a laboratory associated with imec and Ghent University.

Properly Designing PCB Footprints

by Nicholaus Smith
INTEGRATED DEVICE TECHNOLOGY INC.

Today the geometries of board-level circuits are being driven to optimize space, cost, and performance, resulting in a large selection of fine-pitch components, connectors, and integrated circuits. Overcoming the challenges and the complexities of the circuit is challenging enough without considering the obstacles of mass producing the end-product with extremely high yield expectations.

Improperly defined PCB footprints are the culprits behind thousands of costly, time-consuming failure analysis investigations. For the sake of simplicity, it will be assumed that the circuit and all connections are schematically correct and any failures are the result of unreliable footprint designs assembled properly onto the PCB. The most common failures are caused by solder shorts or open circuits that develop during assembly. Other potential defects include poorly contemplated pin escape routing, improper thermal design, and the dreaded intermittent failure.

It is imperative to implement PCB layouts with a strong understanding of the assembly process and how the PCB component footprint can influence yield and performance. This is especially important today, due to factors such as: (a) the expansion of integrated circuit product lines manufactured with pin pitches specified at 0.4 mm and below, and (b) the plethora of package variations available, such as chip scale packages (CSP) and quad flat packages (QFN) in double and single rows.

Prior to addressing footprint design techniques, we must define some layer definitions used in PCB manufacturing, and explain how these layers impact the final board. The pin will be identified as the actual solder contact point

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that is used to mechanically and electrically connect the package to the PCB. Once the PCB has been etched, laminated, and the vias have been electroplated according to design, the next process step involves solder mask application to the outer surfaces of the PCB using printers, photo-masking, and radiation hardening. The role of the solder mask is to keep the solder on the pin during reflow. The solder paste is applied during assembly and is controlled by a layer called the paste mask.

Regarding the final PCB, all of these layers are geometric shapes that are drawn during footprint generation and are intended to facilitate connecting the pins of the device to the PCB. At this point the board would be blank with openings in the solder mask webbing at each pin. It would then be placed into a solder paste application machine where a 4-mil-thick stencil with laser-cut openings matching the pin etch is placed over the board, and then solder paste is applied by a squeegee sliding across the stencil, forcing solder paste onto each pin.

The stencil is then removed, leaving solder on the pins of each component. The solder paste is comprised of a slurry of flux and lead-free solder spheres, and it sticks to the PCB pins and not to the stencil due to the stickiness of the flux and surface tension. Finally, a pick-and-place machine puts each part in the defined locations and rotations; then the PCB is conveyed through a reflow oven. After assembly, the boards are tested and any failures are categorized; the root cause analysis is conducted assuming the percentage exceeds permissible yield limits.

Now a CSP will be considered and footprint design for high yield will be the focus. The most important aspects of any component are the pin geometries, pitch, and the package keepout. The pitch is the spacing from the center of a pin to the next adjacent pin. The keepout is the area defined around the component; it is intended to force the designer to provide sufficient clearance between components, so that they do not interfere with each other during placement and reflow.

When designing the footprint for the package drawing shown in Figure 1 with a pitch of 0.4 mm, key factors will be:

a) specifying the solder mask so that it is guaranteed to be applied in between each pin without overlapping any pins

b) specifying the pin diameter for consistent even soldering

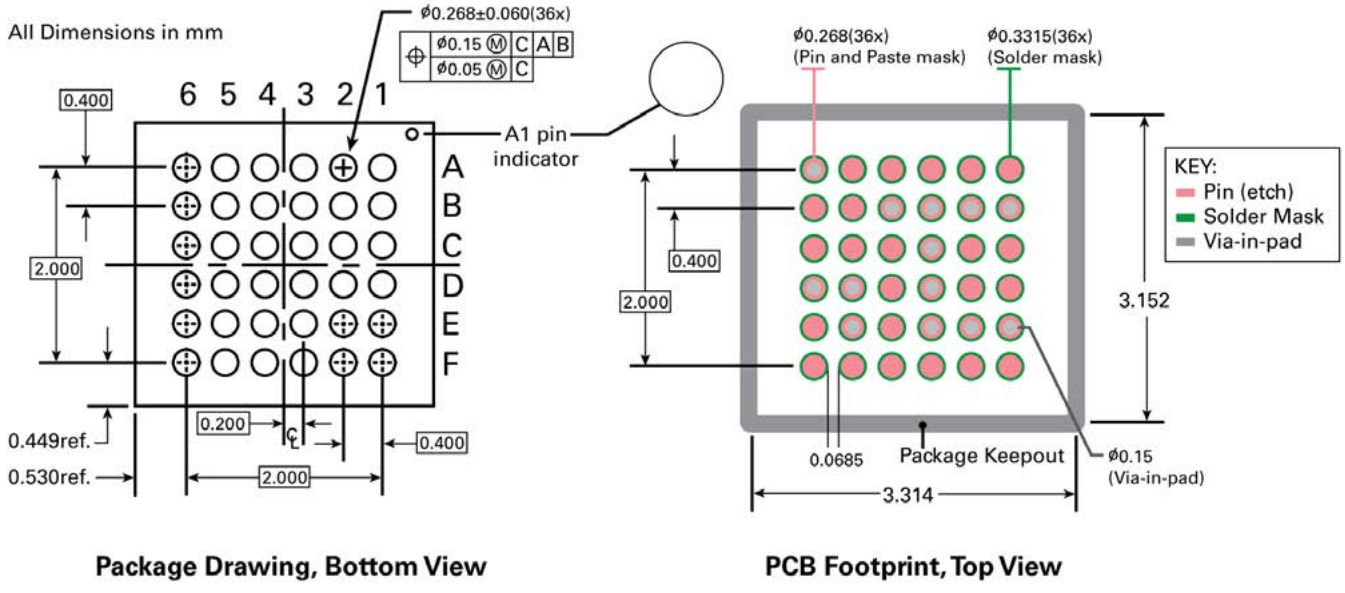

Figure 1: 36-pin CSP packaging diagram used to hold an IDTP902x wireless power receiver IC.

c) determining a via-in-pad that will allow for PCB manufacturers to reliably drill and plate the inner pins so they may be contacted using non-component side layers of the PCB

Most PCB manufacturers are able to apply solder mask down to 0.0635 mm (2.5 mils) and will guarantee that they can create a void in solder mask down to the same size. Therefore, to be certain every PCB will have solder mask applied between each pin while keeping the pins free from solder mask, it is recommended that at least 0.1905 mm of clearance is maintained in between each pin. This is equal to having two solder mask void widths (one for each pin) and one application width (gap between pins).

For this package, the ball size is 0.268 mm +/- 0.06 mm with a pitch of 0.4 mm that leaves only 0.072 mm in between the pads if we design for the maximum possible diameter. This will leave insufficient separation for solder masking to be reliably applied; therefore it is not acceptable to design the pin diameter at 0.328 mm. Now faced with a tradeoff, the highest yield design option is to apply the necessary solder mask bridge between pins and sacrifice the solder mask void.

This tradeoff is valid because the diameter of the pin will be included in the solder mask free area which will allow for adequate registration of the void, while giving the PCB manufacturer the needed solder mask width for guaranteed application. By specifying the pin diameter at 0.268 mm and the solder mask void diameter at 0.3315 mm, this leaves 0.0685 mm for solder mask, which provides crucial extra width since insufficient solder mask will lead to solder shorts under the package. Solder shorts under such packages are impossible to repair without removing and replacing the IC, an operation with lower success rates than the original assembly, due to the complication of applying a single device in a congested area on a potentially suspect footprint. With these diameters, the clearance from the solder mask to the pin is only half of the recommended clearance of 0.0635 mm; however, since the solder mask is not applied over the pin, that area is included in the void, thus the risk of having solder mask on the pin is reduced.

Even if the pin does get partially covered, the risk is that the electrical connection could be reduced by up to 12% of the available pin area. This compromise still leaves 88% guaranteed contact area between the CSP pin and the PCB pin, thus allowing even PCBs created on the low end of the tolerance band to still function with most likely unnoticeable defects. Another complication with such a device is the need to use via-in-pads to access the inner pins (rows B–F and columns 2–5) followed up by back-filling the vias so that the pins may be plated on the surface until they are flat and even with the rest of the PCB copper.

> ***Even if the pin does get partially covered, the risk is that the electrical connection could be reduced by up to 12% of the available pin area.***

Typical vias require that the finished pad diameter is 0.127 mm wider than the finished plated hole diameter and the typical minimum via diameter without a surcharge is 0.127 mm–0.1524 mm. For the 0.268 mm pins requiring vias-in-pad, the solution is to avoid using the minimum via while still allowing for manufacturing tolerances, thus a 0.15 mm via is recommended, leaving only 0.059 mm of pad diameter for registration and drill tolerance. Once the hole is drilled, the selection of the filling material should be considered.

There are two types of back-filling material in use: conductive and non-conductive. Besides the obvious difference, it should be noted that even the conductive fill material conductivity does not approach that of copper (electrically or thermally) and most have expansion coefficients that are very different than the surrounding via wall. During temperature variations of the PCB, non-conductive fill more frequently stretches and cracks the thin via walls compared to its counter-part, causing a higher percentage of intermittent or permanent failures. On the

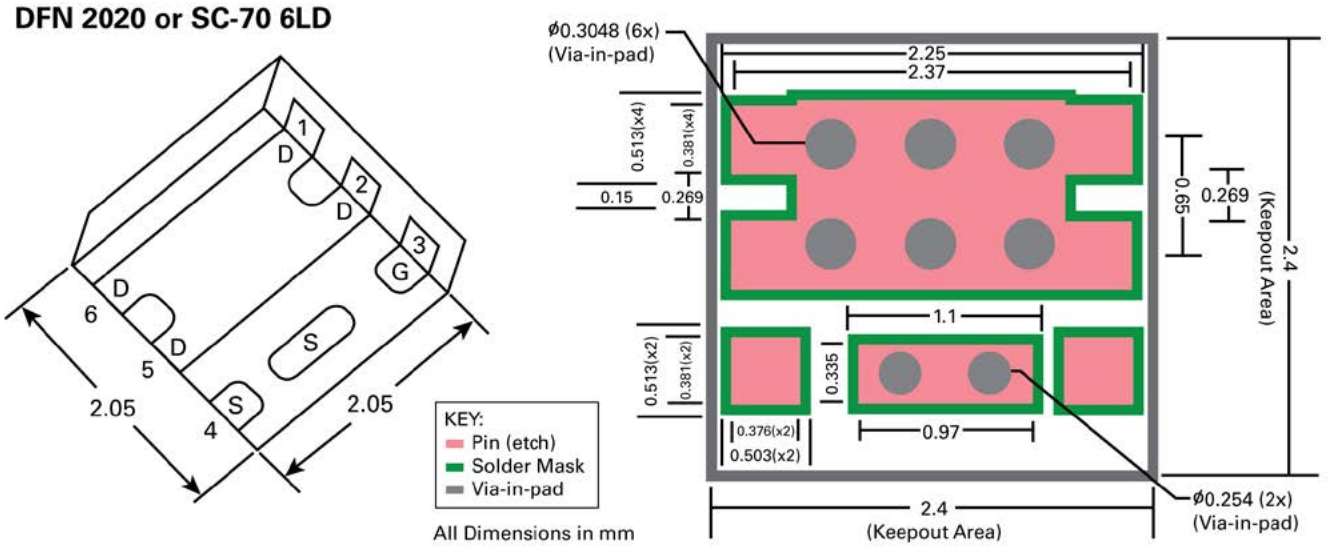

Figure 2: DFN 2x2 mm 6 LEAD (SC-70 6LD) single transistor package.

other hand, non-conductive fill materials coefficient of expansion is typically closer to the vias plating and since the via plating will conduct the majority of the current and potential heat regardless of the type, the non-conductive fill is recommended for most applications. Finally, the package keepout should be specified such that at least 0.127 mm of free space surrounds each package in every direction.

On such fine-pitch components, there are layout techniques that should be implemented to improve yield by reducing the chance of solder shorts or open circuits and that is to not place solid copper planes under the pins on the component side of the device. Adjacent pins that need to be connected to each other electrically should be connected using vertical and/or horizontal traces that match, or are less than the pin diameter in width in a grid type of an array. This is recommended so that in case the solder mask chips under the device during solder paste application (or for any reason), the risk of shorts or open circuits is greatly reduced because the solder will have fewer opportunities to excessively accumulate or spread away from the pin location during assembly.

The next package under inspection is the DFN 2x2 mm or SC70 6 lead device, typically used to hold power transistors or other miniature integrated circuits. Such devices are still relatively small, but they have slightly larger geometries than the CSPs from above and allow the designer to follow standard PCB manufacturing process capabilities. For example, on this device the solder mask voids and applications can be set to 0.0635 mm or greater, and the listed dimensions in Figure 2 are recommended for the pin, solder mask and paste mask sizes. Furthermore, such devices contain quite small silicon and usually need to spread the heat developed away from the die in an effective manner in order to keep the operating temperature to an acceptable level. Vias-in-pads are necessary in order to utilize inner layers to spread the heat from the package into the PCB. The significant design challenge is to maintain 0.127 mm or more of etch surrounding each via for ease of plating and manufacturing. The spacing and diameter of such vias may vary from package-to-package based on available space and the number of vias will substantially improve the operating temperature of the device[1].

As can be seen in Figure 2, the lower center pin does not have 0.127 mm of etch on the top or bottom of the two vias; this is still acceptable since the vias have extra surface area on each side. When a through-hole is designed and 0.127 mm of pad ring cannot fit, creating an ob-

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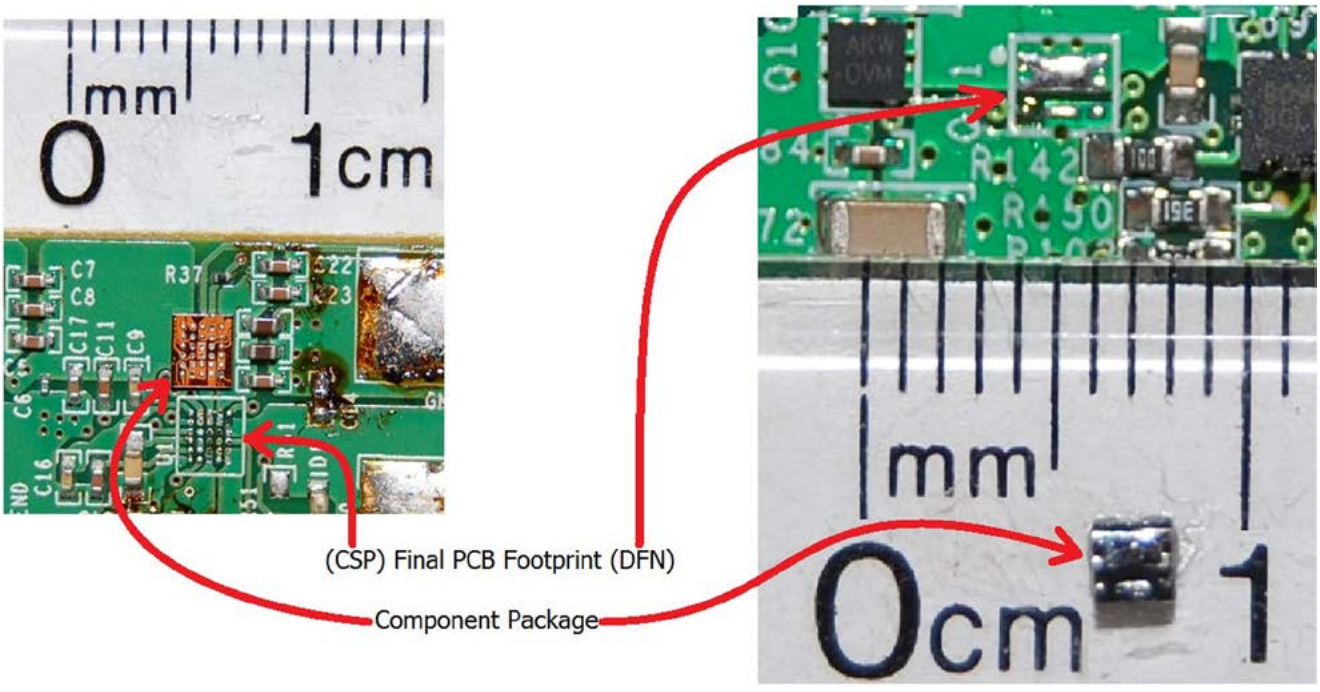

Figure 3: Final assembled CSP and DFN (SC70) footprints in use on PCBs.

long-shaped pad will ensure enough surface for consistent and even via plating, even though the recommended pad ring diameter has been violated. For both of the packages discussed and for almost every surface mount component, it is recommended that the paste mask openings match the pin etch and that the stencil thickness is appropriately thick for the pitch to insure proper fillets are developed at soldering. For the devices discussed, 0.1 mm is recommended, but for larger pitch parts, thicker stencils may be required.

Another aspect that influences yield is the selection of the solder paste. Normal solder pastes are specified according to sphere size, volumetric count and the cleaning process. For small pitches and pins hidden by the packages, it is often necessary to use highly active fluxes to be sure the solder will properly wet and form a solid bond between the pin and the PCB. At the same time, it is also important that the flux is easily clean-able so caustic residues do not remain on the final PCB.

In Figure 3, CSP and DFN (SC-70) packages and final footprints are shown. It should be noted that the green solder mask is present in between every solder connection, guaranteeing a robust and consistent assembly when produced in low or high volumes, designed with a consideration of manufacturing cost-adders and yield. The final product when implementing such designs will be durable, high yields produced at the lowest possible cost. **PCBDESIGN**

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Nicholaus Smith is an applications engineer at Integrated Device Technology Inc.

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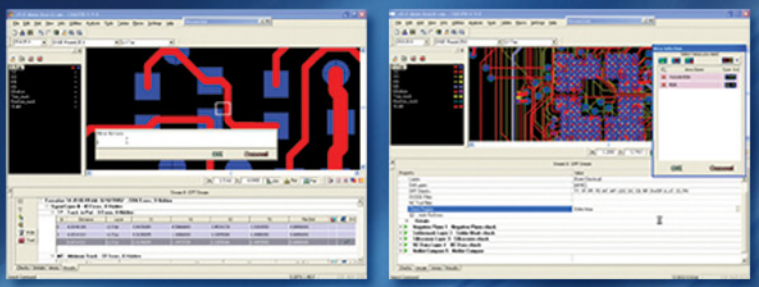

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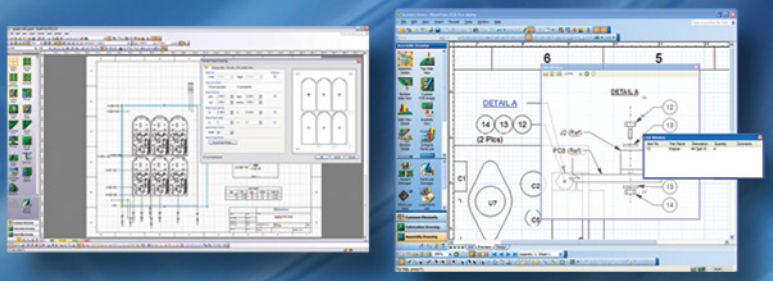

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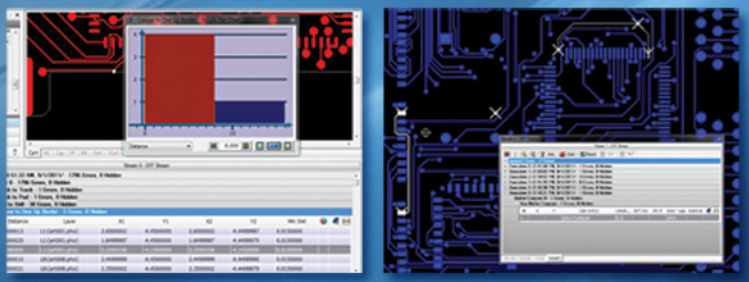

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Matched Length ≠ Matched Delay

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

In previous columns, I have discussed matched length routing and how matched length does not necessarily mean matched delay. But, all design rules, specified by chip manufacturers regarding high-speed routing, specify matched length—not matched delay. In this month's column we'll take a look at the actual differences between the two.

Typically, more than one layer change is required when routing traces to matched length. Figure 1 illustrates the DDR2 address bus routing I did in Altium Designer, my preferred lay-

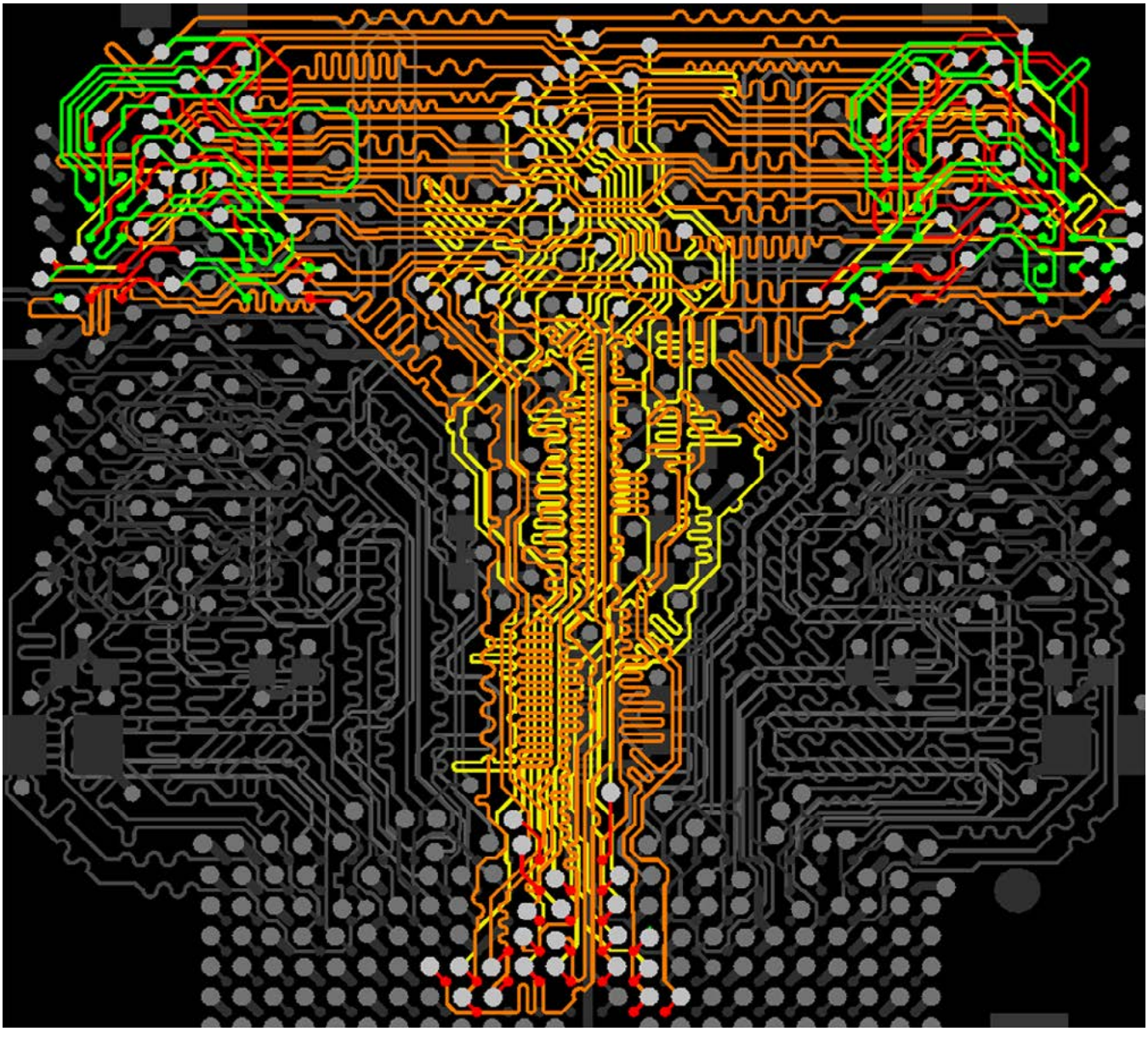

Figure 1: Matched delay T-section DDR2 address routing in Altium Designer.

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Matched Length ≠ Matched Delay *continues*

out tool. In this case, each address signal has four layer changes. The red and green traces are the top and bottom layers—which should be kept as short as possible—and the yellow and orange traces are inner layers embedded between the planes. This was a particularly difficult route as there were two DDR2 memory chips placed on both the top and bottom sides of the board, so each address signal had to go to four different chips and still maintain the correct delay.

The longest routes should be placed on the inner layers as this reduces electromagnetic radiation. With all other factors being equal, generally, a trace routed on the inner stripline layer exhibits 4–10 dB less noise than a trace routed on the outer microstrip layer. Also, please note that there are more high harmonics on the top layer routing. The high-frequency components radiate more readily because their shorter wavelengths are comparable to trace lengths, which act as antennas. Consequently, although the amplitude of the harmonic frequency components decreases as the frequency increases, the radiated frequency varies depending on the trace's characteristics.

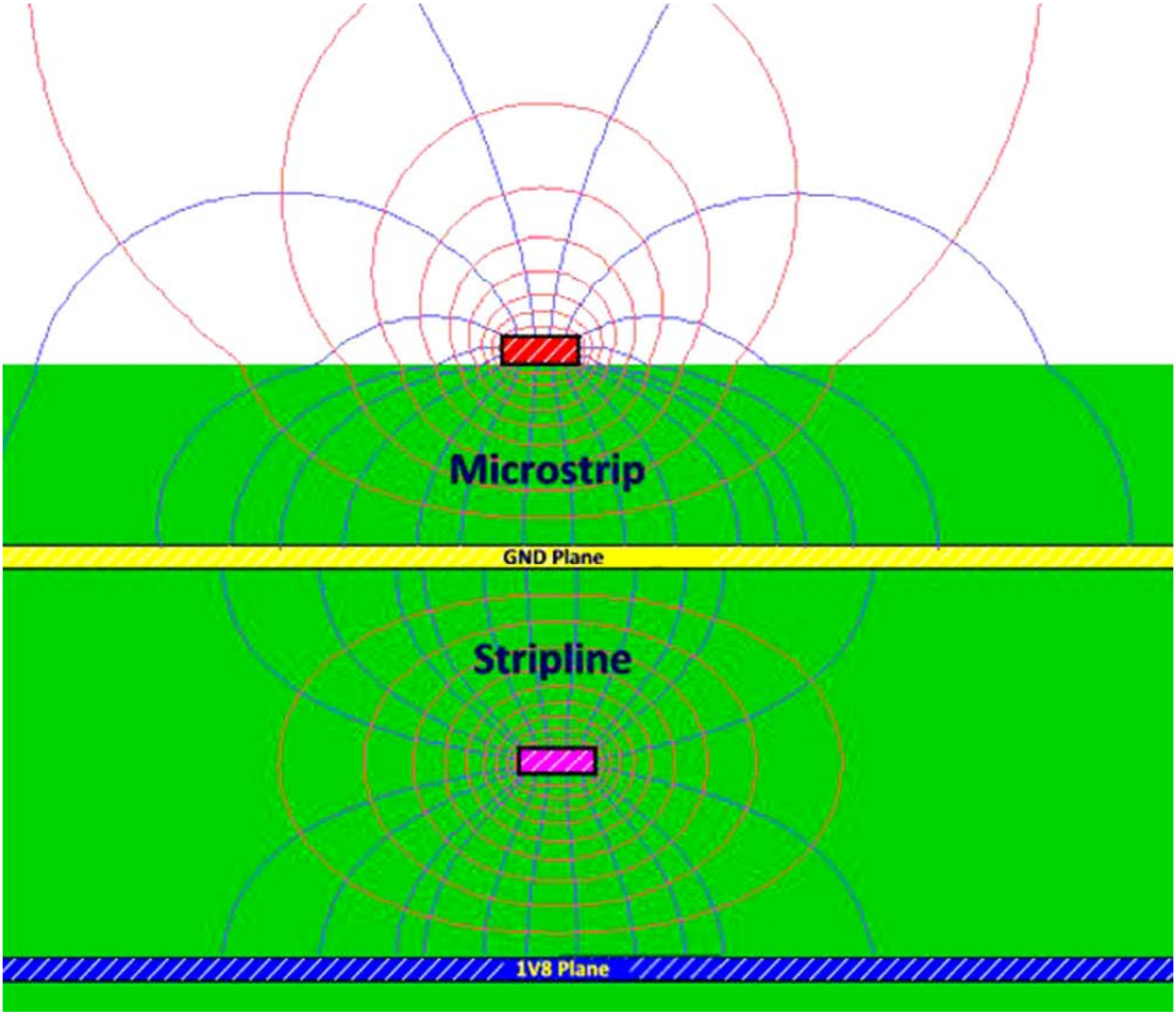

Figure 2: Electric (blue) and magnetic (red) field lines radiation from microstrip and stripline layers.

Microstrip layers are those that are fabricated on the outside of the substrate, top and bottom. Traces on these layers are referenced to the plane below/above, whether it be a ground or power plane. The trace has a dielectric material on either side: FR-4 below and air above. If you look closely at Figure 2, you can see where the field lines refract as they pass from the FR-4 (green) to the air dielectric. This is because the dielectric constant of FR-4 for example (~4.3) changes to air (1.0). The electric field is absorbed by the plane on one side and both the electric and magnetic fields also radiate into the air.

Stripline traces however, are totally embedded in dielectric material between planes. This may be a combination of materials—and dielectric constants—if for example multiple prepregs are stacked to obtain the desired thickness. The electric field is completely contained within the dielectric and blocked by the planes. The magnetic field still tends to radiate, from the board edges, but is limited somewhat.

Since the electromagnetic fields of microstrip layers partly reside within the surrounding air, the speed of propagation of a signal traveling on the microstrip trace is therefore partly determined by the dielectric properties of the PCB material and partly by the surrounding air. Microstrip traces are usually faster than stripline traces because the dielectric constant of air is lower than that of FR-4.

There are two exceptions to this:

1. If you use a microstrip prepreg with a high dielectric constant (Isola 370HR, 3.92) and in the stripline configuration a low dielectric constant (fastRise FR-27 & TSM-26, ~2.7) as in Figure 3. The combination of air (1.0) and Isola 370HR (3.92) brings the total dielectric constant to approximately that of the Taconic fastRise materials, thus the traces exhibit a similar delay.

2. If you add a liquid photo-imageable solder mask, with a dielectric constant of say 3.3, to the outer layers, then the microstrip delay changes again. So it is best to compare the delays using a simulator otherwise you are just guessing.

Contrary to what you may believe, the propagation delay of a serpentine trace is less than the delay through an equivalent length straight trace. The signal is sped up because a portion of the signal will propagate perpendicular to the serpentine. And, this also varies with the type of serpentine pattern used. For example, the serpentine pattern may have long parallel lengths spaced close together in the "U" bend coupling the signal many times through the serpentine pattern. This self-coupling (forward and reverse crosstalk) shortens the electrical path. But in theory, the forward crosstalk—far-end crosstalk—does not exist in the stripline configuration. Please see my previous column, Beyond Design: A New Slant on Matched-Length Routing, for further details.

Also, if two traces of equal length are referenced to different planes, then the return paths may be considerably different and add round-trip delay. This cannot be simulated, so it is important that the return paths are determined to be as short as possible. If planes are changed, then stitching vias or capacitors need

2 Layer | 4 Layer | 6 Layer | 8 Layer | 10 Layer | 12 Layer | 14 Layer | 16 Layer | 18 Layer

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Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
1	8 4 4	Signal	Top	Conductive			1.4	6	6	0.42	52.46	92.91	
		Prepreg		Isola 370HR ; 2113 ; Rc= 56% (10GHz)	3.92	3.6							
2		Plane	GND	Conductive			1.4						
		Core		Taconic TSM-26; (10GHz)	2.6	3.5							
3		Signal	Inner 3	Conductive			1.4	12	6	0.42	47.13	91.84	50.06
		Prepreg		Taconic FR-27-0042-75; (10GHz)	2.73	5.2							
4		Signal	Inner 4	Conductive			1.4	12	6	0.42	47.13	91.84	50.06
		Core		Taconic TSM-26; (10GHz)	2.6	3.5							
5		Plane	1V8	Conductive			1.4						

Figure 3: Isola 370HR (microstrip) and fastRise FR-27 & TSM-26 (stripline) exhibit similar delay.

Matched Length ≠ Matched Delay *continues*

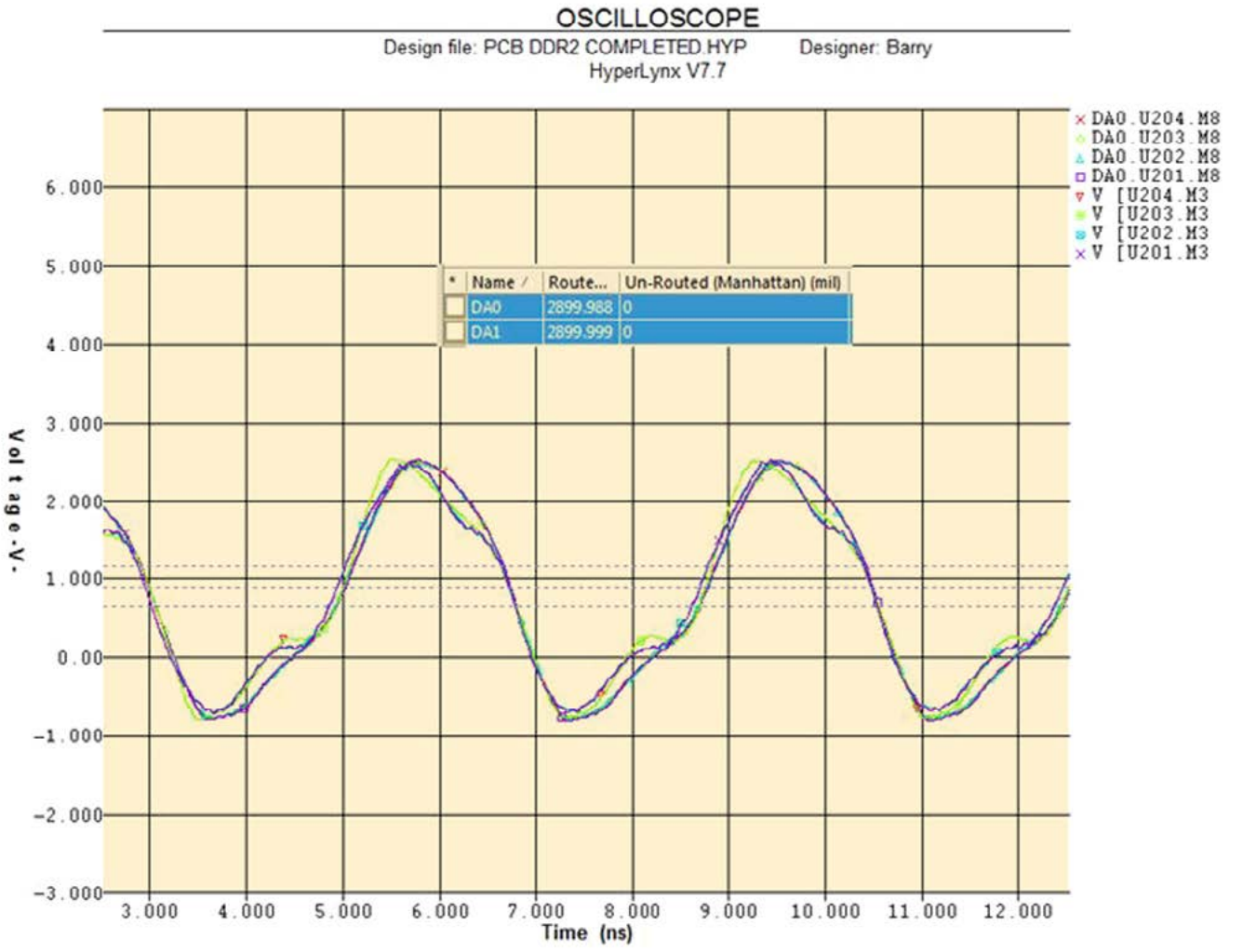

Figure 4: Comparison of two matched length (2,900 mil) traces.

to be employed close to the layer transitions. Decoupling capacitors are normally place near the processor and memory devices which help alleviate this issue.

To prove my point that two matched length traces both of 2,900 mil do not have equal delay, I have simulated two address signals and the results are shown in Figure 4. The delay difference here is 60ps—but still within spec. This is not much admittedly, but they are not matched, as the matched length would suggest. So, although these two signals are exactly the same length, because of the different combination of microstrip and stripline layers plus the fact that the signal propagates faster through serpentine routes, the delays are different.

The slight deviation in the signal waveforms, in Figure 4, is due to the impedance mismatch as the traces separate into two T-sections. Matching the impedance of bifurcated traces is practically impossible with tight routing constraints. However, this is not an issue in this case, since the waveform is stable and the variance does not appear near the trigger point (Vinh).

Points to Remember

- Matched length does not necessarily mean matched delay.
- The longest routes should be placed on the inner layers, as this reduces electromagnetic radiation.

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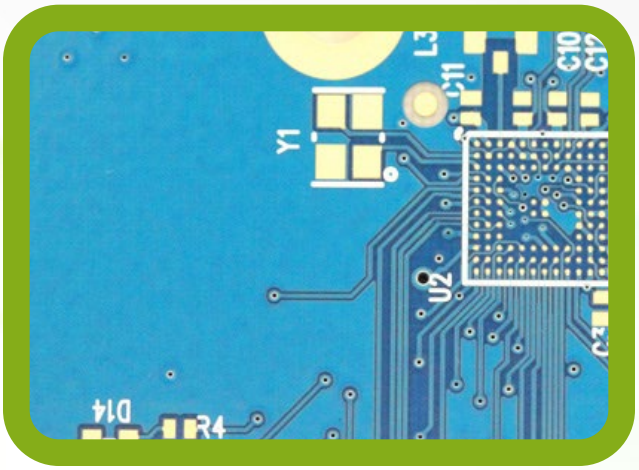

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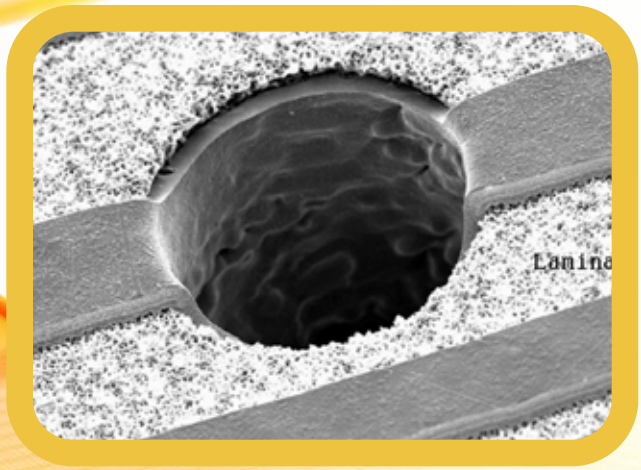

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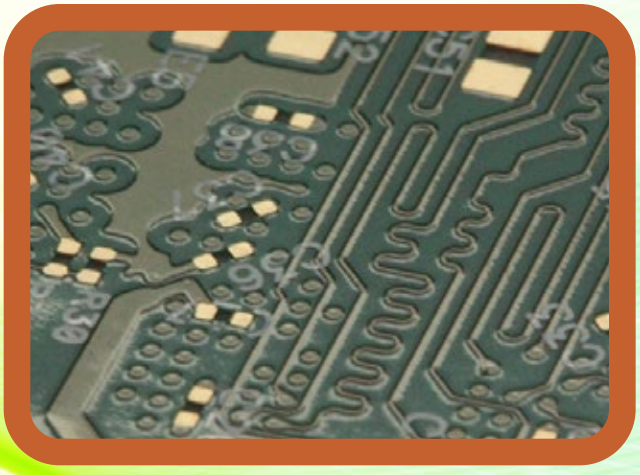

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Matched Length ≠ Matched Delay *continues*

• A trace routed on the inner stripline layer exhibits 4–10 dB less noise then a trace routed on the outer, microstrip layer.

• Microstrip layers are those that are fabricated on the outside of the substrate, top and bottom. The trace has a dielectric material on either side—FR-4 below and air above.

• Microstrip traces are usually faster than stripline traces.

• Stripline traces are totally embedded in dielectric material between planes.

• The propagation delay of a serpentine trace is less than the delay through an equivalent length straight trace. The signal is sped up because a portion of the signal will propagate perpendicular to the serpentine.

• If two traces of equal length are reference to different planes then the return paths may be considerable different and add round-trip delay.

• Although two signals are exactly the same length, they may exhibit different delays.

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References

1. Barry Olney, Beyond Design: Impedance Matching: Terminations, Skewed Again, A New Slant on Matched-Length Routing, Differential Pair Routing, Embedded Signal Routing

2. Howard Johnson: High-Speed Digital Design

3. The ICD Stackup Planner and PDN Planner: www.icd.com.au

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

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Mil/Aero007 News Highlights

Pro-Tech Earns AS9100 Rev C Certification

The company has achieved full certification to AS9100C Quality Management Systems—Requirements for Aviation, Space and Defense Organizations. The successful completion of the requirements and the certification means that Pro-Tech Interconnect Solutions is now certified to AS9100C:2009, ISO 9001:2008 Quality Systems, ISO 13485:2003, MIL-PRF-31032/MIL-PRF-55110, along with ITAR registration.

FTG 4Q Sales Up 12%, 1% FY 2013

"As 2013 ended, FTG had achieved its strategic objective for both its Circuits and Aerospace businesses of establishing manufacturing footprints in Canada, our home base, the United States, the largest aerospace and defense market, and Asia, the fastest growing aerospace market," stated Brad Bourne, president and CEO.

DYCONEX Adds Ticer TCR-HF Foils

DYCONEX announced that it has added Ticer TCR-HF foils to its range of build-up materials. TCR-HF is a low insertion loss NiCr thin film embedded-resistor copper foil, designed especially for high-frequency telecommunications, aerospace, and defense applications.

Schweizer Certified to EN 9100 certification

"By obtaining certificates we have independent parties confirm that our products are manufactured based on internationally determined quality standards and that—related to environment, labour, and health protection—we do more than required by law," stresses Nicolas Schweizer, chief commercial officer.

UAV Market to Hit $114.7B by 2023

A new report says the global UAV market size can be expected to grow to $8,351.11 million by 2018. (HALE/MALE/SUAV) market has the highest business potential throughout the study period whereas the U.S. and Israel will be the maximum revenue generator, among the countries manufacturing UAVs.

Global Comm Sat Imaging Market Sees Demand Increase

According to a new market report "Commercial Satellite Imaging Market—Global Industry Analysis, Size, Share, Growth, Trends, and Forecast, 2013-2019," published by Transparency Market Research, the market for commercial satellite imaging globally is forecast to reach U.S. $5,018.6 million by 2019.

Asia Pacific Takes 36% of World's New Airplane Deliveries

Boeing says strong economic and passenger growth will be main drivers of new airplane demand in the Asia Pacific region. The company estimates the region's airlines will need an additional 12,820 airplanes valued at $1.9 trillion, representing 36% of the world's new airplane deliveries over the next 20 years.

Report: Stretchable Electronics on the Rise

The report provides an examination of how stretchable technology fits into the printed electronics and allied scenes, the materials, and applications that look most promising and the lessons of success and failure.

Carbon Nanotube Fibers Outperform Copper

On a pound-per-pound basis, carbon nanotube-based fibers invented at Rice University have greater capacity to carry electrical current than copper cables of the same mass, according to new research.

Smart Weapons Market Forecasts & Opportunities Report

Smart weapons range from precision-guided artillery rounds and bombs to stand-off missiles. Anti-armor weapons comprise of anti-tank and anti-structure missiles.

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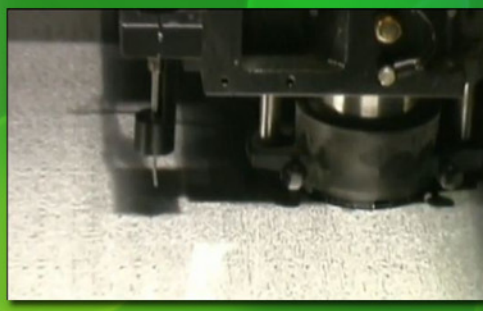

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AS 9100

Checking Cable Performance with VNA

by Istvan Novak
ORACLE

In my December 2013 column Comparing Cable Shields[1], we showed that poor cable shields can result in significant noise pickup from the air, which can easily mask a few mV of noise voltage that we need to measure on a good power distribution rail. We showed a quick comparison of cable shield quality with a signal source and an oscilloscope. In this column, we will look at the same cables in the frequency domain, using a pocket-size vector network analyzer (VNA).

Vector network analyzers are similar to time domain reflectometry (TDR) instruments that many digital engineers may be more familiar with: they both transmit a known signal into the device under test (DUT) and measure the response. TDR instruments use a step waveform with a given rise time; VNAs use a sine wave source sweeping the frequency within a user-defined range. VNAs have long been popular in microwave engineering and more recently in high-speed digital engineering. They measure what are called scattering (S) parameters, which are the complex ratios of transmitted and reflected waves.

Figure 1: The USB-connected miniVNA Pro pocket-size VNA.

In recent years, small, low-cost, portable VNAs have become available. Measured data in this column was collected with a miniVNA Pro[2], a pocket-sized VNA. It operates over the 0.1–200 MHz frequency range. It is battery-powered and features USB and Bluetooth connectivity (Figure 1). We hooked up a two-port DUT to the DUT and DET SMA connectors. The instrument injects sine waves (swept from 0.1–200 MHz or in any user-defined subband of it) into the cable connected to the SMA labeled DUT, measures sine waves propagating back from the DUT SMA (reflection) and the DET

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CHECKING CABLE PERFORMANCE WITH VNA *continues*

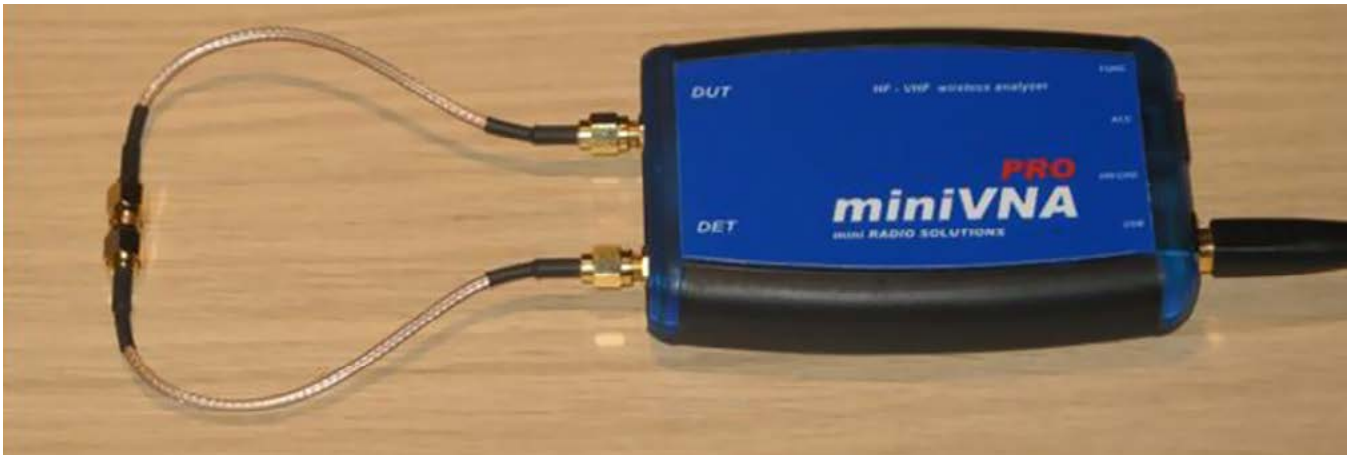

Figure 2: Through calibration layout.

SMA (transmission), and compares the measured received sine waves to the injected sine waves to characterize reflection (e.g., S_{11}) and transmission (e.g., S_{21}). With this instrument, we can measure the full S matrix of a two-port DUT, though to get the full matrix, we have to manually set up four independent measurements. The instrument comes with open, load and short SMA calibration standards, shown on the lower left in Figure 1.

For a nominally symmetrical and reciprocal DUT with two connections, like our cables, there are only two parameters to measure: reflection (S_{11}) and transmission (S_{21}). If the DUT is really symmetrical, reflection measured from either connection will be the same ($S_{11} = S_{22}$). Similarly, a reciprocal DUT will give us the same transmission measurement result, regardless which direction we measure it ($S_{21} = S_{12}$).

Before any measurement is taken, we have to perform a calibration to the end of the connecting cables. Figure 2 shows the through calibration. The two short beige cables are connected with an SMA through piece, also called SMA slug. After calibration, the residual transmission reading by disconnecting the two cables is < - 80dB, pretty good from a pocket-size instrument. The two short beige cables have high quality and therefore we get the same noise floor reading regardless where we open the connection; whether we just remove the slug but leave the two cables connected to the VNA or if we remove the two cables as well.

To check further the shield quality of our coaxial cables, I connected the two cables under test to the VNA, leaving in place the short high-quality cables shown in Figure 2 that were part of the through calibration.

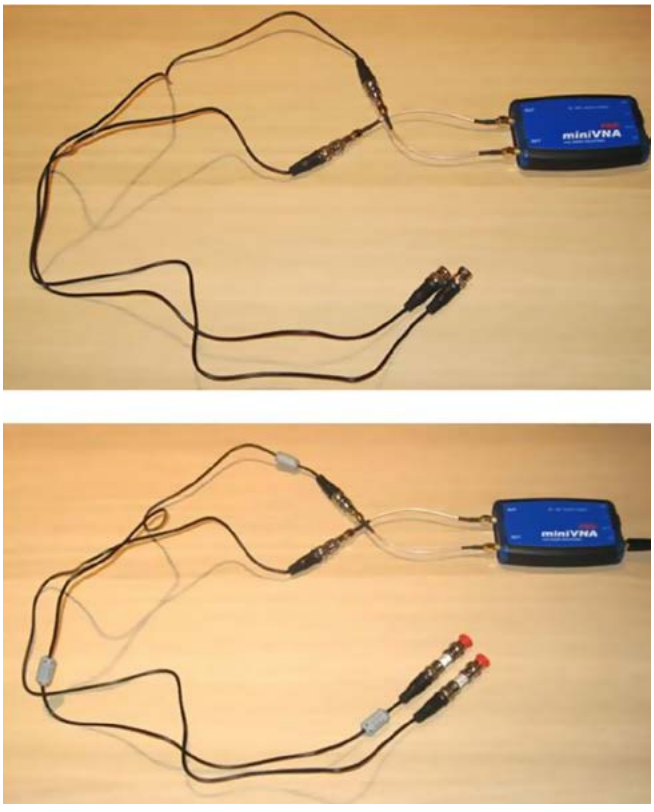

Figure 3: Layout to measure the two poor quality cables. Top: Both cables with open end. Bottom: Both cables terminated.

CHECKING CABLE PERFORMANCE WITH VNA *continues*

A poorly-shielded cable was connected to the DUT port to serve as the aggressor. Several different victim cables were connected, in turn, to the DET port. The aggressor and victim cables lay loosely near each other, as shown in Figure 3.

The results measured for each victim configuration are shown in Figure 4:

- Red trace: High-quality, well-shielded victim cable, with both cables open-ended.
- Blue trace: Poorly-shielded victim cable, with both cables open-ended.
- Green trace: Poorly-shielded victim cable, with both cables terminated.
- Grey trace: Poorly-shielded victim cable, with both cables terminated, with ferrite-absorbers on the victim cable.

The upper photo in Figure 3 shows both cables open-ended, and the lower photo shows both cables terminated and with ferrite absorbers on the victim.

The VNA was set to measure transmission (S_{21}), which in this case represents the crosstalk between the two cables through the cable braid

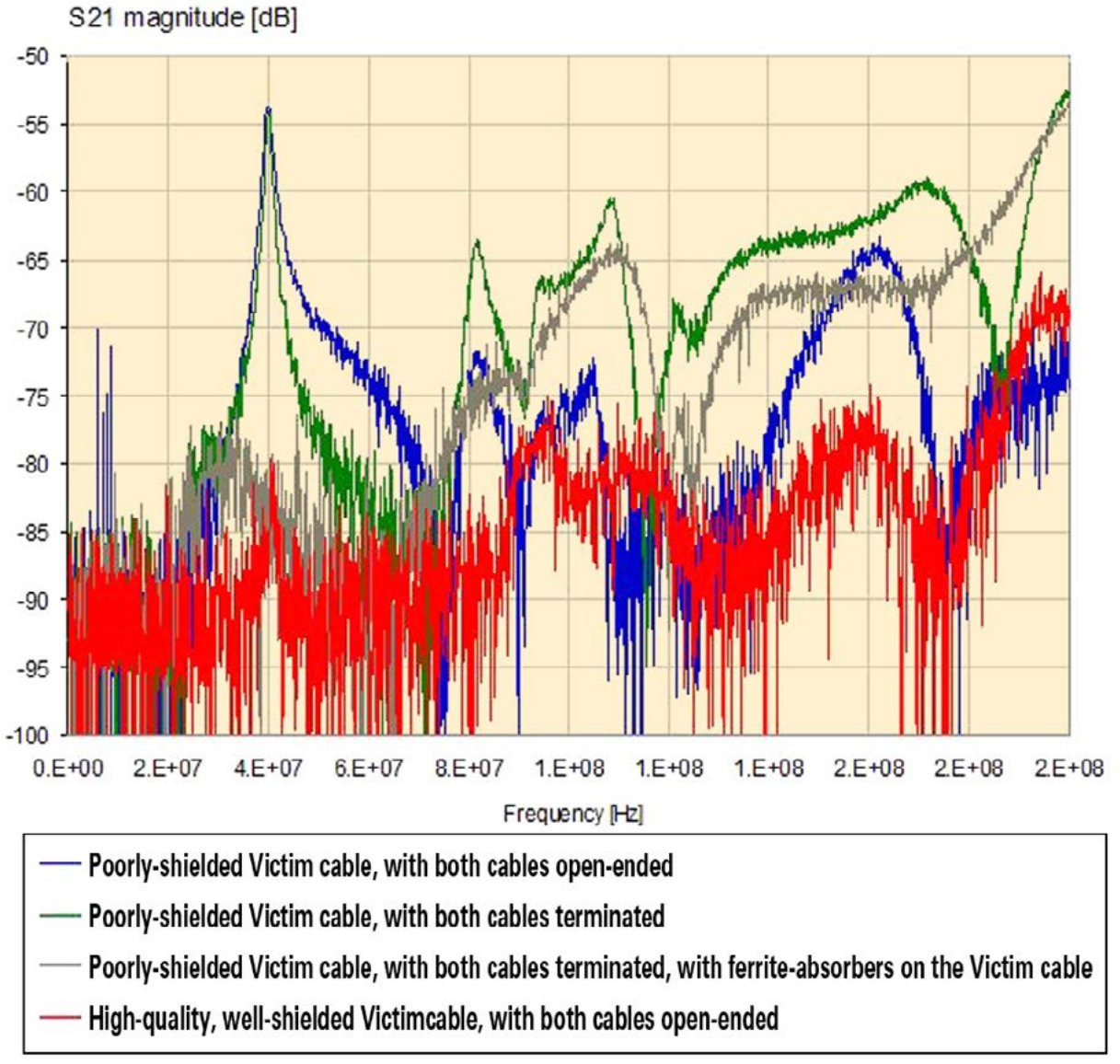

Figure 4: Crosstalk through the cable braid and air for four different cable combinations.

and air. The two extremes are the blue and red traces: blue refers to the poorly shielded cable, and the red trace shows the transmission with a quality cable, both with open ends. These correspond to the information in these two cases in Reference 1. The red trace is hardly above the noise floor of the instrument; the blue trace has multiple big peaks. The sharp 40MHz peak is related to the quarter-wave resonance of the cables, which is one quarter of the inverse of the end-to-end delay. With termination at the far end (green trace) the crosstalk pattern changes, but only ever so slightly: it is somewhat lower in the 40–70 MHz frequency range, but it gets higher above 80 MHz. With the poor quality cable, we can lower the 40MHz peak by putting absorbing ferrites around the cable (shown by the grey trace). The 40 MHz peak got lower by about 25 dB, and the higher-frequency resonances got also reduced by 5–10 dB.

This illustrates that when at least one of the two cables has a quality shield, the coupling path between them is blocked, and the crosstalk drops, regardless of how the far ends are terminated. When both the aggressor and victim cables have poor shielding, the crosstalk at the resonance frequencies is significant, though termination and ferrite absorbers can help a little. In an electromagnetic susceptibility scenario, such as the one we described in the column in Reference 1, we focus on the victim and may not even know where the aggressor is or what generates the aggressor signal. In those situations the quality of the cable shield makes a big difference. **PCBDESIGN**

References

1. Quiet Power column, Comparing Cable Shields, December 2013.

2. MiniVNA-Pro available here.

Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To read past columns, or to contact Novak, click here.

The Rise of the Monolithic 3D Chip

Ever since the integrated circuit made its debut, semiconductors have been "single-story" affairs. But chipmakers are now considering ways to build additional transistor-packed layers right on top of the first.

In a monolithic 3D circuit, a chipmaker would simply continue building on top of a 2D chip, adding an additional layer of silicon on which another set of circuitry could be built. The vertical connections made in this process could potentially be as dense as those found on a 2D logic chip. If such circuits could be made, chipmakers might be able to avoid all the technical complications associated with shrinking circuitry.

But the process is less straightforward than it sounds. Temperatures upwards of 1,000°C are typically used to force dopant atoms into silicon and create the semiconductor portions of the transistor. Applying such heat to create a second layer of transistors could destroy crucial components in the first, including salicide, a metal-silicon alloy used to help carry signals in and out of devices.

When it comes to memory, monolithic 3D fabrication already seems to be making inroads in industry. In August, Samsung announced it had begun production on NAND flash with memory cells arranged along dense vertical lines, and other companies have similar plans. But details are scant on the particulars of the manufacturing process.

"Memory looks like it's already commercialized. Logic has a long way to go," says Sung Kyu Lim of Georgia Tech. In the future, he says, "the only way to go to add more devices will be vertical."

News Highlights from PCBDesign007 this Month

① Mentor Achieves All-time Records in Q4, FY 2013

"The fourth quarter and full year achieved multiple all-time records for Mentor Graphics," said Walden C. Rhines, chairman and CEO. "Record annual bookings, record fourth quarter and annual revenues, record fourth quarter and annual levels of profitability and earnings per share, all evidence the value of Mentor's technology, products and the merits of our strategy."

② Fabstream and Electro-Labs.com Form Partnership

As part of the partnership, Electro-Labs.com will use Fabstream's free, SoloPCB design software to publish projects based on the SoloPCB design flow. This new online offering brings together original designs and projects to help engineers create electronic projects and systems.

③ Zuken Appoints Fusion CADSoft as New CADSTAR Reseller

Zuken announces the expansion of its CADSTAR reseller network in North America with the addition of Fusion CADSoft. CADSTAR is Zuken's powerful and easy-to-use desktop PCB design software for small- to medium-sized workgroups.

④ Agilent ADS 2014 Enhances Design Productivity

Agilent Technologies Inc. has announced a powerful new version of the Agilent EEsof EDA Advanced Design System software (ADS). Designed to dramatically improve design productivity and efficiency with new technologies and capabilities, ADS 2014 is the software's most significant ADS release to date.

5 Altium's Designer 14 Wins DesignVision Award

The company announces that DesignCon has honored Altium Designer 14 with a 2014 DesignVision Award in the PCB Design category. The award program celebrates the achievements of the most innovative electronics companies and the unique tools that support customer needs to improve and simplify the design process.

6 EPTAC Expands IPC Training Centers Across U.S., Canada

EPTAC Corporation has acquired multiple IPC Certification Center licenses for a number of locations across the United States and Canada. New EPTAC programs licensed via IPC include the new IPC-6012 bare board specification program still in development and the current designer certifications, CID and CID+, which are specifically targeted to support the PCB design market.

7 Cadence Intros New Allegro TimingVision Environment

Cadence Design Systems, Inc. has announced new Allegro TimingVision environment, which reduces interface timing closure by up to 67%. Available within Cadence Allegro PCB Designer, TimingVision environment makes it possible for PCB designers to save significant time in ensuring that signals in an interface meet timing requirements.

8 IEEE Forms Groups to Standardize EDA Steps

The IEEE Standards Association has approved the formation of the IEEE P1666.1 SystemC Analog/Mixed-Signal (AMS) Extensions Working Group and the IEEE P2401 LPB – Standard Format for Large Scale Integration (LSI)-Package-Board Interoperable Design Working Group.

9 CadSoft EAGLE Introduces New Simulation Tool

The recently signed cooperation between Felicitas Customized Engineering GmbH and CadSoft Computer GmbH gives EAGLE users access to the new simulation tool, developed by Felicitas Customized Engineering. Within this cooperation, Felicitas uses EAGLE as a front end for their simulation tool for signal integrity, PCBSim, which will be available through a newly developed interface.

10 DesignCon 2014 a Success: Post Conference Report

UBM Tech, the daily source of essential business and technical information for decision makers in the electronics industry, held its annual DesignCon conference and expo last week in Santa Clara, California.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

SMTA Webtorial: Tin Whiskers—All You Should Know
March 11 and 13, 2014
Online

IPC APEX EXPO 2014
March 23-27
Las Vegas, Nevada, USA

Electronics New England
March 26–27, 2014
Boston, Massachusetts, USA

Printed Electronics Europe 2014
April 1–4, 2014
Berlin, Germany

Internet of Things and WSN Europe 2014
April 1–2, 2014
Berlin, Germany

South East Asia Technical Conference on Electronics Assembly
April 8–10, 2014
Penang, Malaysia

Intermountain (Boise) Expo & Tech Forum
April 17, 2014
Boise, Idaho, USA

Smart Fabrics & Wearable Technology 2014
April 23–25, 2014
San Francisco, California, USA

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

PUBLISHER: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:
GROUP EDITORIAL DIRECTOR: **RAY RASMUSSEN**
(916) 337-4402; ray@iconnect007.com

MANAGING EDITOR: **ANDY SHAUGHNESSY**
(404) 806-0508; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:
PRODUCTION MANAGER: **MIKE RADOGNA**
mike@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA**

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